Dense-Pac Microsystems, Inc.

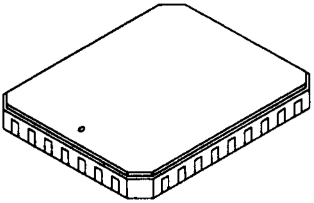
DPS9264G

8K X 8 CMOS SRAM MONOLITHIC LCC

DESCRIPTION:

The DPS9264G-90, -100, -120, -150 is a 8K X 8 Static Random Access Memory (SRAM) fabricated with a CMOS silicon gate process. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The DPS9264G is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required. All devices offer the advantages of low power dissipation, low cost and high performance.

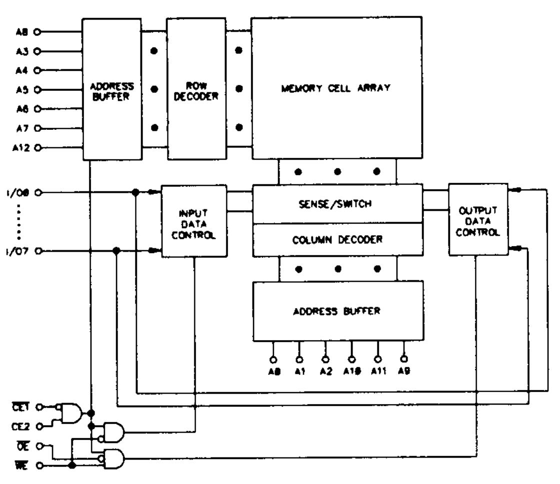


FEATURES:

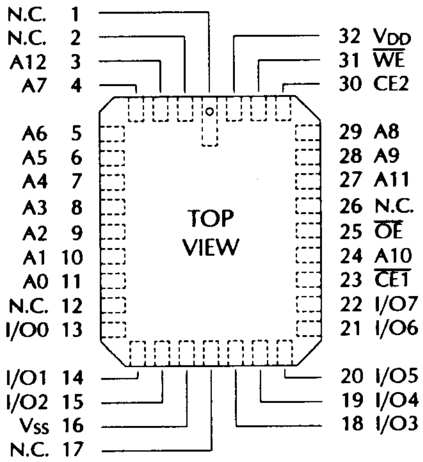
- 8,192 Words by 8-Bits Organization
- Access Times: 90, 100, 120, 150ns (max.)
- Low Power: 1.5mW (max.) Full Standby
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, ±10% Tolerance
- Three State Output
- Standard JEDEC 32-Pad LCC Package

PIN NAMES	
A0-A12	Address Inputs
I/O0-I/O7	Data Input/Output
$\overline{\text{CE1}}$, CE2	Chip Enables
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAMS



TRUTH TABLE						
Mode	$\overline{\text{CE1}}$	CE2	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O	I_{CC}
Not Selected	H	X	X	X	HIGH-Z	Standby
Not Selected	X	L	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	H	HIGH-Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

L = LOW H = HIGH X = Don't Care

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	°C
V_{DD}	Supply Voltage[1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage[1]	-0.3[2] to V_{DD}+0.5	V

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.3[2]		0.8	V

CAPACITANCE[4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	7	pF	V_{IN} = 0V
C_{ADR}	Address Input	7		
C_{WE}	Write Enable	7		
C_{OE}	Output Enable	7		
$C_{I/O}$	Data Input/Output	10		

DC OPERATING CHARACTERISTICS: Over the operating ranges.

Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-2	2	-2	2	-2	2	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{\text{CE1}}$ and $\overline{\text{OE}}$ = V_{IH}, CE2 and $\overline{\text{WE}}$ = V_{IL}	-2	2	-2	2	-2	2	µA
I_{CC1}	Operating Supply Current	$\overline{\text{CE1}}$ = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	-	40	-	45	-	50	mA
I_{CC2}	Average Operating Supply Current	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 0mA, t_{CYC} = min.	-	60	-	65	-	70	mA
I_{SB1}	Standby Supply Current (TTL)	$\overline{\text{CE1}}$ = V_{IH} or CE2 = V_{IL}	-	2	-	2	-	2	mA
I_{SB2}	Standby Supply Current (CMOS)	$\overline{\text{CE1}}$ = CE2 ≥ V_{DD} -0.2V or CE2 ≤ 0.2V	-	120	-	150	-	275	µA
I_{DR3}	3.0V Data Retention Supply Current	$\overline{\text{CE1}}$ = CE2 ≥ V_{DD} -0.2V or CE2 ≤ 0.2, V_{DD} = 3.0V	-	30	-	60	-	110	µA
I_{DR2}	2.0V Data Retention Supply Current	$\overline{\text{CE1}}$ = CE2 ≥ V_{DD} -0.2V or CE2 ≤ 0.2, V_{DD} = 2.0V	-	25	-	50	-	100	µA
V_{OL}	Output Voltage Low	I_{OUT} = 2.1mA	-	0.4		0.4	-	0.4	V
V_{OH}	Output Voltage High	I_{OUT} = -1.0mA	2.4	-	2.4	-	2.4	-	V

DATA RETENTION CHARACTERISTICS: Over the operating ranges.

Symbol	Parameter	Test Condition	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{\text{CE1}}$ = CE2 ≥ V_{DD} -0.2V or CE2 ≤ 0.2V	2.0	5.5	V
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveforms	0	-	ns
t_R	Operation Recovery Time	See Data Retention Waveforms	t_{RC}*	-	ns

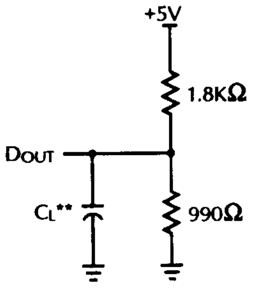
* t_{RC}=Read Cycle Time.

AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.
** Including Probe and Jig Capacitance.

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}

Figure 1. Output Load



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges [6,7]

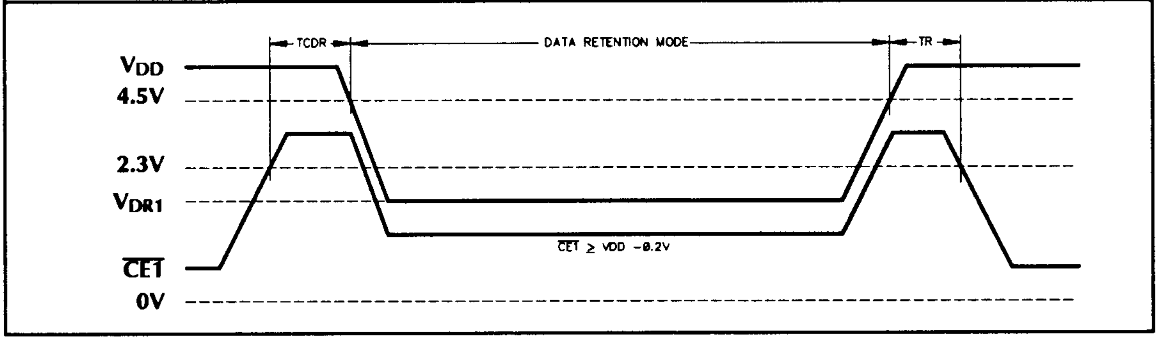
No.	Symbol	Parameter	-90†		-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	90		100		120		150		ns
2	t_{AA}	Address Access Time		90		100		120		150	ns
3	t_{CO1}	Chip Enable ($\overline{CE1}$) to Output Valid		90		100		120		150	ns
4	t_{CO2}	Chip Enable (CE2) to Output Valid		90		100		120		150	ns
5	t_{OE}	Output Enable to Output Valid		50		50		60		70	ns
6	t_{LZ1}	Chip Enable ($\overline{CE1}$) to Output in LOW-Z [4, 5]	10		10		10		10		ns
7	t_{LZ2}	Chip Enable (CE2) to Output in LOW-Z [4, 5]	10		10		10		10		ns
8	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	5		5		5		5		ns
9	t_{HZ1}	Chip Enable ($\overline{CE1}$) to Output in HIGH-Z [4, 5]		35		35		40		50	ns
10	t_{HZ2}	Chip Enable (CE2) to Output in HIGH-Z [4, 5]		35		35		40		50	ns
11	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		35		35		40		50	ns
12	t_{OH}	Output Hold from Address Change	10		10		10		10		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [6,7]

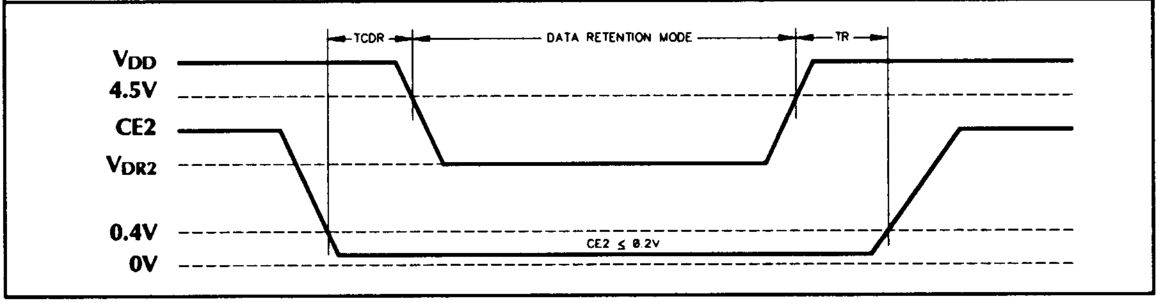
No.	Symbol	Parameter	-90†		-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	90		100		120		150		ns
14	t_{CW1}	Chip Enable ($\overline{CE1}$) to End of Write	75		80		85		90		ns
15	t_{CW2}	Chip Enable (CE2) to End of Write	75		80		85		90		ns
16	t_{AW}	Address Valid to End of Write	75		80		85		90		ns
17	t_{AS}	Address Set-up Time***	0		0		0		0		ns
18	t_{WP}	Write Pulse Width	60		65		70		75		ns
19	t_{WR}	Write Recover Time	0		0		0		0		ns
20	t_{WHZ}	Write Enable to Output in HIGH- Z [4, 5]		35		35		40		45	ns
21	t_{DW}	Data to Write Time Overlap	50		50		50		50		ns
22	t_{DH}	Data Hold Time	0		0		0		0		ns
23	t_{OW}	Output Active from End of Write	5		5		5		5		ns

† Commercial Only.
*** Valid for both Read and Write Cycles.

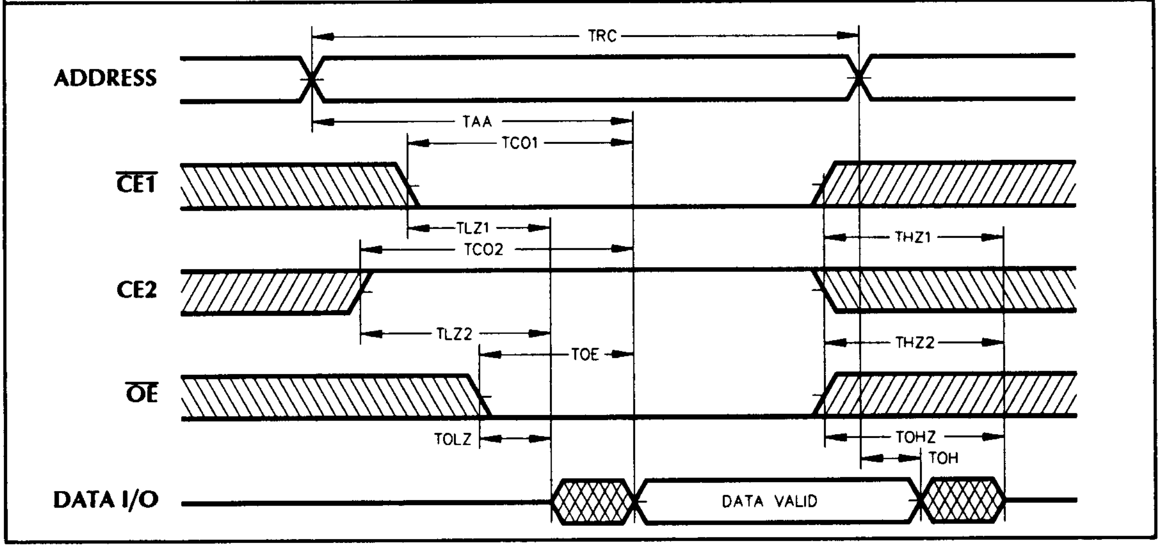
DATA RETENTION WAVEFORM: $\overline{CE1}$ Controlled.



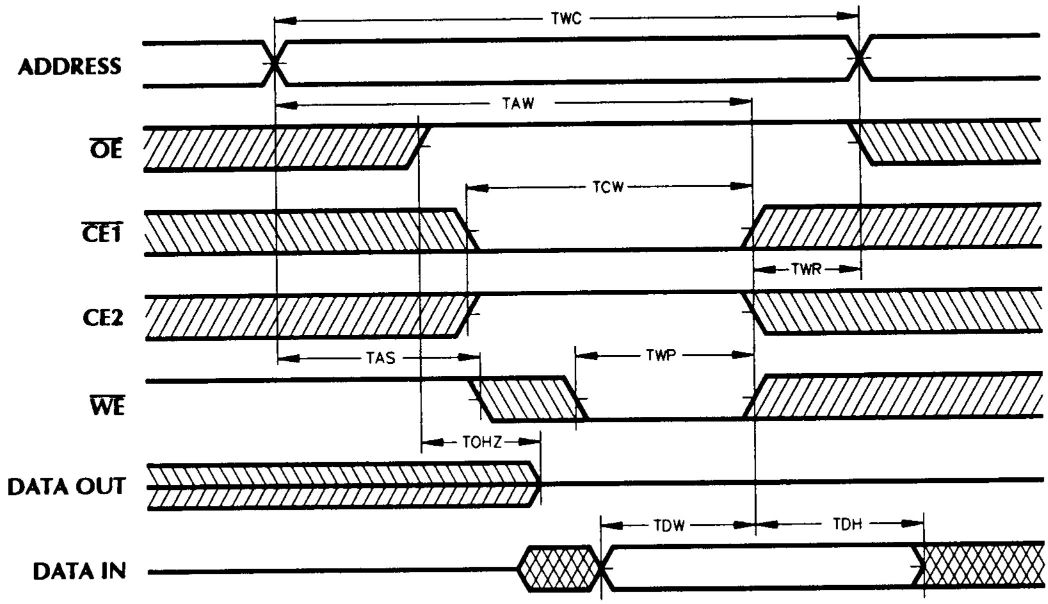
DATA RETENTION WAVEFORM: CE2 Controlled.



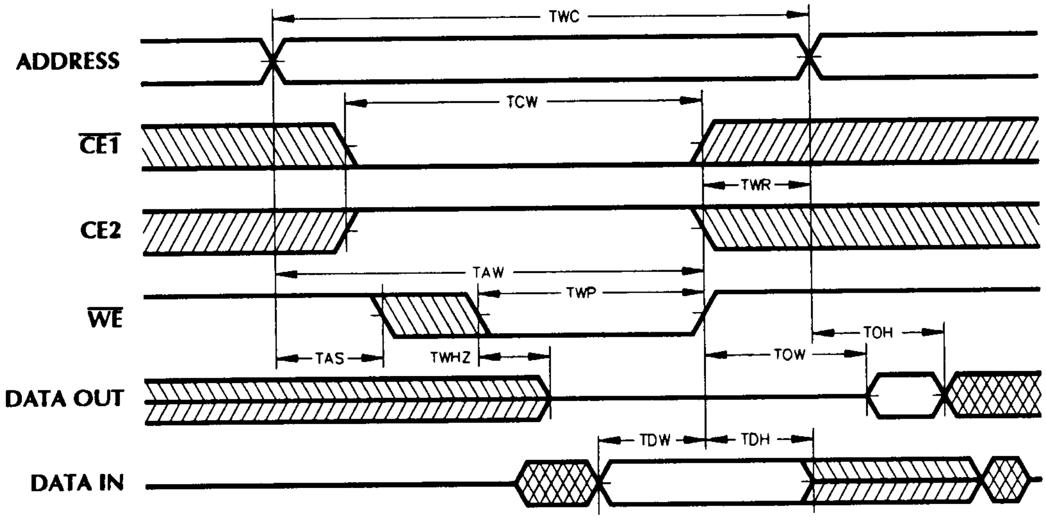
READ CYCLE



WRITE CYCLE 1: $\overline{\text{WE}}$ Controlled. $\overline{\text{OE}}$ Clocked.



WRITE CYCLE 2: $\overline{\text{CE}}$ Controlled. $\overline{\text{OE}}$ is LOW.



ORDERING INFORMATION

DP	S9264G –	XX	X
PREFIX	DEVICE TYPE	SPEED	GRADE

GRADE:

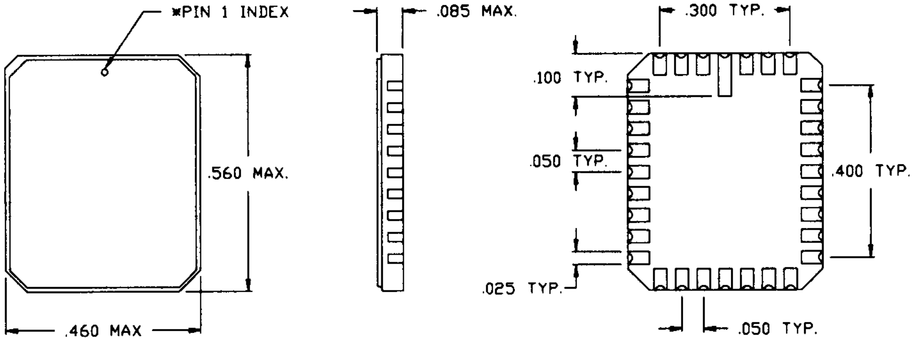
C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	-40°C to +85°C
M	MILITARY	-55°C to +125°C
B	MIL-PROCESSED	-55°C to +125°C

SPEED:

90	90ns
10	100ns
12	120ns
15	150ns

DEVICE TYPE: 8KX8 CMOS SRAM 32-PAD LCC

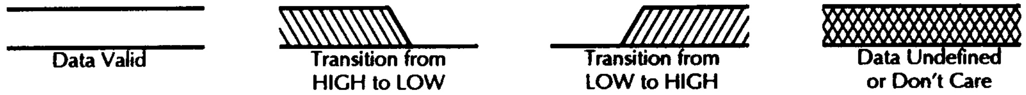
MECHANICAL DIAGRAM



NOTES:

1. All voltages are with respect to Vss.
2. -1.0V min. for pulse width less than 20ns (V_{IL} min.=-0.3V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is sampled and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state; and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY



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