Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 256K (64K x 4-BIT) SRAM

IDT10504
IDT100504
IDT101504

FEATURES:

- 65,536-words x 4-bit organization
- Address access time: 7/8/10/12/15 ns
- Low power dissipation: 1000mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- Standard through-hole and surface mount packages
- Guaranteed-performance die available for MCMs/hybrids

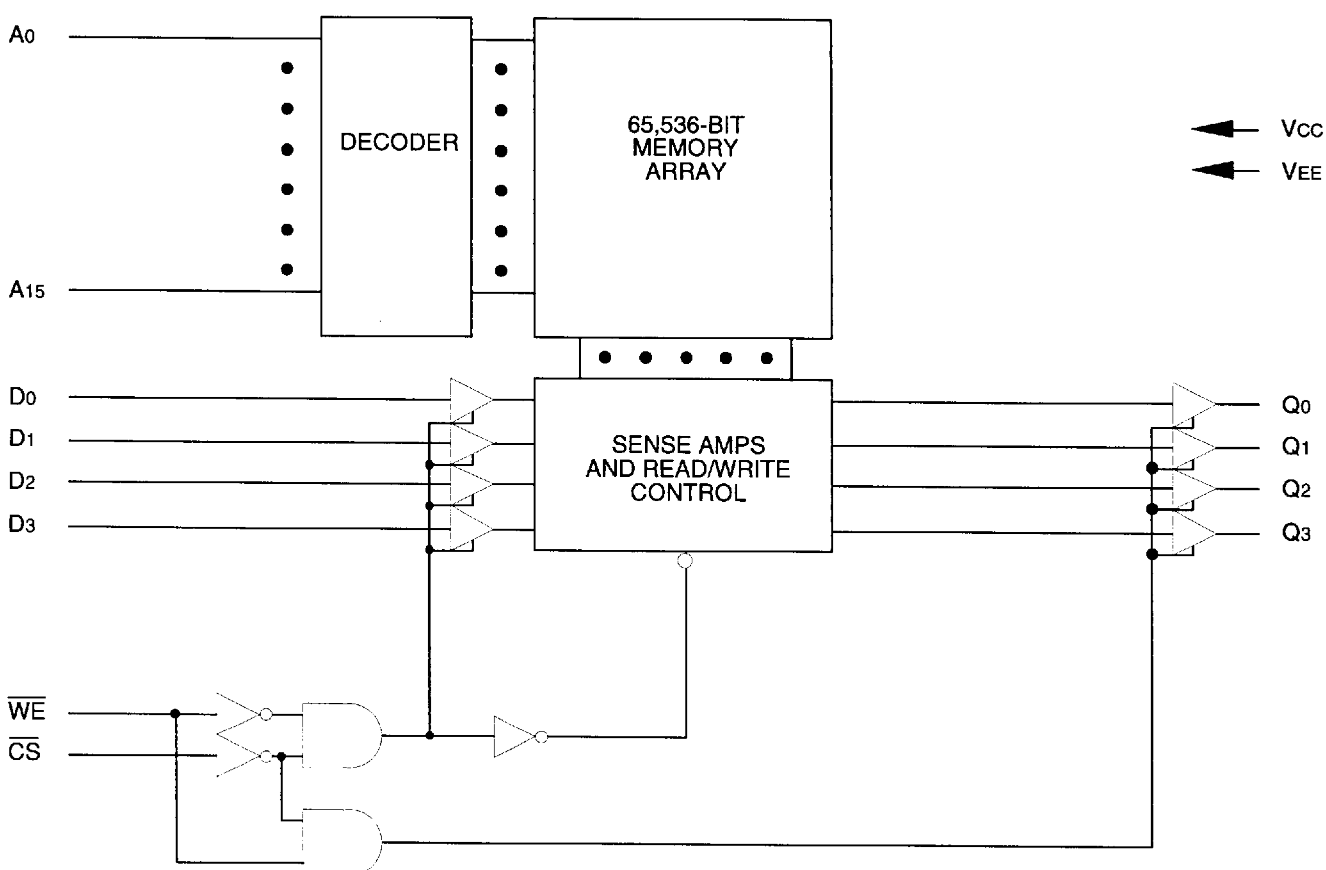
DESCRIPTION:

The IDT10504, IDT100504 and IDT101504 are 262,144-bit high-speed BiCEMOS™ ECL static random access memories organized as 64Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. The devices have been configured to follow the standard ECL SRAM JEDEC pinout. Because they are manufactured in BiCEMOS™ technology, power dissipation is greatly reduced over equivalent bipolar devices. Low power operation provides higher system reliability and makes possible the use of the plastic SOJ package for high-density surface mount assembly.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. DataIN setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

FUNCTIONAL BLOCK DIAGRAM



2780 drw 01

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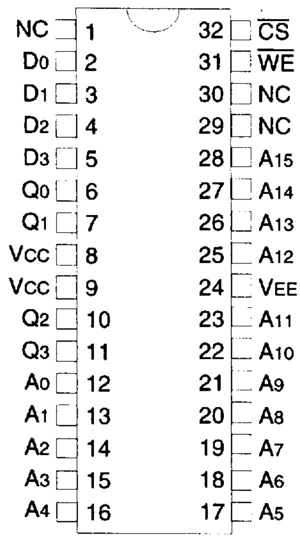
COMMERCIAL TEMPERATURE RANGE **SEPTEMBER 1992**

PIN CONFIGURATION



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Top View

PIN DESCRIPTIONS

Symbol	Pin Name
A_0 through A_{15}	Address Inputs
D_0 through D_3	Data Inputs
Q_0 through Q_3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
V_{EE}	More Negative Supply Voltage
V_{CC}	Less Negative Supply Voltage

2780 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
C_{IN}	Input Capacitance	4	—	3	—	pF
C_{OUT}	Output Capacitance	6	—	3	—	pF

2780 tbl 02

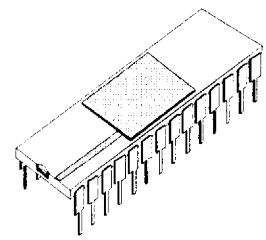
TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DataOUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

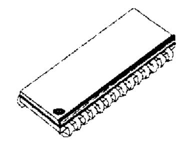
2780 tbl 03

NOTE:
1. H=High, L=Low, X=Don't Care

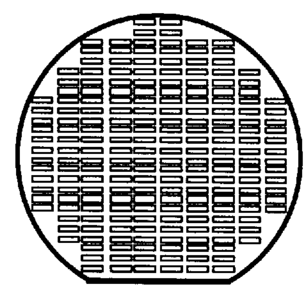
PACKAGES



400-Mil-Wde
CERAMIC PACKAGE
C32-2
2780 drw 03



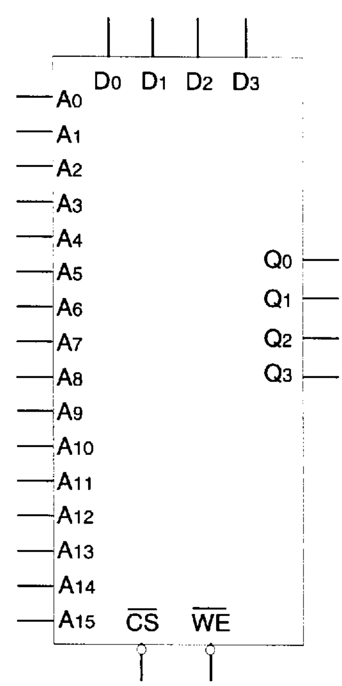
300-Mil-Wide
PLASTIC SOJ PACKAGE
SO32-2
2780 drw 04



Hi-Rel Die
For Hybrid and MCM
Applications

2780 drw 05

LOGIC SYMBOL



2780 drw 06

4825771 0022039 515

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature	10K 100K 101K	0 to +75 0 to +85 0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperatuure	Ceramic Plastic	-65 to +150 -55 to +125	°C
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

NOTE:
2780 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC ELECTRICAL OPERATING RANGES

I/O	V_{EE}	T_A
10K	-5.2V ± 5%	0 to +75°C, air flow exceeding 2 m/sec
100K	-4.5V ± 5%	0 to +85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 to +75°C, air flow exceeding 2 m/sec

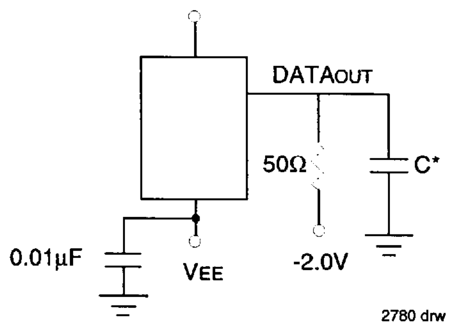
2780 tbl 05

DC ELECTRICAL CHARACTERISTICS (1)

		10K			100K/101K		
Symbol	Parameter	Min.	Max.	TA	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage (V_{IN}= $V_{IH(Max)}$ or $V_{IL(Min)}$)	-1000 -960 -900	-840 -810 -720	0°C 25°C 75°C	-1025	-880	mV
V_{OL}	Output LOW Voltage (V_{IN}= $V_{IH(Max)}$ or $V_{IL(Min)}$)	-1870 -1850 -1830	-1665 -1650 -1625	0°C 25°C 75°C	-1810	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage (V_{IN}= $V_{IH(Min)}$ or $V_{IL(Max)}$)	-1020 -980 -920	— — —	0°C 25°C 75°C	-1035	—	mV
V_{OLC}	Output Threshold LOW Voltage (V_{IN}= $V_{IH(Min)}$ or $V_{IL(Max)}$)	— — —	-1645 -1630 -1605	0°C 25°C 75°C	—	-1610	mV
V_{IH}	Input HIGH Voltage (Guaranteed Input Voltage High for All Inputs)	-1145 -1105 -1045	-840 -810 -720	0°C 25°C 75°C	-1165	-880	mV
V_{IL}	Input LOW Voltage (Guaranteed Input Voltage Low for All Inputs)	-1870 -1850 -1830	-1490 -1475 -1450	0°C 25°C 75°C	-1810	-1475	mV
I_{IH}	Input HIGH Current V_{IN}= $V_{IH(Max)}$: CS Others	— —	220 110	— —	— —	220 110	µA µA
I_{IL}	Input LOW Current V_{IN}= $V_{IL(Min)}$: CS Others	0.5 -50	170 90	— —	0.5 -50	170 90	µA µA
I_{EE}	Supply Current	-220	—	—	-200 (100K) -220 (101K)	— —	mA

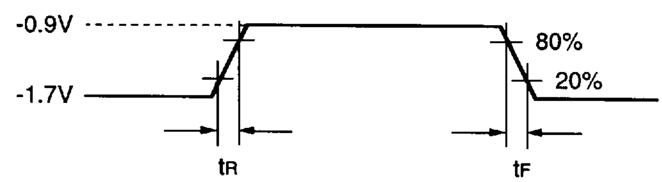
NOTE:
1. RL = 50Ω to -2V, air flow exceeding 2 m/sec.

AC TEST LOAD CONDITION



*Includes probe and jig capacitance.
C < 5pF (7ns speed grade)
C < 30pF (all other speed grades)

AC TEST INPUT PULSE



$t_R = t_F = 1.5$ns typ.

Note: All timing measurements are referenced to 50% input levels.

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RISE/FALL TIME

Symbol	Parameter	Min.	Typ.	Max.	Unit
tR	Output Rise Time	—	1.5	—	ns
tF	Output Fall Time	—	1.5	—	ns

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FUNCTIONAL DESCRIPTION

The IDT10504, IDT100504, and IDT101504 BiCEMOS ECL static RAMs provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the conventional center power pinout and functionality for 64Kx4 ECL SRAMs.

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select (CS). The Address (ADDR) settles and data appears on the output after time t_{AA}. Note that DataOUT is held for a short time (t_{OH}) after the address begins to change for the next access, then ambiguous data is on the bus until a new time t_{AA}.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input (WE) to control the write to the SRAM array. While CS and ADDR must be set-up when WE goes low, DataIN can settle after the falling edge of WE, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If CS is held low (active) and addresses remain unchanged, the Data OUT pins will output the written data after "Write Recovery time" (t_{WR}).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads.

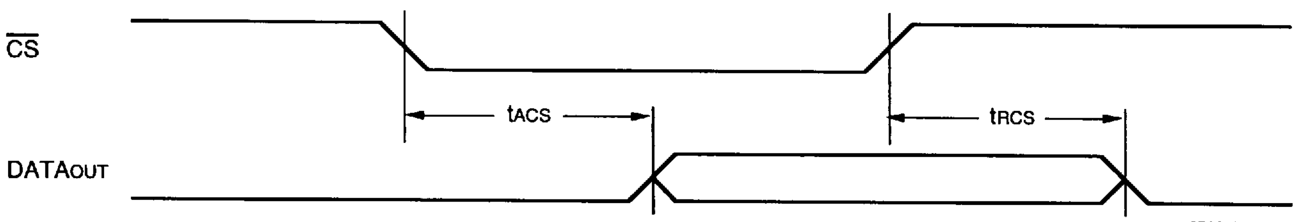
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	S7 Min.	S7 Max.	S8 Min.	S8 Max.	S10 Min.	S10 Max.	S12, 15 Min.	S12, 15 Max.	Unit
Read Cycle										
tACS	Chip Select Access Time	—	3	—	3	—	4	—	4	ns
tRCS	Chip Select Recovery Time	—	3	—	3	—	4	—	4	ns
tAA	Address Access Time	—	7	—	8	—	10	—	12	ns
tOH	Data Hold from Address Change	3	—	3	—	3	—	3	—	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.
2. Output load capacitance, C < 5pF (7ns speed grade only), see "AC Load Test Condition" on previous page.

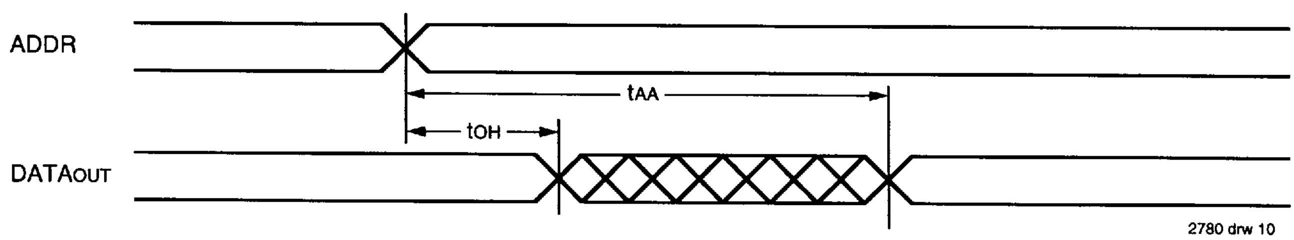
2780 tbl 07

READ CYCLE GATED BY CHIP SELECT (1, 2)



2780 drw 09

READ CYCLE GATED BY ADDRESS (1, 3)



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NOTE:
1. WE is high for read cycle.
2. Address valid prior to or minimum of tAA-tACS beforeCS active.
3. CS active prior to or minimum tAA-tACS after address valid.

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter(1)	S7		S8		S10		S12, 15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tw	Write Pulse Width (twSA = minimum)	5	—	6	—	8	—	8	—	ns
twSD	Data Set-up Time	0	—	0	—	0	—	0	—	ns
twSD2(2)	Data Set-up Time to WE High	5	—	5	—	5	—	5	—	ns
twSA	Address Set-up Time (tw = minimum)	0	—	0	—	0	—	0	—	ns
twSCS	Chip Select Set-up Time	0	—	0	—	0	—	0	—	ns
twHD	Data Hold Time	2	—	2	—	2	—	2	—	ns
twHA	Address Hold Time	2	—	2	—	2	—	2	—	ns
twHCS	Chip Select Hold Time	2	—	2	—	2	—	2	—	ns
twS	Write Disable Time	—	5	—	5	—	5	—	5	ns
twR(3)	Write Recovery Time	—	5	—	5	—	5	—	5	ns

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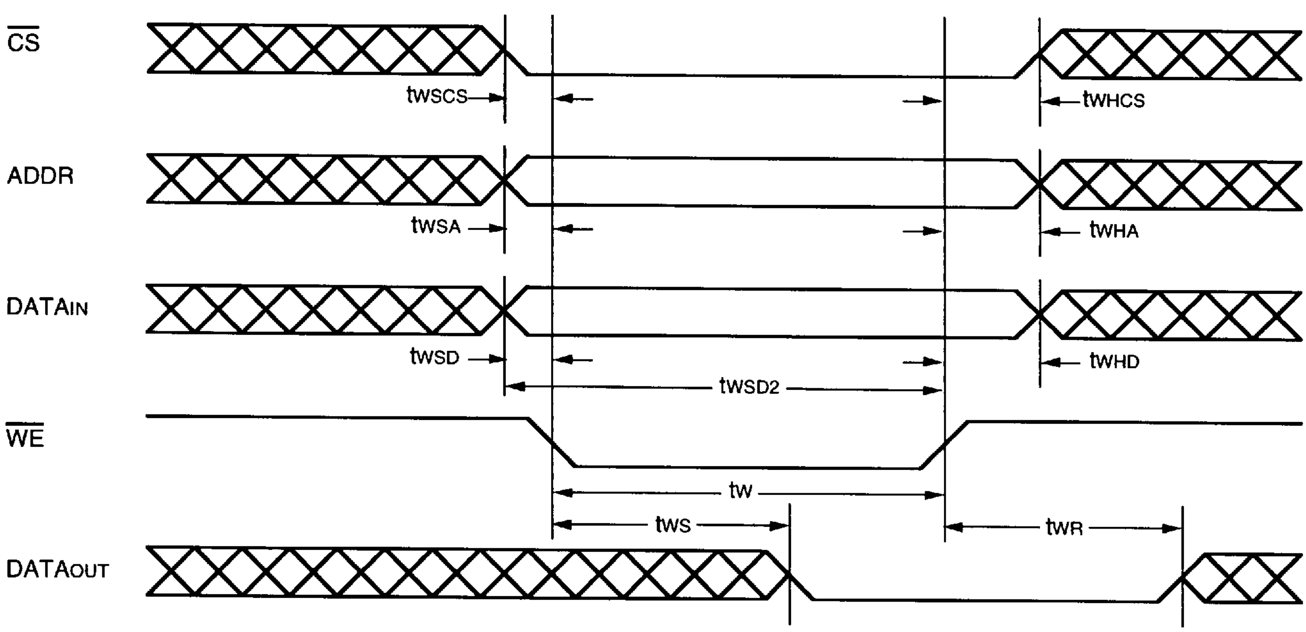
NOTE:
1. Input and Output reference level is 50% point of waveform.
2. twSD is specified with respect to the falling edge of WE for compatibility with bipolar part specifications, but this device actually only requires twSD2 with respect to rising edge of WE.
3. twR is defined as the time to reflect the newly written data on the Data Outputs (Q0 to Q3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2780 drw 11

4825771 0022043 T4b

ORDERING INFORMATION

IDT nnnnn (Device Type) aa (Architecture) nn (Speed) a (Package) a (Process/Temp. Range)

Field	Code	Description
Process/Temp. Range	Blank	Commercial
Package	C	Sidebraze DIP
	U(1)	Hi-Rel Die for MCMs and/or Hybrids
	Y	Plastic SOJ
Speed	7, 8, 10, 12, 15	Speed in Nanoseconds
Architecture	S	Standard Architecture
Device Type	10504	256K (64K x 4-bits) BiCMOS ECL-10K Static RAM
	100504	256K (64K x 4-bits) BiCMOS ECL-100K Static RAM
	101504	256K (64K x 4-bits) BiCMOS ECL-101K Static RAM

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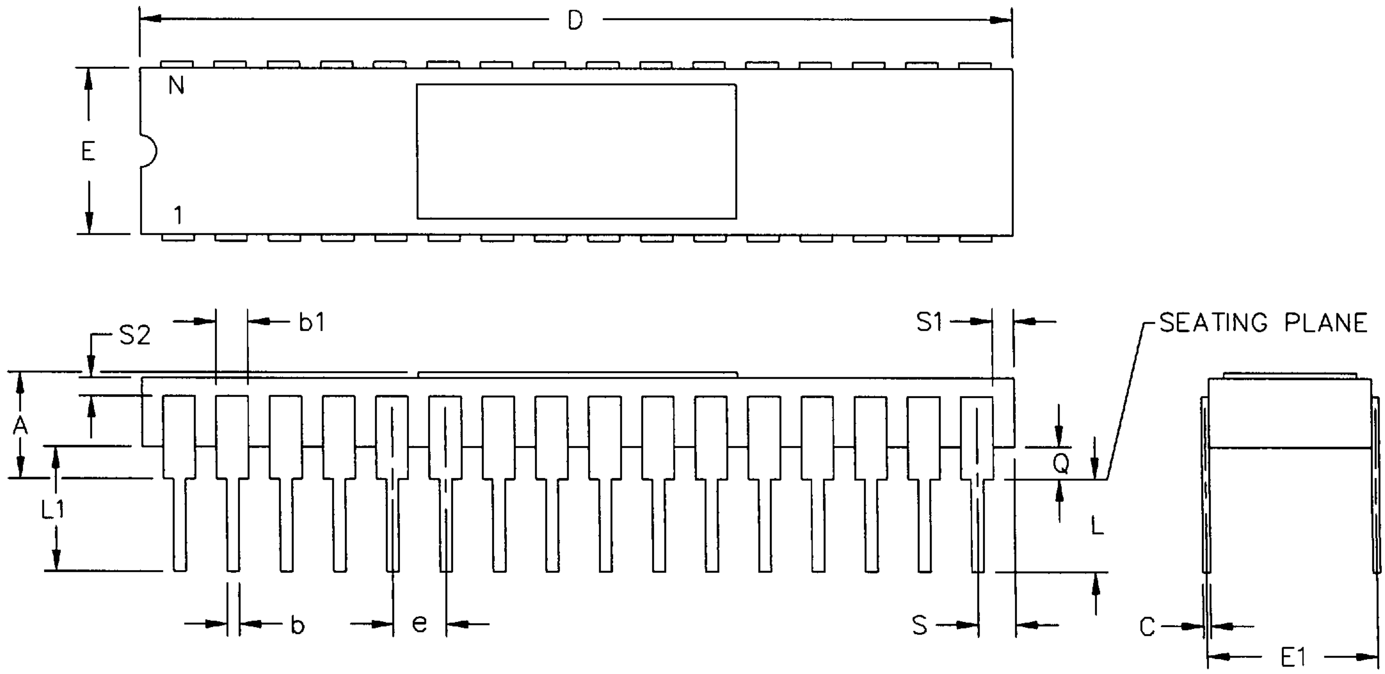
NOTE:
1. Please contact your IDT Sales Representative for more information on specifications and availability of Die products.

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054-3090 Telephone: (408) 727-6116 FAX 408-492-8674

SIDEBRAZE (Continued)

REV	DCN	DESCRIPTION	DATE	APPROVED
01	17566	UPDATED TO STANDARDIZE DWG	4/2/90	D Guilhamet
02	22236	CHANGED b1 MIN DIM		



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	C32-2	
SYMBOL	MIN	MAX
A	.090	.200
b	.014	.023
b1	.045	.060
C	.008	.014
D	1.580	1.640
E	.380	.410
E1	.390	.420
e	.100 BSC	
L	.100	.175
L1	.150	–
N	32	
Q	.030	.060
S	.030	.065
S1	.005	–
S2	.005	–

	CONFIGURATION	EXCEPTIONS
MIL-M-38510	NOT LISTED	
JEDEC	NOT REGISTERED	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC ± – DEC ± – ANGLES ± –

APPROVALS	DATE
DRAWN A.A	03/90
CHECKED	

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727-6116 FAX: (408) 727-2328

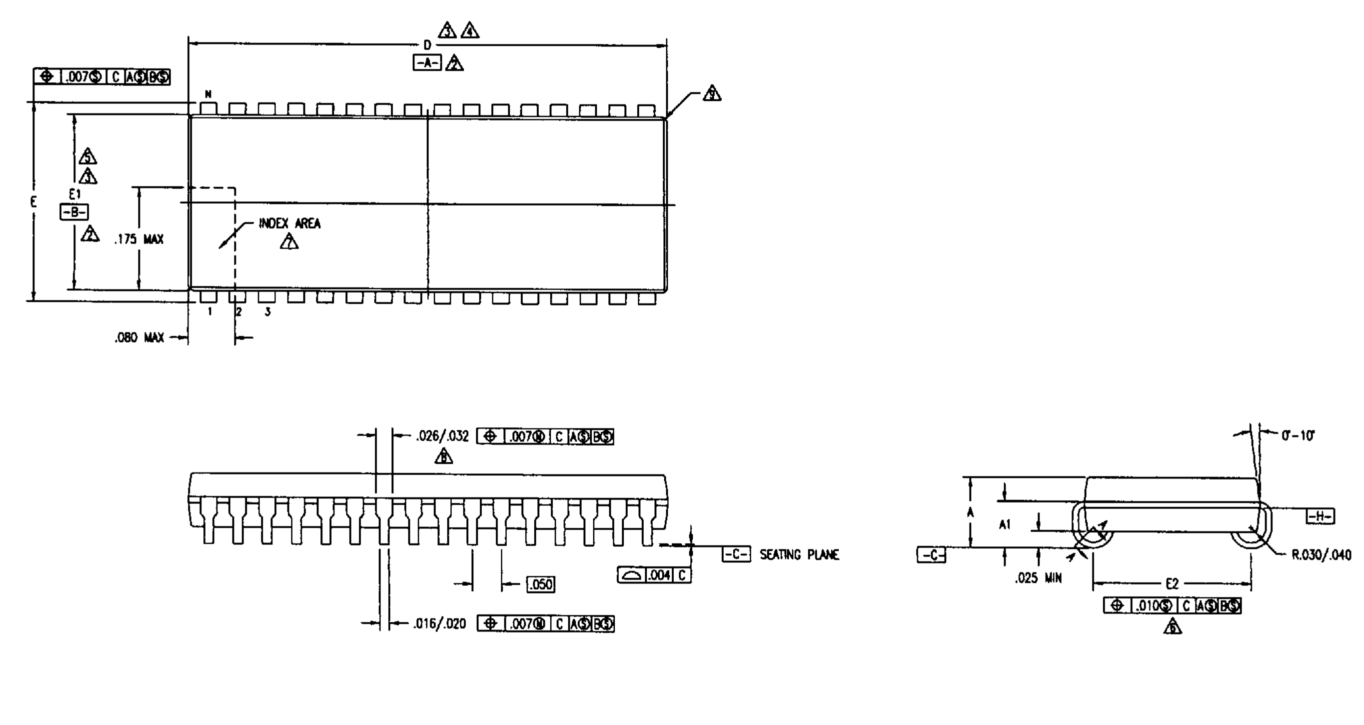
32 LD SIDE BRAZE (400 MIL) MKT DWG

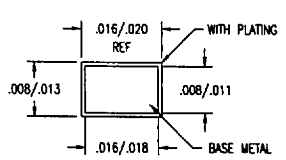
SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC-2080	02

DO NOT SCALE DRAWING — SHEET 38

SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27655	00	MOVE FROM PSC-4024 REDRAW TO JEDEC FORMAT	03/15/95	





SECTION A–A

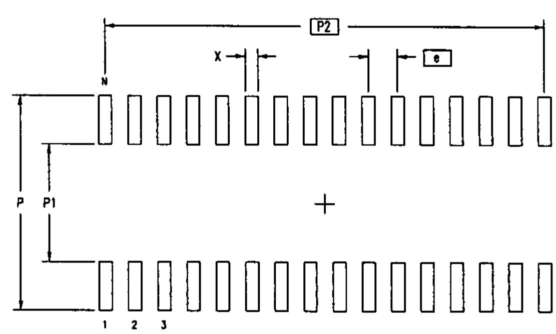
TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS	DATE	TITLE PJ 32 PACKAGE OUTLINE .300" BODY WIDTH SOJ .050" PITCH	
DRAWN JU	03/15/95		
CHECKED			
		SIZE C DRAWING No. PSC-4047	REV 00
		DO NOT SCALE DRAWING	

SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27655	00	MOVE FROM PSC-4024 REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	S032-2			
SYMBOL	JEDEC VARIATION			NOTE
	AC			
	MIN	NOM	MAX	
A	.130	.139	.148	
A1	.082	.088	.095	
D	.820	.825	.830	3,4
E	.330	.335	.340	
E1	.295	.300	.305	3,5
E2	.260	.267	.275	6
N	32			

LAND PATTERN DIMENSIONS



	MIN	MAX
P	.362	.370
P1	.196	.204
P2	.750 BSC	
X	.018	.026
e	.050 BSC	
N	32	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

4 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

5 DIMENSION E1 DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E2 TO BE DETERMINED AT SEATING PLANE -C- CONTACT POINT

7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .005 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION

9 EXACT SHAPE OF EACH CORNER IS OPTIONAL

10 ALL DIMENSIONS ARE IN INCHES

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-077, VARIATION AC. EXCEPTIONS: JEDEC MAXIMUM PLATED & BASE METAL FRAME THICKNESS ARE .010 & .009 RESPECTIVELY

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
DECIMAL XX± XXX± XXXX±	ANGULAR ±			
APPROVALS	DATE	TITLE PJ 32 PACKAGE OUTLINE .300" BODY WIDTH SOJ .050" PITCH		
DRAWN JV	03/15/95			
CHECKED				
		SIZE C	DRAWING No. PSC-4047	REV 00
		DO NOT SCALE DRAWING		