CMOS 4-BIT HIGH-SPEED MICROPROCESSOR SLICE

KEY FEATURES

- **2901 Architecture in CMOS**
- **Drop-In Replacement for 2901C**
- **Expandable in 4-Bit Increments**
- **DESC SMD No. 5962-88535**
- **High Speed**
  — Maximum Clock Frequency of 43 MHz (23 ns)
- **Very Low Power**
  — 30 mA Maximum (Commercial Temperature)
- **EPI Processing**
  — Latch-Up Immunity Over 200 mA

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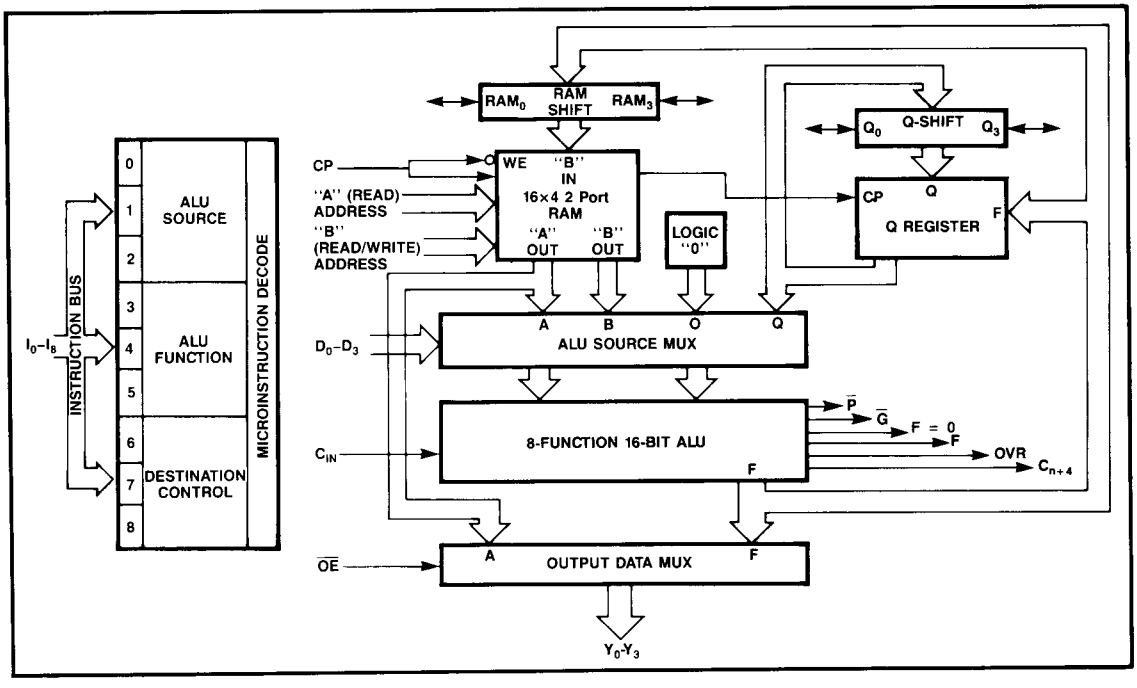
GENERAL DESCRIPTION

The WS5901 is a 4-bit high-speed microprocessor which contains the logic of a Bipolar 2901 bit slice processor.

This microprogrammable circuit has the flexibility to efficiently emulate almost any digital computing machine. It is an ideal candidate for such applications as peripheral controllers, CPUs, programmable microprocessors, and Digital Signal Processors.

The advanced CMOS process, with which the 5901 is manufactured, provides significant performance improvements over its counterpart. While operating as fast as a 2901C based system, the WS5901C requires less than 8% of the power consumed by its Bipolar equivalent. The WS5901D is a 25% speed enhancement over the "C" speed.

FUNCTIONAL BLOCK DIAGRAM

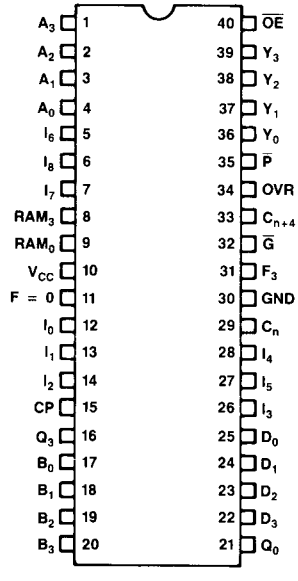


PIN DESCRIPTION

Signal Name	I/O	Description
A0-3	I	Addresses which select the word of on board RAM which is to be displayed through the A port.
B0-3	I	Addresses which select the word of on board RAM which is to be displayed through the B port and into which data is written when the clock is low.
I0-8	I	Block of three instruction groups which are to select 1) which data sources will be applied to the ALU (I012), 2) what function the ALU will perform (I345), and 3) what data is to be written into the Q register or on board RAM(I678).
Q3, RAM3	I/O	Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I678 indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the ALU output is available on the RAM 3 pin and the MSB of the Q-register is available on the Q3 pin. Otherwise, the pins appear as inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of RAM (octal 4 and 5) and the Q register (octal 4).
Qo, RAMo	I/O	Shift lines similar to Q3 and RAM3. However the description is applied to the LSB of RAM and the Q-register.
D0-D3	I	These four direct data inputs can be selected as a data source for the ALU. DO is the LSB.
Y0-Y3	O	These four three state outputs, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I678.
$\overline{OE}$	I	When high, the Y outputs are in the high impedance state. When low, either the contents of the A-register or the outputs of the ALU are displayed on Y0-Y3, as determined by I678.
$\overline{G}$, $\overline{P}$	O	The carry generate and propagate outputs of the ALU.
OVR	O	This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation.
F = 0	O	This output, when high, indicates the result of an ALU operation is zero.
F3	O	The most significant ALU output bit.
Cn	I	The carry-in to the ALU.
Cn + 4	O	The carry-out of the ALU.
CP	I	This clock signal is applied to the A and B-port latches, RAM, and Q-register. The clock low time is the write enable to the on-board 16 x 4 RAM, including set-up time for the A and B port registers. The A and B port and Q-register outputs change on the clock low-to-high transition.

PIN DESIGNATOR

Dual-In-Line Package



TOP

ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) . . . . . 0°C to +70°C
(Mil) . . . . . −55°C to +125°C
Storage Temp. (No Bias) . . . . . −65°C to +150°C
Voltage on Any Pin with
Respect to GND . . . . . −0.6V to +7V
Latch-Up Protection . . . . . >200 mA
ESD Protection . . . . . > ±2000V

***Notice:** Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

DC READ CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{OH}	Output High Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	All Outputs	I_{OH} = −3.4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	Y_0–Y_3	I_{OL} = 20 mA Comm'l		0.4	
			All Others	I_{OL} = 16 mA Mil			
V_{IH}	Input High Voltage	Guaranteed Input High Voltage			2.0		
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	
I_{IX}	Input Load Current	V_{CC} = Max, V_{IN} = Gnd or V_{CC}			−10	10	µA
I_{OZ}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}			−40	40	
I_{CC}	Power Supply Current	V_{CC} = Max (Note 2)	Comm'l (0°C to +70°C)			30	mA

NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C. 2) 100 ns System Cycle

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4}, and OVR

The four signals, G, P, C_{n+4} and OVR are designed to indicate carry and overflow conditions when the WS5901 is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Table 1.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$
$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$
$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$
$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R}_i$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S}_i$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0}+C_n$	$\overline{P_3P_2P_1P_0}+C_n$
4	R ∧ S	LOW	$\overline{G_3+G_2+G_1+G_0}$	$G_3+G_2+G_1+G_0+C_n$	$G_3+G_2+G_1+G_0+C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R}_i$ for R_i in definitions →		
6	R ∀ S	← Same as $\overline{R \forall S}$ equations, but substitute $\overline{R}_i$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3+G_2+G_1+G_0$	$P_3G_2+P_3P_2G_1+P_3P_2P_1G_0$	$\overline{G_3+P_3G_2+P_3P_2G_1+P_3P_2P_1P_0(G_0+\overline{C_n})}$	See note 1

NOTES: 1) $(P_2 + G_2P_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n) \forall (\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n)$
2) + = OR

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Table 1 : ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EXOR	R ▽ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \triangledown S}$

Table 2. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_3	Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care.
B = Register Addressed by B inputs.
DOWN is toward LSB. UP is toward MSB.

Table 3. ALU Destination Control.

		I_{210} (Octal Code)							
		0	1	2	3	4	5	6	7
I_{543} (Octal Code)	ALU Function	ALU Source (R, S)							
		A, Q	A, B	O, Q	O, B	O, A	D, A	D, Q	D, O
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D + Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ▽ Q	A ▽ B	Q	B	A	D ▽ A	D ▽ Q	D
7	R EX-NOR S	$\overline{A \triangledown Q}$	$\overline{A \triangledown B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \triangledown A}$	$\overline{D \triangledown Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ▽ = EX-OR.

Table 4. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0, I1, and I2 instruction inputs. The ALU performs eight functions; three arithmetic and five logic. This function selection is controlled by the I3, I4, and I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operations which the WS5901 can perform and Table 6 shows the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (Cn = 0) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	$A \wedge Q$
4 1		$A \wedge B$
4 5		$D \wedge A$
4 6		$D \wedge Q$
3 0	OR	$A \vee Q$
3 1		$A \vee B$
3 5		$D \vee A$
3 6		$D \vee Q$
6 0	EX-OR	$A \triangledown Q$
6 1		$A \triangledown B$
6 5		$D \triangledown A$
6 6		$D \triangledown Q$
7 0	EX-NOR	$\overline{A \triangledown Q}$
7 1		$\overline{A \triangledown B}$
7 5		$\overline{D \triangledown A}$
7 6		$\overline{D \triangledown Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A} \wedge Q$
5 1		$\overline{A} \wedge B$
5 5		$\overline{D} \wedge A$
5 6		$\overline{D} \wedge Q$

Table 5. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
0 0	ADD	A + Q	ADD plus one	A + Q + 1
0 1		A + B		A + B + 1
0 5		D + A		D + A + 1
0 6		D + Q		D + Q + 1
0 2	PASS	Q	Increment	Q + 1
0 3		B		B + 1
0 4		A		A + 1
0 7		D		D + 1
1 2	Decrement	Q - 1	PASS	Q
1 3		B - 1		B
1 4		A - 1		A
2 7		D - 1		D
2 2	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
2 3		-B - 1		-B
2 4		-A - 1		-A
1 7		-D - 1		-D
1 0	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
1 1		B - A - 1		B - A
1 5		A - D - 1		A - D
1 6		Q - D - 1		Q - D
2 0		A - Q - 1		A - Q
2 1		A - B - 1		A - B
2 5		D - A - 1		D - A
2 6		D - Q - 1		D - Q

Table 6. ALU Arithmetic Mode Functions.

WS5901C COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901C over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	31 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	32 MHz
Minimum Clock Low Time	15 ns
Minimum Clock High Time	15 ns
Minimum Clock Period	31 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	23 ns
From $\overline{OE}$ High to output disable	23 ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

FROM INPUT \ TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	40	40	40	37	40	40	40	—	ns
D_0–D_3	30	30	30	30	38	30	30	—	
C_n	22	22	20	—	25	22	25	—	
I_{012}	35	35	35	37	37	35	35	—	
I_{345}	35	35	35	35	38	35	35	—	
I_{678}	25	—	—	—	—	—	26	26	
A BYPASS ALU (I = 2XX)	35	—	—	—	—	—	—	—	
CLOCK	35	35	35	35	35	35	35	28	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

CP INPUT	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	15	1 (Note 3)	30 (Note 4)	1	ns
B Destination Address	15	DO NOT CHANGE (Note 2)		1	
D_0–D_3	—	—	25	0	
C_n	—	—	20	0	
I_{012}	—	—	30	0	
I_{345}	—	—	30	0	
I_{678}	10	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	—	—	12	0	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H>L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H>L included here.

WS5901CYM MILITARY RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901C over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	32 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	31 MHz
Minimum Clock Low Time	17 ns
Minimum Clock High Time	15 ns
Minimum Clock Period	32 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	25 ns
From $\overline{OE}$ High to output disable	25 ns

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COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

FROM INPUT \ TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	48	48	48	44	48	48	48	—	ns
D_0–D_3	37	37	37	34	40	37	37	—	
C_n	25	25	21	—	28	25	28	—	
I_{012}	40	40	40	44	44	40	40	—	
I_{345}	40	40	40	40	40	40	40	—	
I_{678}	29	—	—	—	—	—	29	29	
A BYPASS ALU (I = 2XX)	40	—	—	—	—	—	—	—	
CLOCK	40	40	40	40	40	40	40	33	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

CP \ INPUT	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	15	1 (Note 3)	32 (Note 4)	2	ns
B Destination Address	15	DO NOT CHANGE (Note 2)		2	
D_0–D_3	—	—	25	0	
C_n	—	—	20	0	
I_{012}	—	—	30	0	
I_{345}	—	—	30	0	
I_{678}	10	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	—	—	12	0	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H>L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H>L included here.

WS5901D COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901D over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	23 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	43 MHz
Minimum Clock Low Time	11 ns
Minimum Clock High Time	11 ns
Minimum Clock Period	23 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	14 ns
From $\overline{OE}$ High to output disable	16 ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

FROM INPUT \ TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	30	30	30	28	30	30	30	—	ns
D_0–D_3	21	20	20	20	24	21	22	—	
C_n	17	17	14	—	19	16	18	—	
I_{012}	26	25	24	24	25	24	25	—	
I_{345}	26	24	24	24	26	24	26	—	
I_{678}	16	—	—	—	—	—	21	21	
A BYPASS ALU (I = 2XX)	24	—	—	—	—	—	—	—	
CLOCK	24	23	23	23	24	24	24	19	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

CP \ INPUT	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	10	0 (Note 3)	21 (Note 4)	1	ns
B Destination Address	10	DO NOT CHANGE (Note 2)		1	
D_0–D_3	—	—	16	0	
C_n	—	—	13	0	
I_{012}	—	—	19	0	
I_{345}	—	—	19	0	
I_{678}	7	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	—	—	9	1	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H>L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H>L included here.

WS5901DYM MILITARY RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS5901D over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	27 ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	37 MHz
Minimum Clock Low Time	15 ns
Minimum Clock High Time	12 ns
Minimum Clock Period	27 ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5 pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	16 ns
From $\overline{OE}$ High to output disable	18 ns

2

COMBINATIONAL PROPAGATION DELAYS (C_L = 50 pF)

FROM INPUT \ TO OUTPUT	Y	F3	C_{n+4}	$\overline{G}$, $\overline{P}$	F = 0	OVR	RAM0, RAM3	Q0, Q3	UNITS
A, B ADDRESS	33	33	33	33	33	33	33	—	ns
D_0–D_3	24	23	23	21	25	24	25	—	
C_n	18	17	14	—	19	17	19	—	
I_{012}	28	27	26	28	29	27	27	—	
I_{345}	27	27	26	26	27	26	27	—	
I_{678}	18	—	—	—	—	—	21	21	
A BYPASS ALU (I = 2XX)	26	—	—	—	—	—	—	—	
CLOCK	27	26	26	25	27	26	27	20	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

CP \ INPUT	Set Up before H → L	Hold after H → L	Set Up before L → H	Hold after L → H	UNITS
A, B Source Address	12	0 (Note 3)	25 (Note 4)	2	ns
B Destination Address	12	DO NOT CHANGE (Note 2)		2	
D_0–D_3	—	—	16	0	
C_n	—	—	13	0	
I_{012}	—	—	19	0	
I_{345}	—	—	19	0	
I_{678}	9	DO NOT CHANGE (Note 2)		0	
RAM0, 3 and Q0, 3	—	—	9	0	

NOTES: 1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H>L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H>L included here.

ORDERING INFORMATION

PART NUMBER	SPEED (ns)	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS5901CP	C	40 Pin Plastic DIP, 0.6"	P1	Comm'l	Standard
WS5901CY	C	40 Pin CERDIP, 0.6"	Y1	Comm'l	Standard
WS5901CYM	C	40 Pin CERDIP, 0.6"	Y1	Military	Standard
WS5901CYMB	C	40 Pin CERDIP, 0.6"	Y1	Military	MIL-STD-883C
WS5901DP	D	40 Pin Plastic DIP, 0.6"	P1	Comm'l	Standard
WS5901DY	D	40 Pin CERDIP, 0.6"	Y1	Comm'l	Standard
WS5901DYM	D	40 Pin CERDIP, 0.6"	Y1	Military	Standard
WS5901DYMB	D	40 Pin CERDIP, 0.6"	Y1	Military	MIL-STD-883C