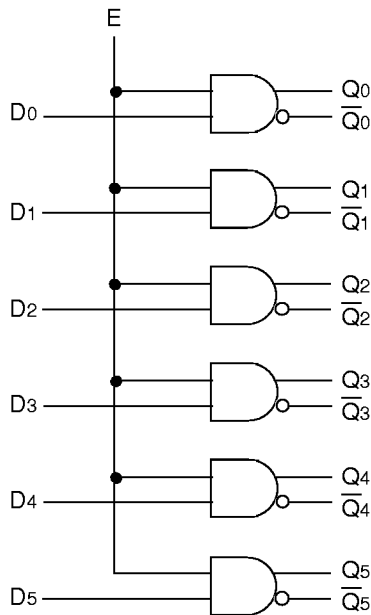


FEATURES

- Operates from a single +5V supply
- Differential PECL outputs
- Companion chip to SY100S390 PECL-to-TTL translator
- Function and pinout compatible with National and Signetics F100K
- ESD protection of 2000V
- Available in 24-pin CERDIP, 24-pin CERPACK and 28-pin PLCC packages

BLOCK DIAGRAM

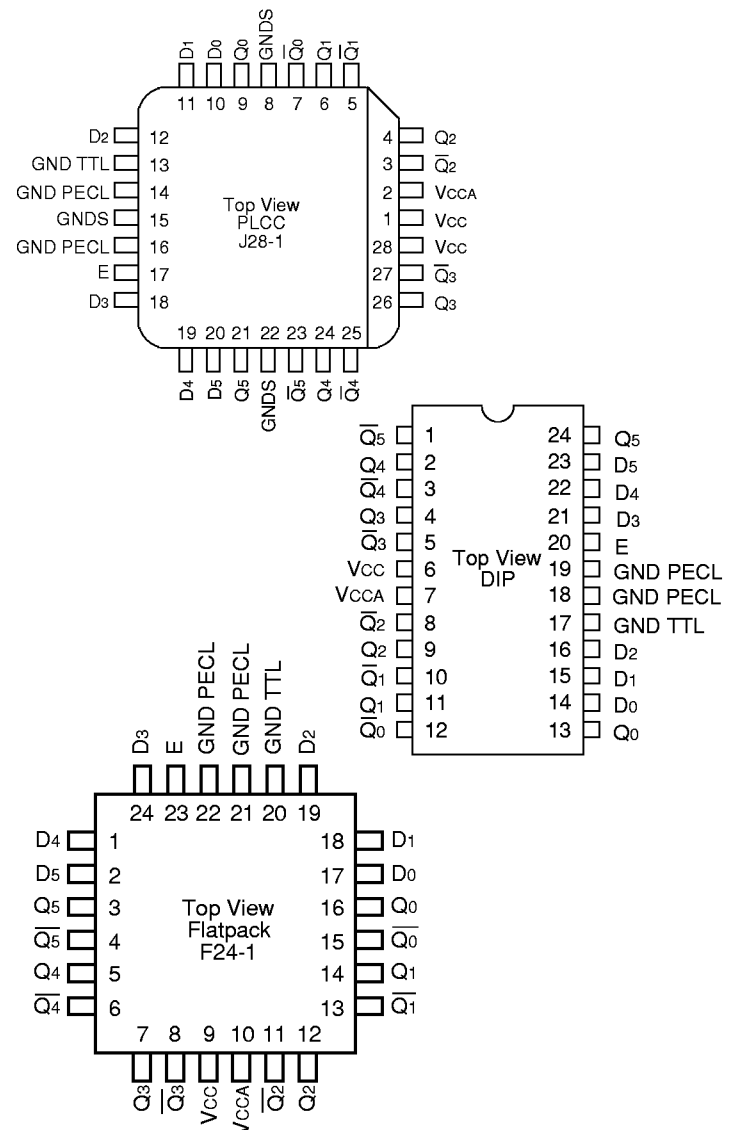


DESCRIPTION

The SY100S391 is a hex TTL-to-PECL translator for converting TTL logic levels to 100K logic levels. The unique feature of this translator is the ability to do this translation using only one +5V supply. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. A common enable (E), when LOW, holds all inverting outputs HIGH and all non-inverting inputs LOW.

The SY100S391 is ideal for those mixed PECL/TTL applications which only have a +5V supply available. When used in the differential mode, the S391, due to its high common mode rejection, overcomes voltage gradients between the TTL and PECL ground systems.

PIN CONFIGURATIONS



PIN NAMES

Pin	Function
D ₀ — D ₅	Data Inputs (TTL)
Q ₀ — Q ₅	Data Outputs (PECL)
\bar{Q}_0 — \bar{Q}_5	Inverting Data Outputs (PECL)
E	Enable Input (TTL)
V _{CCA}	V _{CCO} for ECL Outputs

TRUTH TABLE

Inputs		Outputs	
D _n	E	Q _n	\bar{Q}_n
H	H	H	L
L	H	L	H
H	L	L	H
L	L	L	H

NOTE:

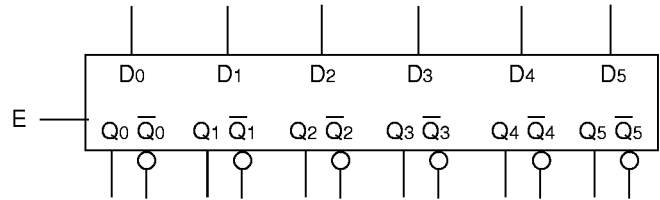
1. H = High Voltage Level, L = Low Voltage Level

GUARANTEED OPERATING CONDITIONS⁽¹⁾

Symbol	Rating	Value	Unit
T _A	Operating Temperature Commercial	0 to +85	°C
V _{CC}	Supply Voltage	+4.5 to +5.5	V

NOTE:

1. Do not exceed.

LOGIC SYMBOL

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
—	TTL Input Voltage ⁽²⁾	-0.5 to +7.0	V
—	TTL Input Current ⁽²⁾	-30 to +5.0	V
—	PECL Output Current (DC Output HIGH)	-50	V
—	V _{CC} Pin Potential to Ground Pin	-0.5 to +7.0	V
T _{store}	Storage Temperature	-65 to +150	°C
T _J	Max. Junction Temp. Ceramic Plastic	+175 +150	°C

NOTE:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.
2. Either voltage limit or current limit is sufficient to protect inputs.

TTL-TO-PECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

 V_{CC} = +5.0V ± 10%; GND = 0V

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V _{OH}	Output HIGH Voltage	V _{CC} -1025	V _{CC} -955	V _{CC} -870	mV	V _{IN} = V _{IH} (Max.) or V _{IL} (Min.) Loading with 50Ω to V _{CC} -2V
V _{OL}	Output LOW Voltage	V _{CC} -1890	V _{CC} -1705	V _{CC} -1620		
V _{OHc}	Output HIGH Voltage Corner Point High	V _{CC} -1035	—	—	mV	V _{IN} = V _{IH} (Min.) or V _{IL} (Max.) Loading with 50Ω to V _{CC} -2V
V _{OLc}	Output LOW Voltage Corner Point Low	—	—	V _{CC} -1610	mV	
V _{IH}	Input HIGH Voltage	2.0	—	5.0	V	Over V _{TTL} , V _{EE} , T _A Range
V _{IL}	Input LOW Voltage	0	—	0.8	V	Over V _{TTL} , V _{EE} , T _A Range
I _{IH}	Input HIGH Current	—	—	10	μA	V _{IN} = +2.7V
	Breakdown Current	—	—	100	μA	V _{IN} = +5.5V, V _{CC} = Max.
I _{IL}	Input LOW Current	D _n E	—	-0.8 -4.2	mA	V _{IN} = +0.5V
V _{CD}	Input Clamp Diode Voltage	—	—	-1.2	V	I _{IN} = -18mA
I _{CC}	V _{CC} Supply Current	25	—	69	mA	Inputs Open

NOTE:

1. The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

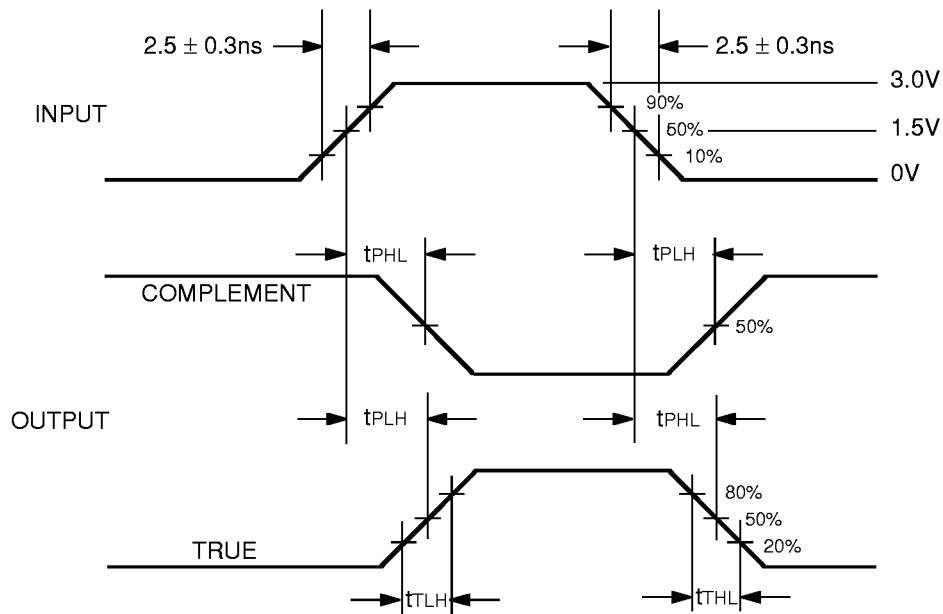
AC ELECTRICAL CHARACTERISTICS

CERDIP, CERPACK AND PLCC

VCC = +5.0V ± 10%

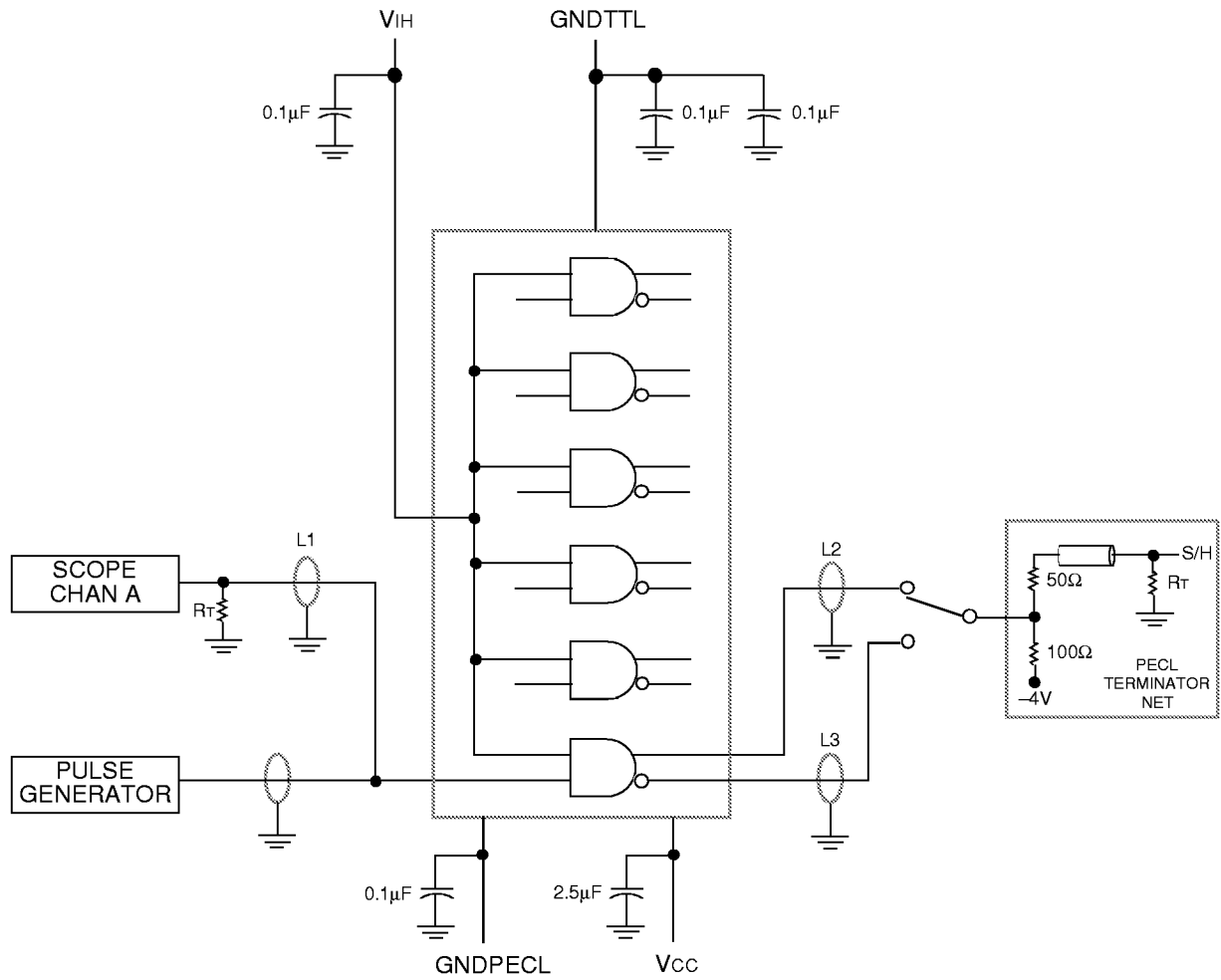
Symbol	Parameter	TA = 0°C		TA = +25°C		TA = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
tPLH tPHL	Propagation Delay Data and Enable to Output	400	1400	400	1400	400	1400	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	350	1700	350	1700	350	1700	ps	

TIMING DIAGRAM



Propagation Delay and Transition Times

TEST CIRCUIT



PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100S391DC	D24-1	Commercial
SY100S391FC	F24-1	Commercial
SY100S391JC	J28-1	Commercial
SY100S391JCTR	J28-1	Commercial

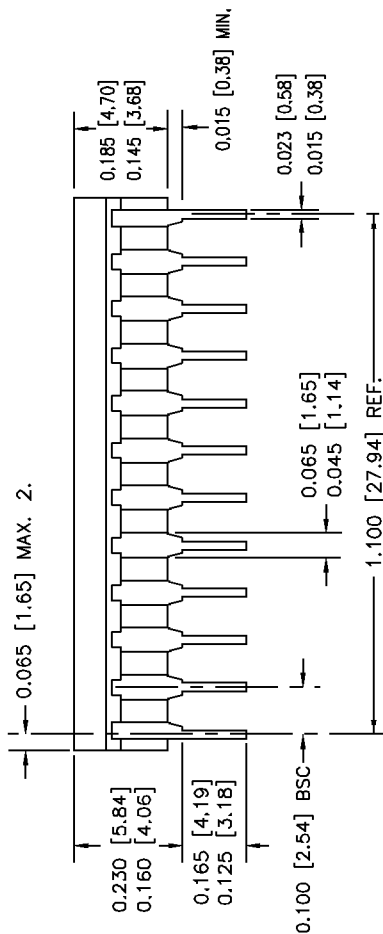
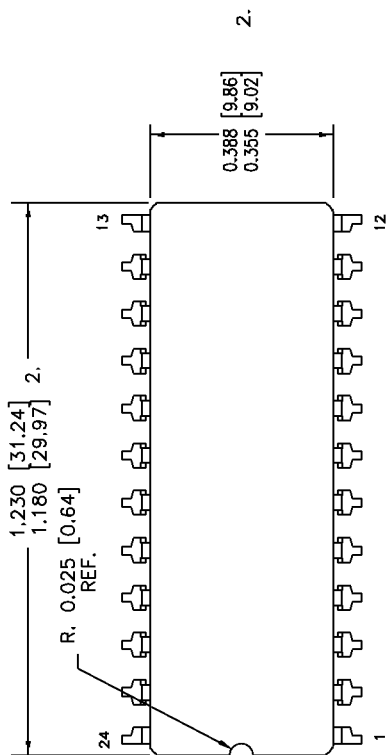
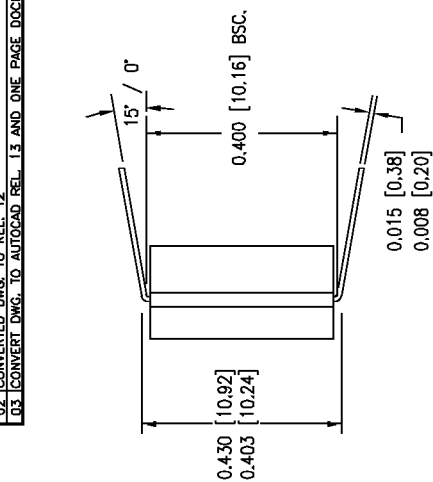
24 LEAD CERDIP (D24-1)

FILE/REV #: PD0003A03

PD/0003/ASCORP

PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT DWG. TO DESIGNER VERSION 4.0 FORMAT.	12/30/93
02	CONVERTED DWG. TO REL. 12	03/15/96
03	CONVERT DWG. TO AUTOCAD REL. 1.3 AND ONE PAGE DOCUMENT.	02/18/98



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.



3250 SCOTT BOULEVARD
SANTA CLARA CA 95054
TEL: 408-990-9191
FAX: 408-567-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	24 LEAD CERDIP (400" WIDE) PACKAGE OUTLINE
ORIGINATOR: FERMIN G. LURRITA	02/23/98	QUALITY: MARSHALL WILDER		A	
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					SCALE N/A
					REVISION 03

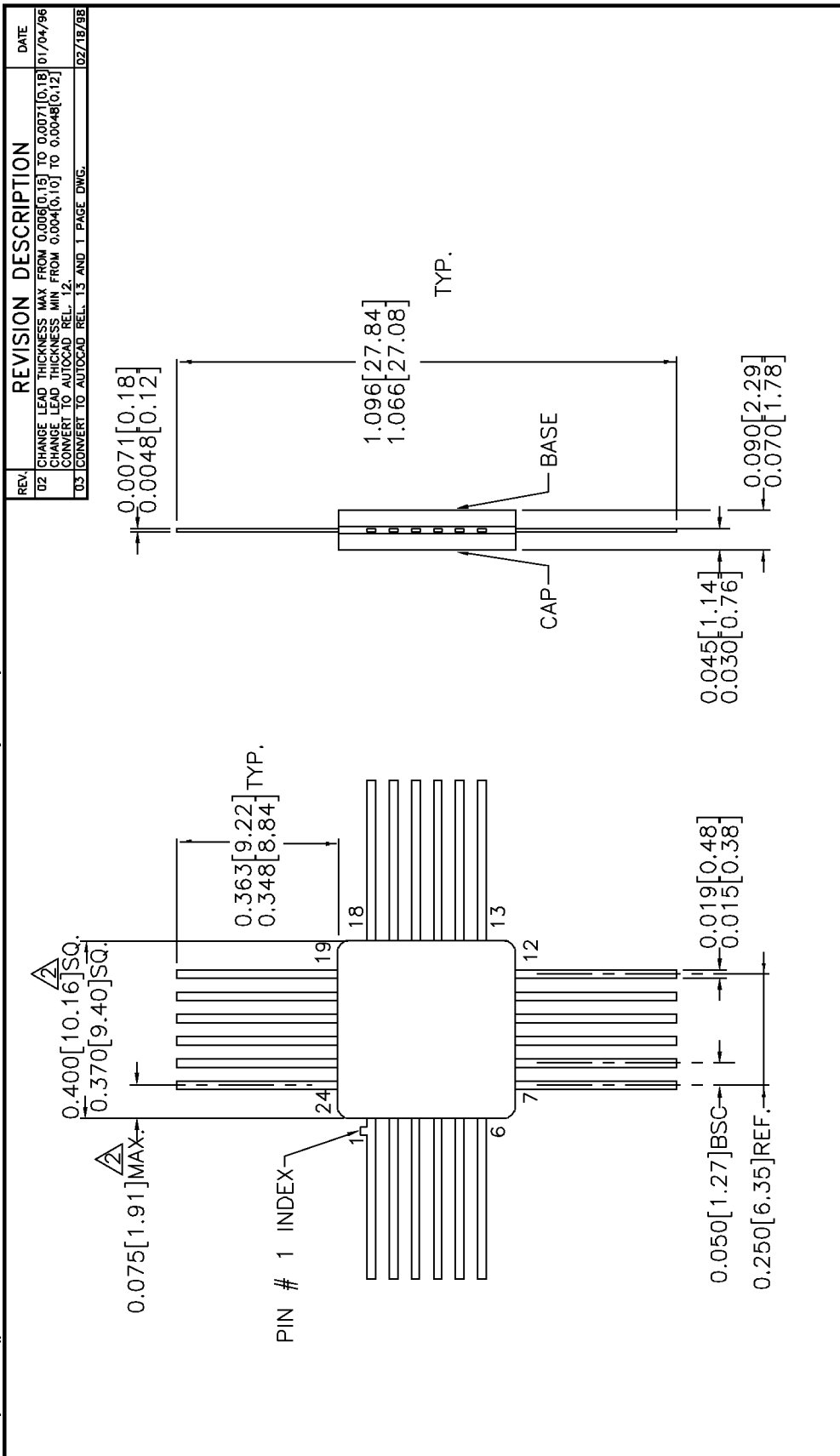
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24 LEAD CERPACK (F24-1)

FILE/REV #: PD0006A03

PD/0006/ASCORP

PAGE 1 OF 1



REV.	REVISION DESCRIPTION	DATE
02	CHANGE LEAD THICKNESS MAX FROM 0.006 [0.15] TO 0.0071 [0.18] CHANGE LEAD THICKNESS MIN FROM 0.004 [0.10] TO 0.0048 [0.12] (CONVERT TO AUTOCAD REL. 12)	01/04/96
03	CONVERT TO AUTOCAD REL. 13 AND 1 PAGE DWG.	02/18/98

SYNERGY
SEMICONDUCTOR

3250 SCOTT BOULEVARD
SANTA CLARA CA 95054
TEL: 408-980-9191
FAX: 408-587-7878

24 LEAD CERPACK
PACKAGE OUTLINE

APPROVALS	DATE	APPROVALS	DATE	SIZE
ORIGINATOR: FERNUN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO		
RELEASE DATE:				

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SCALE: N/A
REVISION: 03

- NOTES:
1. DIMENSIONS ARE IN INCHES [MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)

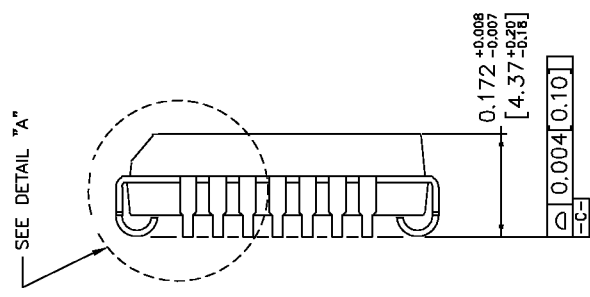
FILE/REV #: PD0008A03

PD/0008/ASCORP

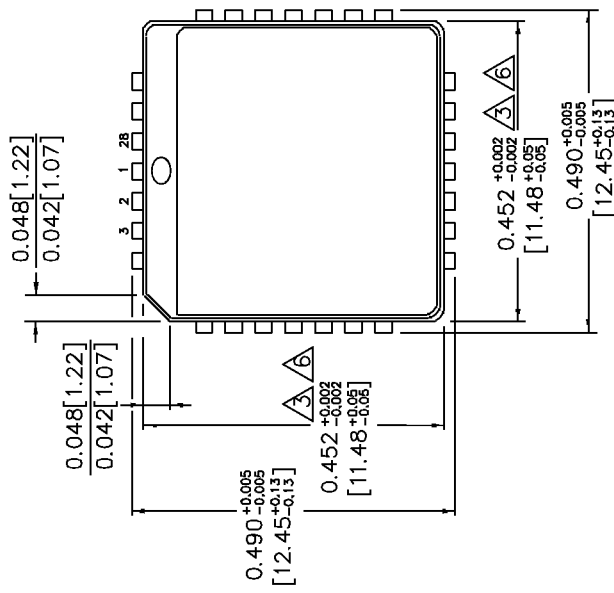
PAGE 1 OF 1

REV.	REVISION DESCRIPTION	DATE
01	CONVERT TO DESIGNER VERSION A.D. FORMAT AND COVER PAGE TO SPEC. CHANGE BODY WIDTH DIMENSION FROM 0.450[11.43] TO 0.443[11.25] TYP. GEOMETRICAL ERROR.	08/18/94
02	CONVERT DWG FROM DESIGNER TO AUTOCAD REL. 12. REFERENCE AMKOR DWG. NO. 34653 REV. 00.	02/22/96
03	CONVERT DWG TO REL. 15 AND ONE PAGE DOCUMENT.	02/18/98

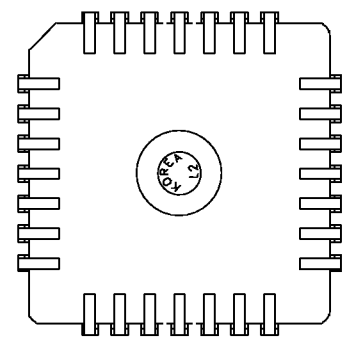
SIDE VIEW



TOP VIEW

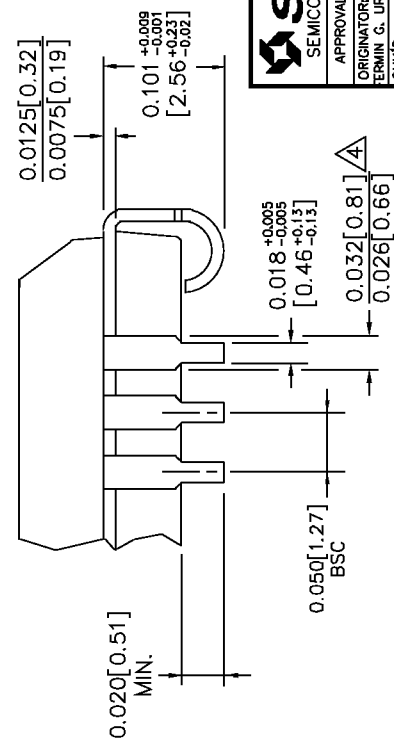


BOTTOM VIEW



NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203].
4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



DETAIL "A"

SYNERGY
SEMICONDUCTOR

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SANTA CLARA, CA. 95054
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FAX: 408-367-7878

APPROVALS	DATE	APPROVALS	DATE	SIZE	28 LEAD PLCC
ORIGINATOR: ERMIN G. URRUTIA	02/23/98	QUALITY: MARSHALL WILDER		A	PACKAGE OUTLINE
CHK'D: WON CHANG		DOCUMENT CONTROL: BRIAN SANFILIPPO			
RELEASE DATE:					

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SCALE: N/A
REVISION: 03