ML610471/472/473/Q471/Q472/Q473

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

This LSI is a high performance CMOS 8-bit microcontroller equipped with an 8-bit CPU nX-U8/100 and integrated with peripheral functions such as the UART, RC oscillation type A/D converter, and LCD driver.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipe line architecture parallel processing. Additionally, it adopts the low-/high-speed dual clock system, standby mode, and process that prohibits leak current at high temperatures, and is most suitable for battery-driven applications.
MTP version (ML610Q471/ML610Q472/ML610Q473) can rewrite programs on-board, which can contribute to reduction in product development TAT. The flash memory incorporated into this MTP version implements the mask ROM-equivalent low-voltage operation (1.25V or higher) and low-power consumption (typically 5uA at low-speed operation), enabling volume production by the MTP version.
For industrial use, ML610471P/ML610472P/ML610473P/ML610Q471P/ML610Q472P/ML610Q473P with the extended operating ambient temperature ranging from -40°C to 85°C are available.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit length instruction
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Flash Memory rewrite function (MTP version only)
  - Minimum instruction execution time
    30.5 μs (@ 32.768 kHz system clock)
    2 μs (@ 500 kHz system clock)

- Internal memory
  - ML610471/ML610472/ML610473
    Internal 8KByte Mask ROM (4K x 16 bits) (including unusable 256Byte TEST area)
    Internal 512Byte RAM (512 x 8 bits)
  - ML610Q471/ML610Q472/ML610Q473
    Internal 8KByte Flash ROM (4K x 16 bits) (including unusable 256Byte TEST area)
    Internal 512Byte RAM (512 x 8 bits)

- Interrupt controller
  - 1 non-maskable interrupt source:
    Internal source: 1 (Watchdog Timer)
  - 12 maskable interrupt sources:
    Internal source: 8 (Timer 2, Timer 3, UART0, RC Oscillation type A/D converter, TBC128Hz, TBC32Hz, TBC16Hz, TBC2Hz)
    External source: 4 (P00, P01, P02, P03)

- Time base counter
  - Low-speed time base counter x 1 channel
    Frequency compensation (Compensation range: Approx. -488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter x 1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s)

- Timers
  - 8 bits x 2 channels [also available is 16-bit configuration (using Timers 2 and 3) x 1 channels]
  - Clock frequency measurement function mode (16-bit configuration using Timers 2 and 3 x 1 channel only)

- Capture
  - Time base capture x 2 channels (4096 Hz to 32 Hz)

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- RC oscillation type A/D converter
  - 16-bit counter
  - Time division x 1 channels

- General-purpose ports
  - Input-only port: 4 channels (including secondary functions)
  - Output-only port
    ML610471/ML610Q471: 10 channels (including secondary functions)
    ML610472/ML610Q472: 6 channels (including secondary functions)
    ML610473/ML610Q473: 2 channels (including secondary functions)
  - Input/output port: 7 channels (including secondary functions)

- LCD driver
  - Number of segments
    ML610471/ML610Q471:
    Up to 55 dots (select among 11 segments x 5 commons, 12 segments x 4 commons, 13 segments x 3 commons, and 14 segments x 2 commons)
    ML610472/ML610Q472:
    Up to 75 dots (select among 15 segments x 5 commons, 16 segments x 4 commons, 17 segments x 3 commons, and 18 segments x 2 commons)
    ML610473/ML610Q473:
    Up to 95 dots (select among 19 segments x 5 commons, 20 segments x 4 commons, 21 segments x 3 commons, and 22 segments x 2 commons)
  - 1/1 to 1/5 duty
  - 1/2 or 1/3 bias (built-in bias generation circuit)
  - Frame frequency selectable (approx. 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow

- Clock
  - Low-speed clock (Operation of this LSI is not guaranteed under a condition with no supply of low-speed crystal oscillation clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock
    Built-in RC oscillation (500 kHz)

- Power management
  - HALT mode: Suspends the instruction execution by CPU (peripheral circuits are in operating states)
  - STOP mode: Stops the low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - High-speed clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block control function: Completely stops the operation of any function block circuit that is not used (resets registers and stops clock)

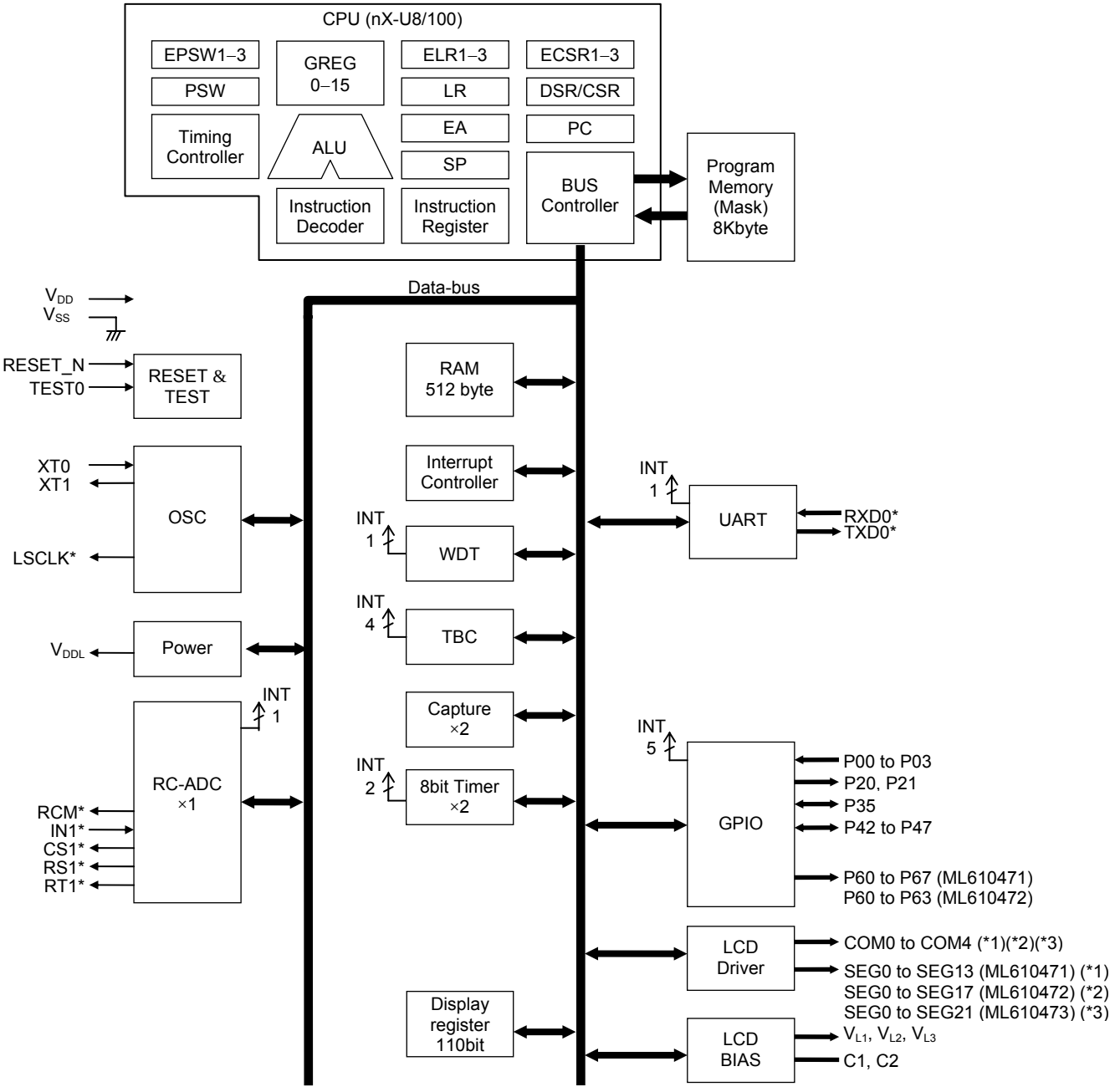
- Shipment
  – Chip (Die)
  ML610471-xxxWA / ML610Q471-xxxWA
  ML610472-xxxWA / ML610Q472-xxxWA
  ML610473-xxxWA / ML610Q473-xxxWA
  ML610471P-xxxWA / ML610Q471P-xxxWA
  ML610472P-xxxWA / ML610Q472P-xxxWA
  ML610473P-xxxWA / ML610Q473P-xxxWA
  – 48-pin plastic TQFP
  ML610471-xxxTPZ03A / ML610Q471-xxxTPZ03A
  ML610472-xxxTPZ03A / ML610Q472-xxxTPZ03A
  ML610473-xxxTPZ03A / ML610Q473-xxxTPZ03A
  ML610471P-xxxTPZ03A / ML610Q471P-xxxTPZ03A
  ML610472P-xxxTPZ03A / ML610Q472P-xxxTPZ03A
  ML610473P-xxxTPZ03A / ML610Q473P-xxxTPZ03A
  – 64-pin plastic TQFP
  ML610471-xxxTBZ03A / ML610Q471-xxxTBZ03A
  ML610472-xxxTBZ03A / ML610Q472-xxxTBZ03A
  ML610473-xxxTBZ03A / ML610Q473-xxxTBZ03A
  ML610471P-xxxTBZ03A / ML610Q471P-xxxTBZ03A
  ML610472P-xxxTBZ03A / ML610Q472P-xxxTBZ03A
  ML610473P-xxxTBZ03A / ML610Q473P-xxxTBZ03A

  xxx: ROM code number (xxx of the blank product is NNN, MTP version only)
  Q: MTP version
  P: Wide range temperature version (P version)
  WA: Chip (Die)
  TPZ03A: 48pin plastic TQFP
  TBZ03A: 64pin plastic TQFP

- Guaranteed Operation Range
  – Operating temperature: -20°C to +70°C (P version: -40°C to +85°C)
  – Operating voltage: V_{DD} = 1.25V to 3.6V

BLOCK DIAGRAM

ML610471/ML610472/ML610473



* Secondary function or Tertiary function

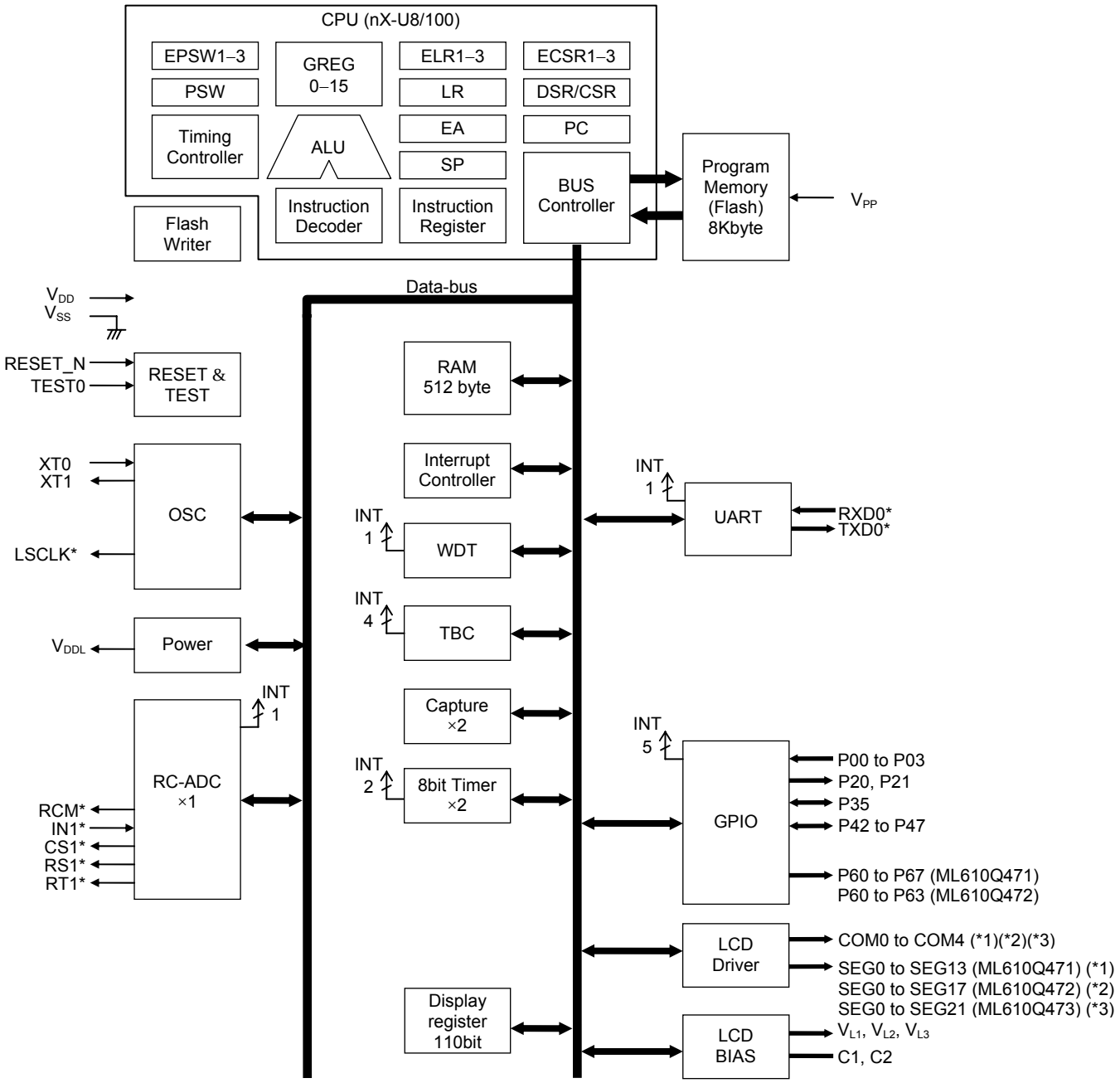
(*1) Select among 11 segments x 5 commons, 12 segments x 4 commons, 13 segments x 3 commons, and 14 segments x 2 commons with the register

(*2) Select among 15 segments x 5 commons, 16 segments x 4 commons, 17 segments x 3 commons, and 18 segments x 2 commons with the register

(*3) Select among 19 segments x 5 commons, 20 segments x 4 commons, 21 segments x 3 commons, and 22 segments x 2 commons with the register

Figure 1 ML610471/ML610472/ML610473 Block Diagram

ML610Q471/ML610Q472/ML610Q473

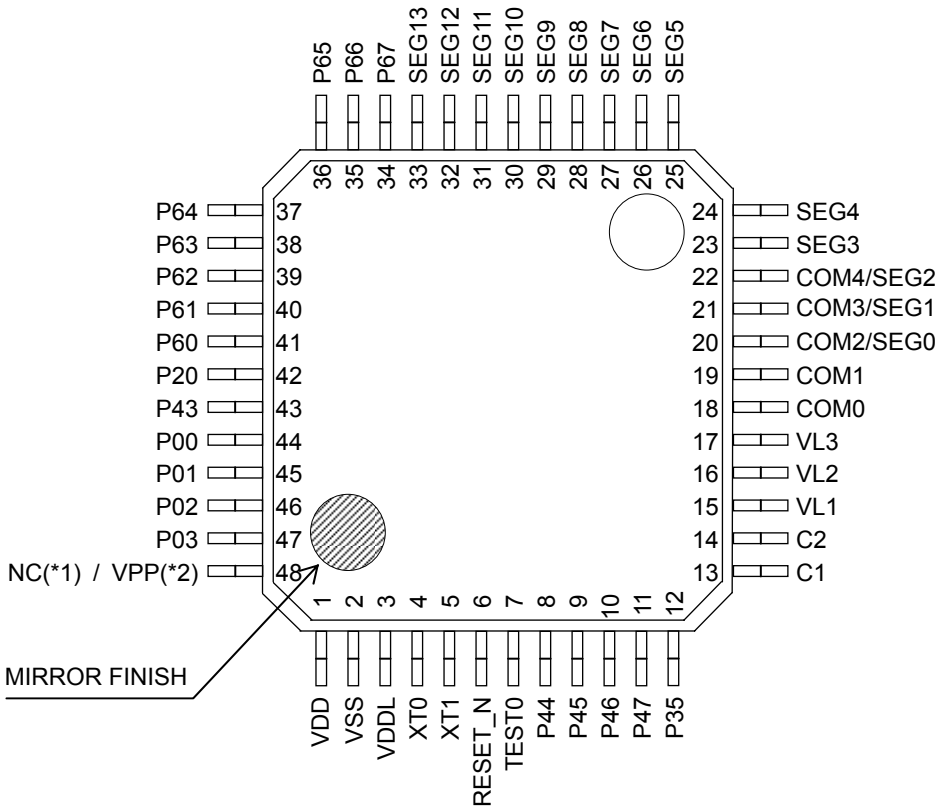


* Secondary function or Tertiary function
(*1) Select among 11 segments x 5 commons, 12 segments x 4 commons, 13 segments x 3 commons, and 14 segments x 2 commons with the register
(*2) Select among 15 segments x 5 commons, 16 segments x 4 commons, 17 segments x 3 commons, and 18 segments x 2 commons with the register
(*3) Select among 19 segments x 5 commons, 20 segments x 4 commons, 21 segments x 3 commons, and 22 segments x 2 commons with the register

Figure 2 ML610Q471/ML610Q472/ML610Q473 Block Diagram

PACKAGE PIN/CHIP PAD LAYOUT

ML610471/ML610Q471 48pin TQFP Package Pin Layout

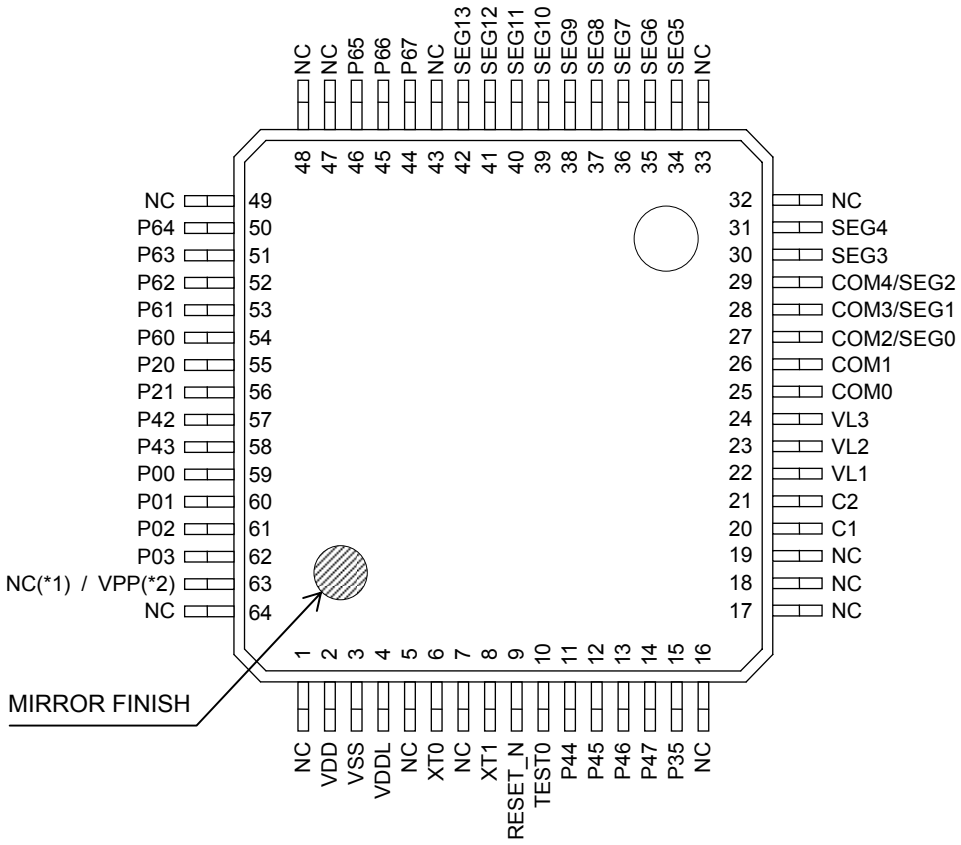


(NC): No Connection

(*1) : ML610471
(*2) : ML610Q471

Figure 3 ML610471/ML610Q471 48pin TQFP Package Pin Layout

ML610471/ML610Q471 64pin TQFP Package Pin Layout

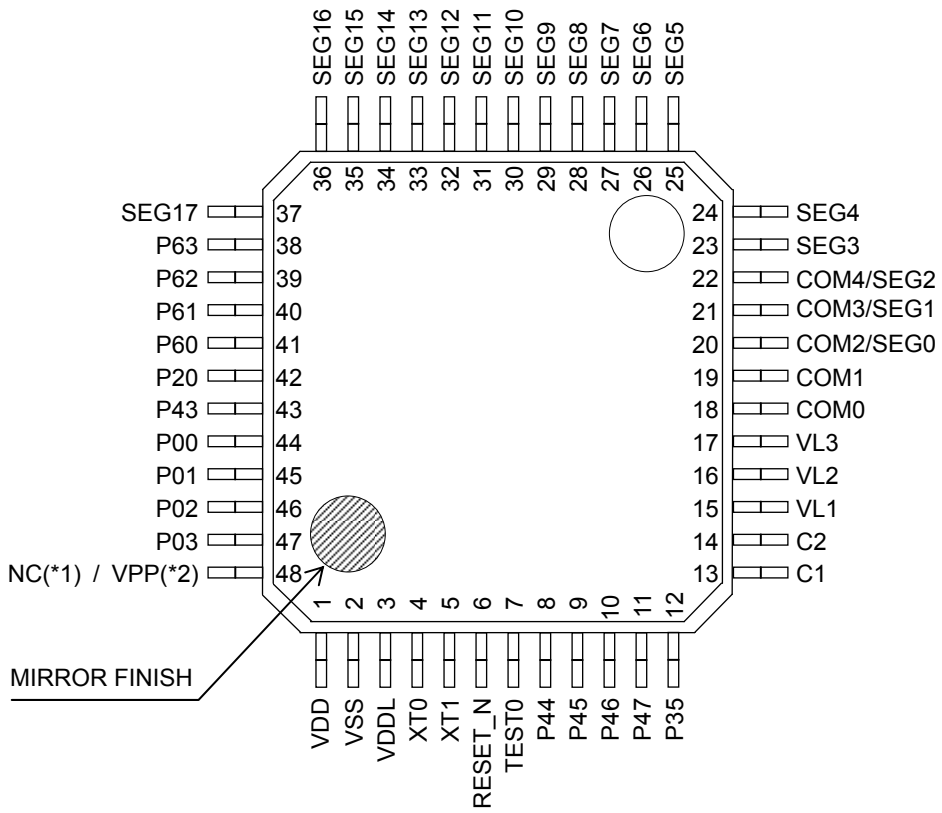


(NC): No Connection

(*1) : ML610471
(*2) : ML610Q471

Figure 4 ML610471/ML610Q471 64pin TQFP Package Pin Layout

ML610472/ML610Q472 48pin TQFP Pin Layout

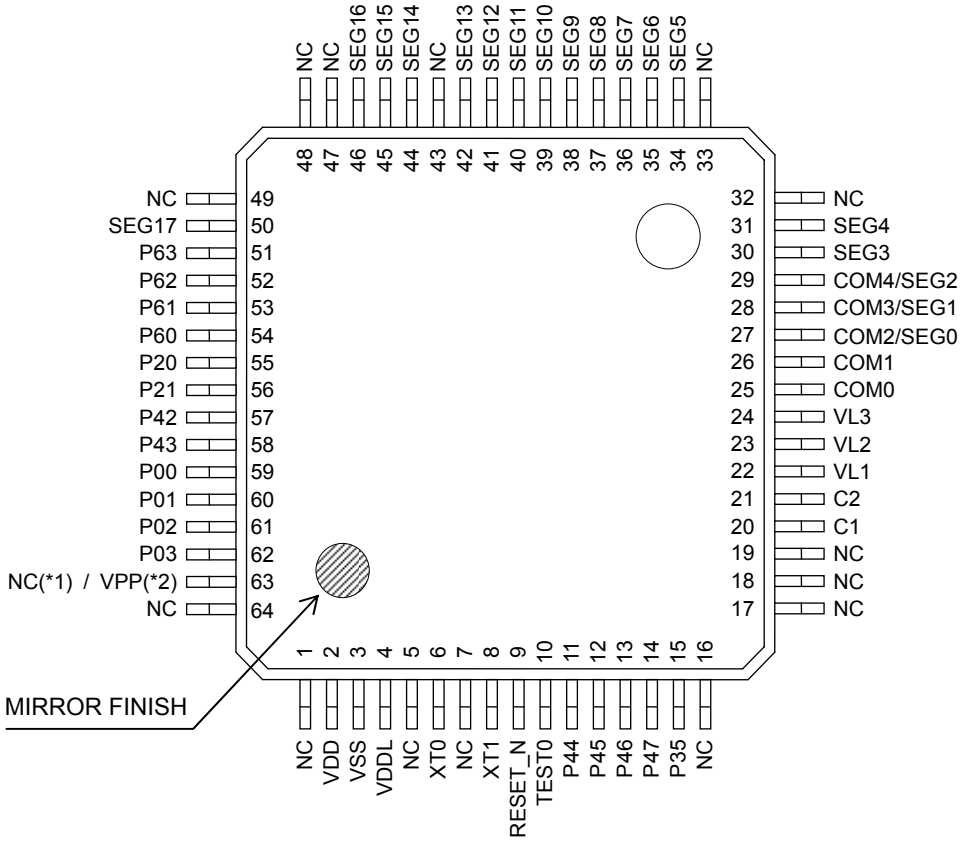


(NC): No Connection

(*1) : ML610472
(*2) : ML610Q472

Figure 5 ML610472/ML610Q472 48pin TQFP Package Pin Layout

ML610472/ML610Q472 64pin TQFP Pin Layout

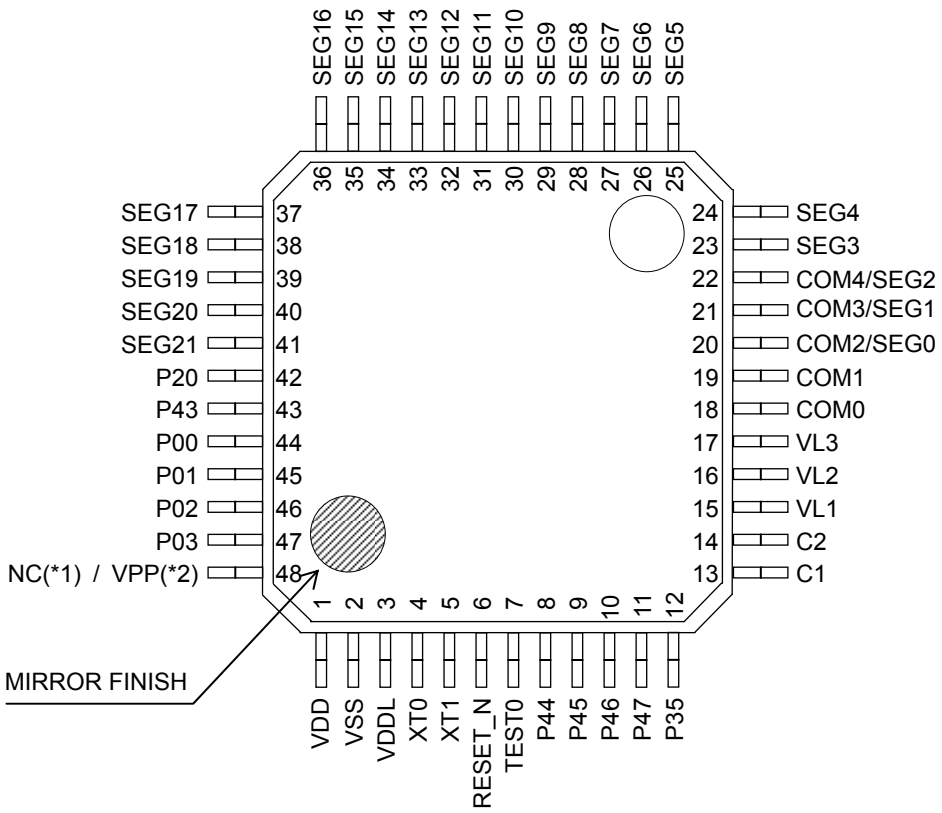


(NC): No Connection

(*1) : ML610472
(*2) : ML610Q472

Figure 6 ML610472/ML610Q472 64pin TQFP Package Pin Layout

ML610473/ML610Q473 48pin TQFP Pin Layout

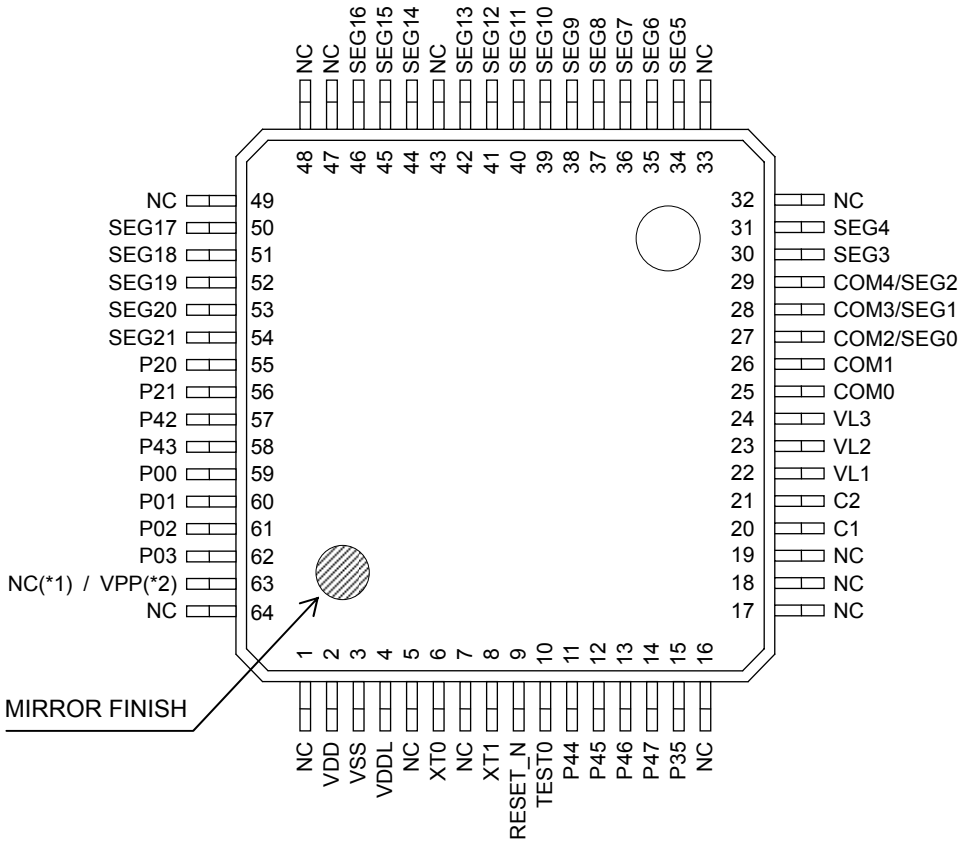


(NC): No Connection

(*1) : ML610473
(*2) : ML610Q473

Figure 7 ML610473/ML610Q473 48pin TQFP Package Pin Layout

ML610473/ML610Q473 64pin TQFP Pin Layout

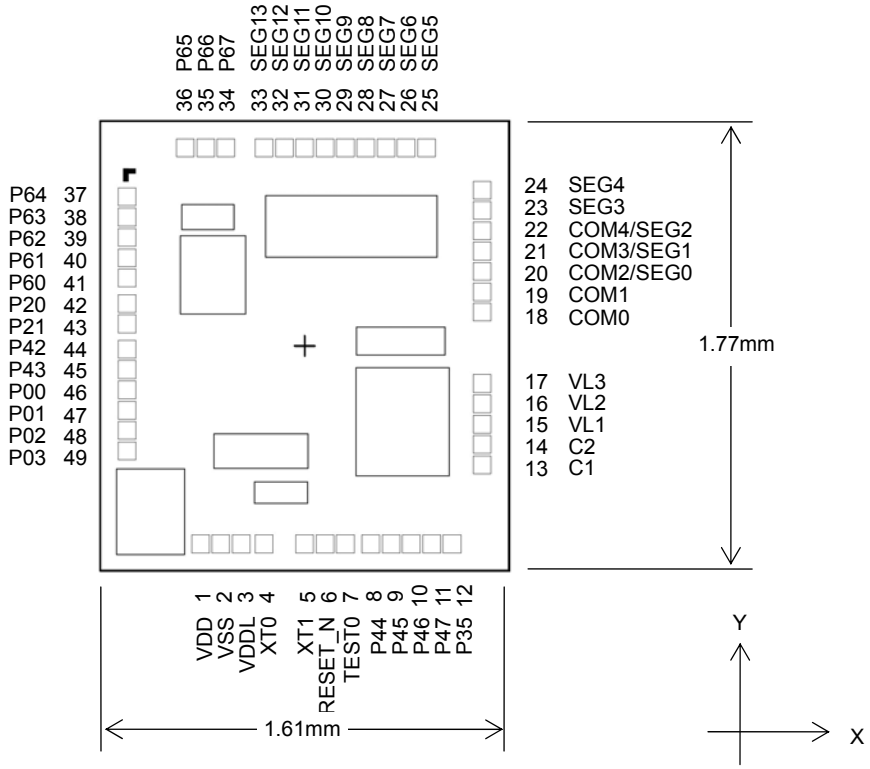


(NC): No Connection

(*1) : ML610473
(*2) : ML610Q473

Figure 8 ML610473/ML610Q473 64pin TQFP Package Pin Layout

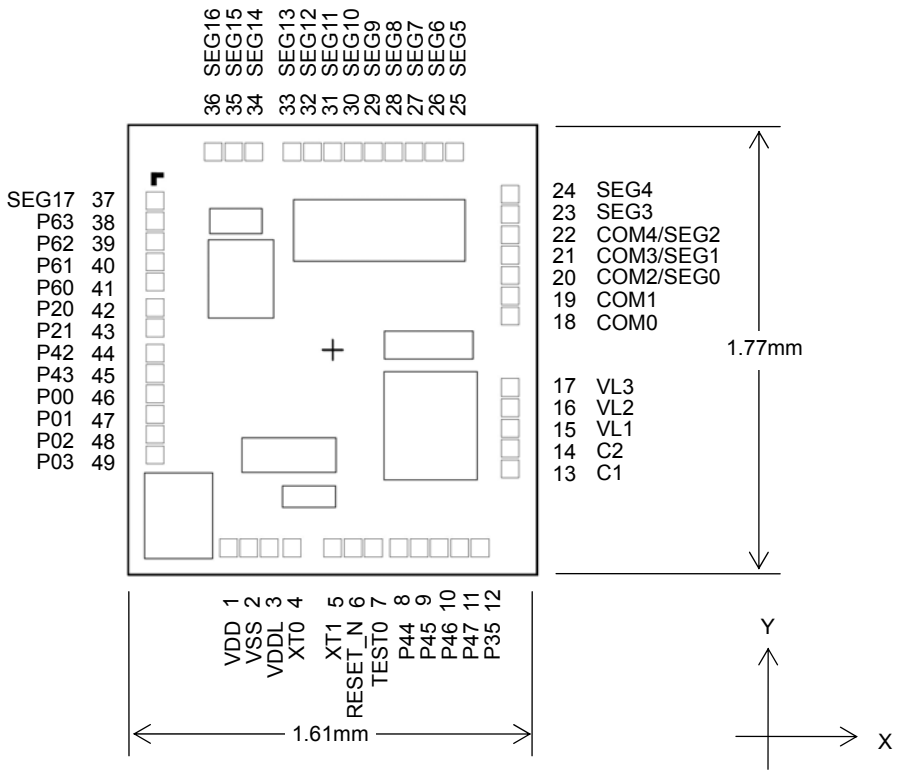
ML610471 Chip Pad Layout & Dimension



Chip size: 1.61 mm × 1.77 mm
PAD count: 49 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

Figure 9 ML610471 Chip Pin Layout & Dimension

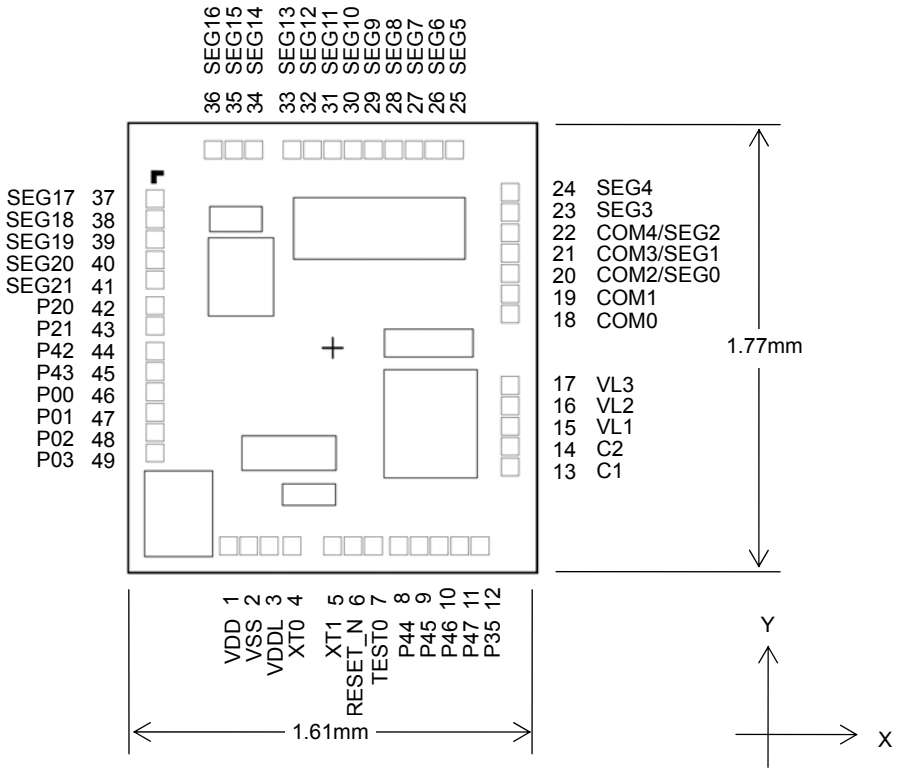
ML610472 Chip Pad Layout & Dimension



Chip size: 1.61 mm × 1.77 mm
PAD count: 49 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

Figure 10 ML610472 Chip Pin Layout & Dimension

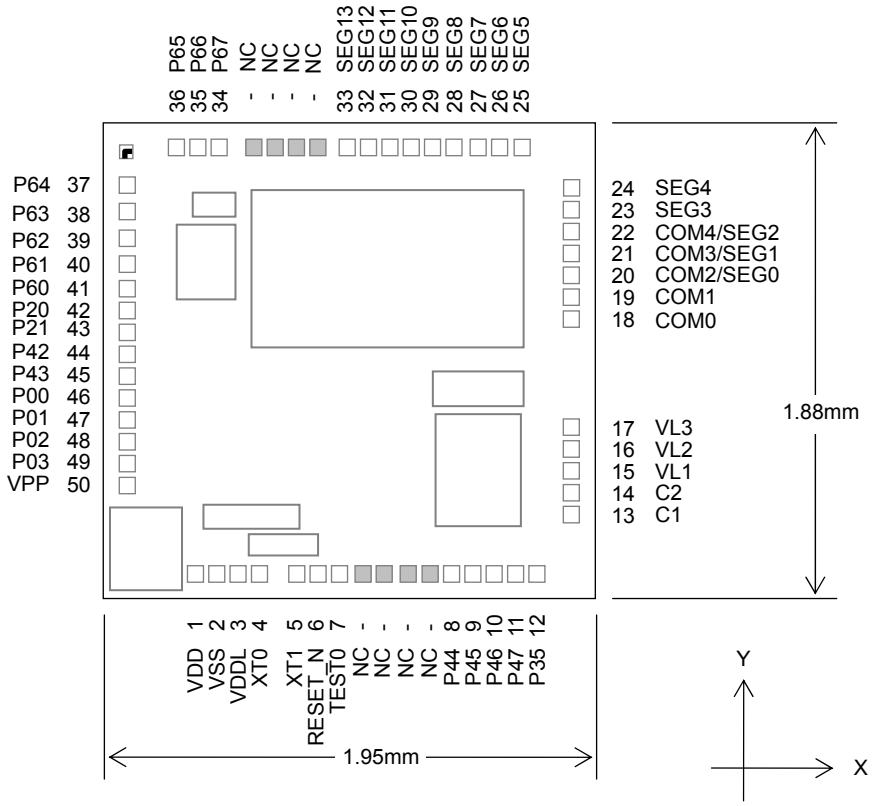
ML610473 Chip Pad Layout & Dimension



Chip size: 1.61 mm × 1.77 mm
PAD count: 49 pins
Minimum PAD pitch: 80 μm
PAD aperture: 70 μm×70 μm
Chip thickness: 350 μm
Voltage of the rear side of chip: V_{SS} level.

Figure 11 ML610473 Chip Pin Layout & Dimension

ML610Q471 Chip Pad Layout & Dimension

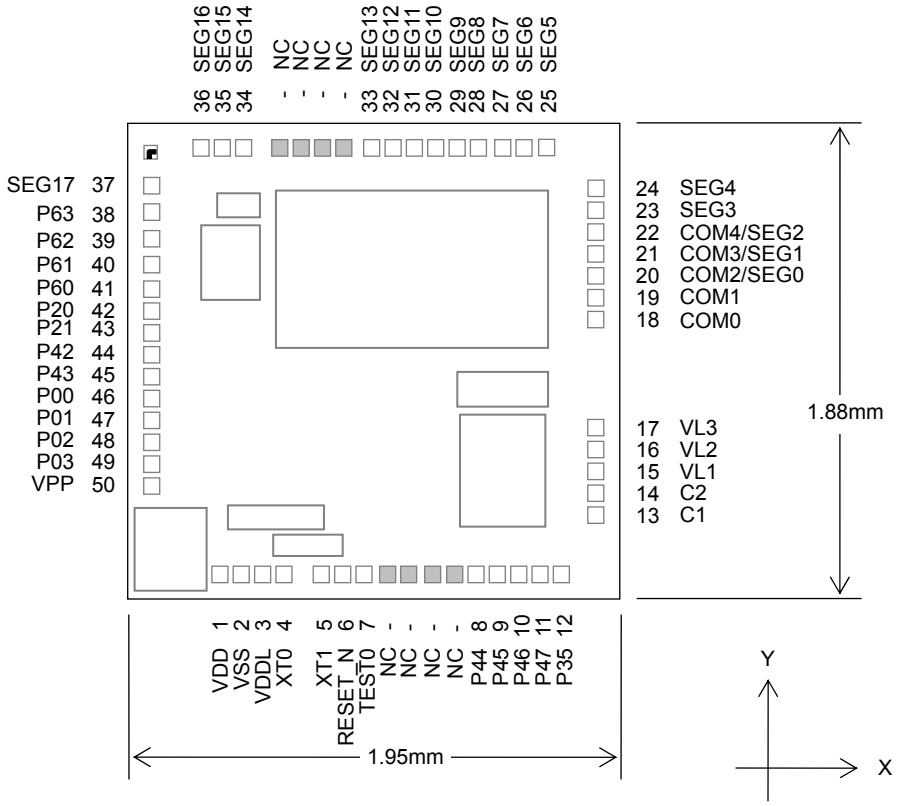


(NC): No Connection

Chip size: 1.95 mm × 1.88 mm
PAD count: 50 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

Figure 12 ML610Q471 Chip Pin Layout & Dimension

ML610Q472 Chip Pad Layout & Dimension

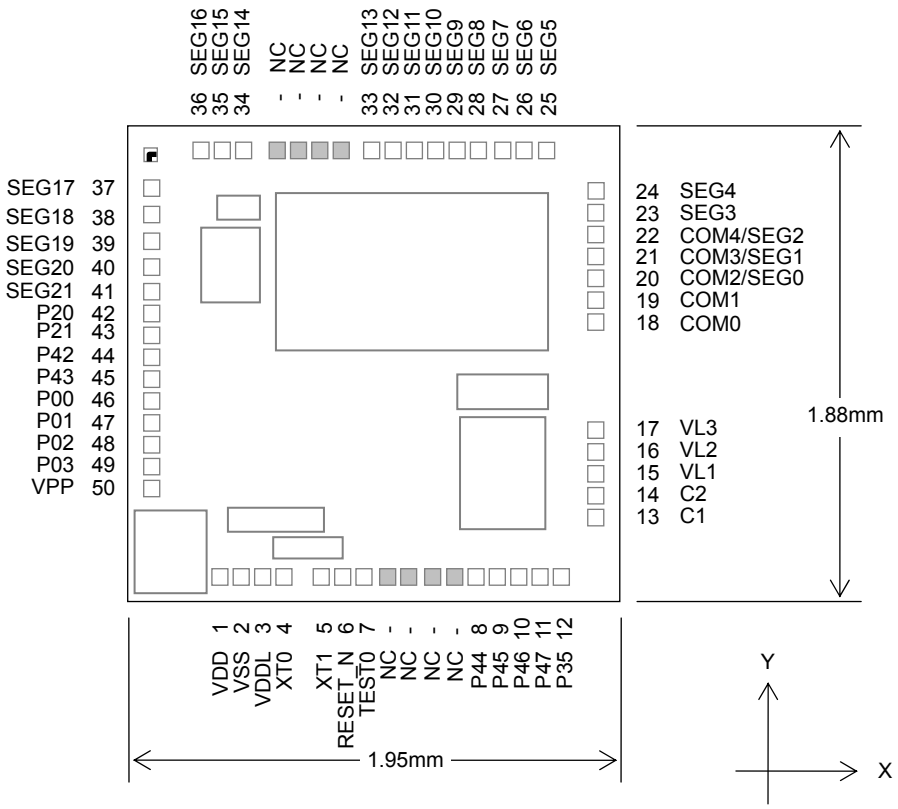


(NC): No Connection

Chip size: 1.95 mm × 1.88 mm
PAD count: 50 pins
Minimum PAD pitch: 80μm
PAD aperture: 70μm×70μm
Chip thickness: 350μm
Voltage of the rear side of chip: V_{SS} level.

Figure 13 ML610Q472 Chip Pin Layout & Dimension

ML610Q473 Chip Pad Layout & Dimension



(NC): No Connection

Chip size: 1.95 mm × 1.88 mm
PAD count: 50 pins
Minimum PAD pitch: 80 μm
PAD aperture: 70 μm×70 μm
Chip thickness: 350 μm
Voltage of the rear side of chip: V_{SS} level.

Figure 14 ML610Q473 Chip Pin Layout & Dimension

PAD COORDINATES

ML610471/ML610472/ML610473 Pad Coordinates

Table 1 ML610471/ML610472/ML610473 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610471/2/3	
		X (µm)	Y (µm)
1	VDD	-410	-779
2	VSS	-330	-779
3	VDDL	-250	-779
4	XT0	-160	-779
5	XT1	0	-779
6	RESET_N	-80	-779
7	TEST0	160	-779
8	P44	260	-779
9	P45	340	-779
10	P46	420	-779
11	P47	500	-779
12	P35	580	-779
13	C1	699	-468
14	C2	699	-388
15	VL1	699	-308
16	VL2	699	-228
17	VL3	699	-148
18	COM0	699	133
19	COM1	699	213
20	COM2/SEG0	699	293
21	COM3/SEG1	699	373
22	COM4/SEG2	699	453
23	SEG3	699	533
24	SEG4	699	613
25	SEG5	480	779
26	SEG6	400	779
27	SEG7	320	779
28	SEG8	240	779
29	SEG9	160	779

PAD No.	Pad Name	ML610471/2/3	
		X (µm)	Y (µm)
30	SEG10	80	779
31	SEG11	0	779
32	SEG12	-80	779
33	SEG13	-160	779
34	P67(*1) / SEG14(*2)(*3)	-310	779
35	P66(*1) / SEG15(*2)(*3)	-390	779
36	P65(*1) / SEG16(*2)(*3)	-470	779
37	P64(*1) / SEG17(*2)(*3)	-699	587
38	P63(*1)(*2) / SEG18(*3)	-699	507
39	P62(*1)(*2) / SEG19(*3)	-699	427
40	P61(*1)(*2) / SEG20(*3)	-699	347
41	P60(*1)(*2) / SEG21(*3)	-699	267
42	P20	-699	167
43	P21	-699	87
44	P42	-699	-13
45	P43	-699	-93
46	P00	-699	-173
47	P01	-699	-253
48	P02	-699	-333
49	P03	-699	-413

(*1) Pad for ML610471 . (*2) Pad for ML610472. (*3) Pad for ML610473.

ML610Q471/ML610Q472/ML610Q473 Pad Coordinates

Table 2 ML610Q471/ML610Q472/ML610Q473 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	ML610Q471/2/3	
		X (µm)	Y (µm)
1	VDD	-580	-834
2	VSS	-500	-834
3	VDDL	-420	-834
4	XT0	-330	-834
5	XT1	-170	-834
6	RESET_N	-90	-834
7	TEST0	-10	-834
8	P44	430	-834
9	P45	510	-834
10	P46	590	-834
11	P47	670	-834
12	P35	750	-834
13	C1	869	-523
14	C2	869	-443
15	VL1	869	-363
16	VL2	869	-283
17	VL3	869	-203
18	COM0	869	175
19	COM1	869	255
20	COM2/SEG0	869	335
21	COM3/SEG1	869	415
22	COM4/SEG2	869	495
23	SEG3	869	575
24	SEG4	869	655
25	SEG5	650	834
26	SEG6	570	834
27	SEG7	490	834
28	SEG8	410	834
29	SEG9	330	834

PAD No.	Pad Name	ML610Q471/2/3	
		X (µm)	Y (µm)
30	SEG10	250	834
31	SEG11	170	834
32	SEG12	90	834
33	SEG13	10	834
34	P67(*1) / SEG14(*2) (*3)	-480	834
35	P66(*1) / SEG15(*2) (*3)	-560	834
36	P65(*1) / SEG16(*2) (*3)	-640	834
37	P64(*1) / SEG17(*2) (*3)	-869	642
38	P63(*1) (*2) / SEG18(*3)	-869	562
39	P62(*1) (*2) / SEG19(*3)	-869	482
40	P61(*1) (*2) / SEG20(*3)	-869	402
41	P60(*1) (*2) / SEG21(*3)	-869	322
42	P20	-869	222
43	P21	-869	142
44	P42	-869	42
45	P43	-869	-38
46	P00	-869	-118
47	P01	-869	-198
48	P02	-869	-278
49	P03	-869	-358
50	VPP	-869	-438

(*1) Pad for ML610Q471 . (*2) Pad for ML610Q472. (*3) Pad for ML610Q473.

PIN LIST

PIN No.		PAD No. (MASK)	PAD No. (FLASH)	Primary function			Secondary function		
48(*1)	64(*2)			Pin name	I/O	Function	Pin name	I/O	Function
2	3	2	2	VSS	—	Negative power supply pin	—	—	—
1	2	1	1	VDD	—	Positive power supply pin	—	—	—
3	4	3	3	VDDL	—	Power supply pin for internal logic (internally generated)	—	—	—
48	63	—	50	VPP(*3)	—	Power supply pin for Flash ROM	—	—	—
15	22	15	15	VL1	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)(*2)	—	—	—
16	23	16	16	VL2	—	Power supply pin for LCD bias (internally generated or connected to positive power supply pin)(*2)	—	—	—
17	24	17	17	VL3	—	Power supply pin for LCD bias (internally generated)	—	—	—
13	20	13	13	C1	—	Capacitor connection pin for LCD bias generation	—	—	—
14	21	14	14	C2	—	Capacitor connection pin for LCD bias generation	—	—	—
7	10	7	7	TEST0	I/O	Test pin	—	—	—
6	9	6	6	RESET_N	I	Reset input pin	—	—	—
4	6	4	4	XT0	I	Low-speed clock oscillation pin	—	—	—
5	8	5	5	XT1	O	Low-speed clock oscillation pin	—	—	—
44	59	46	46	P00/EXI0/ CAP0	I	Input port, External interrupt, Capture 0 input	—	—	—
45	60	47	47	P01/EXI1/ CAP1	I	Input port, External interrupt, Capture 1 input	—	—	—
46	61	48	48	P02/EXI2/ RXD0	I	Input port, External interrupt, UART0 received data	—	—	—
47	62	49	49	P03/EXI3	I	Input port, External interrupt	—	—	—
42	55	42	42	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output
—	56	43	43	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output
12	15	12	12	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor
—	57	44	44	P42	I/O	Input/output port	RXD0	—	UART0 received data
43	58	45	45	P43	I/O	Input/output port	TXD0	O	UART data output
8	11	8	8	P44/ T2CK	I/O	Input/output port, Timer 2 external clock input	IN1	I	RC type ADC1 oscillation input pin
9	12	9	9	P45/T3CK	I/O	Input/output port, Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin
10	13	10	10	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin
11	14	11	11	P47	I/O	Input/output port	RT1	O	RC type ADC1 measurement resistor sensor connection pin

(*1) 48pin TQFP. (*2) 64pin TQFP
(*3) Pad for ML610Q471/ML610Q472/ML610Q473

PIN No.		PAD No. (MASK)	PAD No. (FLASH)	Primary function			Secondary function		
48(*1)	64(*2)			Pin name	I/O	Function	Pin name	I/O	Function
18	25	18	18	COM0	O	LCD common pin	—	—	—
19	26	19	19	COM1	O	LCD common pin	—	—	—
20	27	20	20	COM2/ SEG0	O	LCD common/segment pin	—	—	—
21	28	21	21	COM3/ SEG1	O	LCD common/segment pin	—	—	—
22	29	22	22	COM4/ SEG2	O	LCD common/segment pin	—	—	—
23	30	23	23	SEG3	O	LCD segment pin	—	—	—
24	31	24	24	SEG4	O	LCD segment pin	—	—	—
25	34	25	25	SEG5	O	LCD segment pin	—	—	—
26	35	26	26	SEG6	O	LCD segment pin	—	—	—
27	36	27	27	SEG7	O	LCD segment pin	—	—	—
28	37	28	28	SEG8	O	LCD segment pin	—	—	—
29	38	29	29	SEG9	O	LCD segment pin	—	—	—
30	39	30	30	SEG10	O	LCD segment pin	—	—	—
31	40	31	31	SEG11	O	LCD segment pin	—	—	—
32	41	32	32	SEG12	O	LCD segment pin	—	—	—
33	42	33	33	SEG13	O	LCD segment pin	—	—	—
34	44	34	34	P67(*4)	O	Output port	—	—	—
				SEG14(*5)(*6)		LCD segment pin	—	—	—
35	45	35	35	P66(*4)	O	Output port	—	—	—
				SEG15(*5)(*6)		LCD segment pin	—	—	—
36	46	36	36	P65(*4)	O	Output port	—	—	—
				SEG16(*5)(*6)		LCD segment pin	—	—	—
37	50	37	37	P64(*5)	O	Output port	—	—	—
				SEG17(*5)(*6)		LCD segment pin	—	—	—
38	51	38	38	P63(*4)(*5)	O	Output port	—	—	—
				SEG18(*6)		LCD segment pin	—	—	—
39	52	39	39	P62(*4)(*5)	O	Output port	—	—	—
				SEG19(*6)		LCD segment pin	—	—	—
40	53	40	40	P61(*4)(*5)	O	Output port	—	—	—
				SEG20(*6)		LCD segment pin	—	—	—
41	54	41	41	P60(*4)(*5)	O	Output port	—	—	—
				SEG21(*6)		LCD segment pin	—	—	—

(*1) 48pin TQFP. (*2) 64pin TQFP ,
(*3) Pad for ML610Q471/ML610Q472/ML610Q473
(*4) Pad for ML610471/ML610Q471
(*5) Pad for ML610472/ML610Q472
(*6) Pad for ML610473/ML610Q473.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal resonator is connected to this pin. Capacitors C_{DL} and C_{GL} are connected across this pin and VSS. (see appendix C measuring circuit 1)	—	—
XT1	O		—	—
LSCLK	O	Low-speed clock output. Assigned to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00 to P03	I	General-purpose input port.	Primary	Positive
General-purpose output port				
P20, P21	O	General-purpose output port. This cannot be used as the general output port when used as the secondary function.	Primary	Positive
General-purpose input/output port				
P35	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P42 to P47	I/O	General-purpose input/output port. This cannot be used as the general input/output port when used as the secondary function.	Primary	Positive
P60 to P63	O	General-purpose output port. Incorporated only into ML610471/610Q471/ML610472/ML610Q472, and not into ML610473/ML610Q473.	Primary	Positive
P64 to P67	O	General-purpose output port. Incorporated only into ML610473/ML610Q473, and not into ML610471/ML610Q471/ML610472/ ML610Q472.	Primary	Positive
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary	Positive
External interrupt				
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00 to P03 pins.	Primary/ Secondary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary	Logic
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	Positive/ negative
CAP1	I		Primary	Positive/ negative
Timer				
T2CK	I	External clock input pin used for Timer 2. This pin is used as the primary function of the P44 pin.	Primary	—
T3CK	I	External clock input pin used for Timer 3. This pin is used as the primary function of the P45 pin.	Primary	—
LED drive				
LED0-1	O	N-channel open drain output pins to drive LED. This pin is used as the primary function of the P20 pin and P21 pin.	Primary	Positive /negative
RC oscillation type A/D converter				
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—

Pin name	I/O	Description	Primary/ Secondary	Logic
LCD drive signal				
COM0 to COM4	O	Common output pins. COM2, COM3, and COM4 can be switched to SEG0, SEG1, and SEG2, respectively, through the register setting. To change the setting, switch between COM4 and SEG2 for one pin and switch between COM3, COM4 and SEG1, SEG2 for two pins.	—	—
SEG0 to SEG13	O	Segment output pin. The SEG0, SEG1, and SEG2 pins are for switching the register setting with the COM2, COM3, and COM4.	—	—
SEG14 to SEG17	O	Segment output pin. Incorporated into ML610472/ML610Q472/ML610473/ML610Q473, not into ML610471/ML610Q471.	—	—
SEG18 to SEG21	O	Segment output pin. Incorporated into ML610473/ML610Q473, not into ML610471/ML610Q471/ML610472/ML610Q472.	—	—
LCD driver power supply				
VL1	—	Power supply pin for LCD bias (internally generated) or power supply connection pin. Depending on LCD Bias setting and V_{DD} voltage level, V_{DD} or V_{DDL} or capacitor is connected. For details of the connection method, see measuring circuit 1.	—	—
VL2	—		—	—
VL3	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitor C_{12} (see measuring circuit 1) is connected between C1 and C2.	—	—
C2	—		—	—
Test				
TEST0	I/O	Pin for testing. A pull-down resistor is internally connected.	—	Positive
Power supply				
VSS	—	Negative power supply pin.	—	—
VDD	—	Positive power supply pin.	—	—
VDDL	—	Positive power supply pin (internally generated) for internal logic. Capacitors C_{L0} and C_{L1} (see measuring circuit 1) are connected between this pin and VSS.	—	—
VPP	—	Power supply pin for programming Flash ROM. A pull-down resistor is internally connected. This pin is only for ML610Q471/ML610Q472/ML610Q473.	—	—

TERMINATION OF UNUSED PINS

Table 2 shows methods of terminating the unused pins.

Table 2 Termination of Unused Pins

Pin	Recommended pin handling
VPP	Open
VL1	Open
VL2	Open
VL3	Open
C1, C2	Open
RESET_N	Open
TEST0	Open
P00 to P03	VDD or VSS
P20, P21	Open
P35	Open
P42 to P47	Open
P60 to P67	Open
COM0 to COM4	Open
SEG0 to SEG21	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS}= 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	-0.3 to +4.6	V
Power supply voltage 2	V_{PP}	Ta=25°C	-0.3 to +9.5	V
Power supply voltage 3	V_{DDL}	Ta=25°C	-0.3 to +3.6	V
Power supply voltage 4	V_{L1}	Ta=25°C	-0.3 to +2.0	V
Power supply voltage 5	V_{L2}	Ta=25°C	-0.3 to +4.0	V
Power supply voltage 6	V_{L3}	Ta=25°C	-0.3 to +6.0	V
Input voltage	V_{IN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port 3 to 6, Ta=25°C	-12 to +11	mA
Output current 2	I_{OUT2}	Port 2, Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	0.9	W
Storage temperature	T_{STG}	—	-55 to +150	°C

Recommended Operating conditions

(V_{SS}= 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	without P version	-20 to +70	°C
		P version	-40 to +85	
Operating voltage	V_{DD}	f_{OP}=30k to 625kHz	1.25 to 3.6	V
Operating frequency (CPU)	f_{OP}	V_{DD}=1.25 to 3.6V	30k to 625k	Hz
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitance	C_{DL}	—	3 to 18	pF
	C_{GL}	—	3 to 18	
V_{DDL} pin external capacitance	C_L	—	0.47±30%	µF
$V_{L1, 2, or 3}$ pin external capacitance	$C_{a,b,c}$	—	0.1±30%	µF
Pin-to-pin (C1 to C2) external capacitance	C_{12}	—	0.47±30%	µF

Operating conditions of FlashROM

(VSS= 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase	2.75 to 3.6	V
	V_{DDL}	At write/erase*1	2.5 to 2.75	
	V_{PP}	At write/erase	7.7 to 8.3	
Rewrite count	C_{EP}	—	80	cycles
Data retention	Y_{DR}	—	10	years

*1: When writing to and erasing on the flash Memory, the voltage in the specified range needs to be supplied to the V_{DDL} pin. The V_{PP} pin has an internal pull-down resistor.

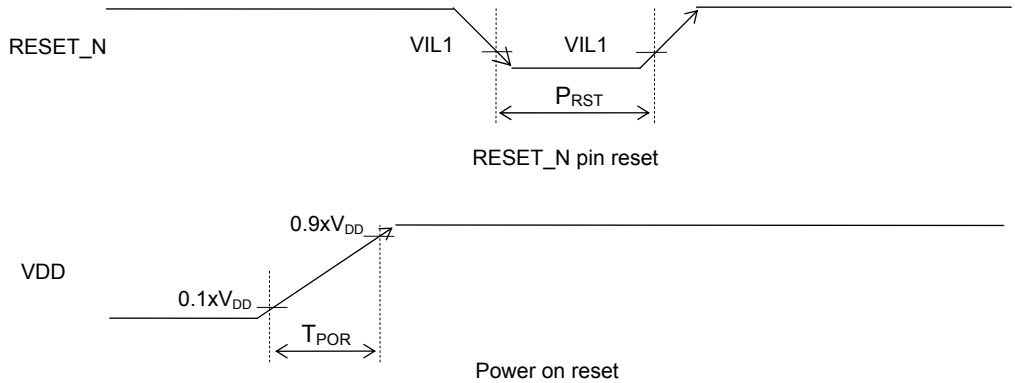
DC Characteristics (1/6)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measurement circuit
500kHz RC oscillation frequency	f_{RC}	V_{DD}=1.25 to 3.6V	Ta=25°C	Typ. -10%	500	Typ. +10%	kHz	1
			*2	Typ. -25%	500	Typ. +25%	kHz	
Low-speed crystal oscillation start time*1	T_{XTL}	—		—	0.6	2	s	
500kHz RC oscillation start time	T_{RC}	—		—	—	3	µs	
Reset pulse width	P_{RST}	—		200	—	—	µs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset generated power rise time	T_{POR}	—		—	—	10	ms	

*1: 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=12pF).
*2: Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)

RESET



DC Characteristics (2/6)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
V_{DDL} voltage	V_{DDL}	fop=30k to 625kHz	1.1	1.2	1.3	V	1
V_{DDL} temperature deviation *1	ΔV_{DDL}	V_{DD}=3.0V	—	-1	—	mV/°C	
V_{DDL} voltage dependency *1	ΔV_{DDL}	—	—	5	20	mV/V	

*1: The maximum V_{DDL} voltage becomes the V_{DD} voltage level when the V_{DDL} voltage determined by the temperature and voltage deviations mathematically exceeds the V_{DD} voltage.

DC Characteristics for ML610471/472/473 (3/6)

(VDD=3.0V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measurement circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/High-speed oscillation: stopped.	Ta=25°C	—	0.3	0.8	µA	1
			*5	—	—	3		
Supply current 2	IDD2	CPU: In HALT state. (LTBC, WDT: Operating)*3*4. High-speed 500kHz oscillation: Stopped. LCD/BIAS circuits: Operating *6	Ta=25°C	—	0.8	1.8	µA	
			*5	—	—	4		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz oscillation: Stopped, LCD/BIAS circuits: Operating *2	Ta=25°C	—	3	6	µA	
			*5	—	—	9		
Supply current 4-1	IDD4-1	CPU: In 500kHz RC operating state. LCD/BIAS circuits: Operating.*2	Ta=25°C	—	50	70	µA	
			*5	—	—	80		

*1: When the CPU operating rate is 100% (no HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : 32.768KHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF)
*4 : Significant bits of BLKCON0 to BLKCON4 registers are all "1" except DLCD bit on BLKCON4.
*5 : Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)
*6: LCD stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

DC Characteristics for ML610Q471/Q472/Q473 (4/6)

(VDD=3.0V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measurement circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/High-speed oscillation: stopped.	Ta=25°C	—	0.3	1.25	µA	1
			*5	—	—	5.5		
Supply current 2	IDD2	CPU: In HALT state. (LTBC, WDT: Operating)*3*4. High-speed 500kHz oscillation: Stopped. LCD/BIAS circuits: Operating *6	Ta=25°C	—	0.8	3.2	µA	
			*5	—	—	8.5		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed 500kHz oscillation: Stopped, LCD/BIAS circuits: Operating *2	Ta=25°C	—	4.7	7.5	µA	
			*5	—	—	13		
Supply current 4-1	IDD4-1	CPU: In 500kHz RC operating state. LCD/BIAS circuits: Operating.*2	Ta=25°C	—	70	100	µA	
			*5	—	—	120		

*1: When the CPU operating rate is 100% (no HALT state).
*2: All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : 32.768KHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=6pF)
*4 : Significant bits of BLKCON0 to BLKCON4 registers are all "1" except DLCD bit on BLKCON4.
*5 : Recommended operating temperature (Ta=-20 to 70°C, Ta=-40 to 85°C for P version)
*6: LCD stop mode, 1/3 bias, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)

DC Characteristics (5/6)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Output voltage 1 (P20, P21 (N-channel open drain output mode is not selected)) (P35) (P42 to P47) (P60 to P63) *2 (P60 to P67) *1	VOH1	IOH1=-0.5mA, V_{DD}=1.8 to 3.6V	V_{DD} -0.5	—	—	V	2
		IOH1=-0.03mA, V_{DD}=1.25 to 3.6V	V_{DD} -0.3	—	—		
	VOL1	IOL1=+0.5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
		IOL1=+0.1mA, V_{DD}=1.25 to 3.6V	—	—	0.3		
Output voltage 2 (P20, P21 (N-channel open drain output mode is selected))	VOL2	IOL2=+5mA, V_{DD}=1.8 to 3.6V	—	—	0.5		
Output voltage 3 (COM0 to 4) (SEG0 to 13) *1 (SEG0 to 17) *2 (SEG0 to 21) *3	VOH3	IOH3=-0.05mA, VL1=1.2V	V_{L3} -0.2	—	—		
	VOML3	IOML3=+0.05mA, VL1=1.2V	—	—	V_{L2} +0.2		
	VOML3S	IOML3S=-0.05mA, VL1=1.2V	V_{L2} -0.2	—	—		
	VOLM3	IOLM3=+0.05mA, VL1=1.2V	—	—	V_{L1} +0.2		
	VOLM3S	IOLM3S=-0.05mA, VL1=1.2V	V_{L1} -0.2	—	—		
	VOL3	IOL3=+0.05mA, VL1=1.2V	—	—	0.2		
Output leakage (P20, P21) (P35) (P42 to P47) (P60 to P63) *2 (P60 to P67) *1	IOOH	VOH=V_{DD} (in high-impedance state)	—	—	1	μA	3
	IOOL	VOL=V_{SS} (in high-impedance state)	-1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1=V_{DD}	—	—	1	μA	4
	IIL1	VIL1=V_{SS}	-600	-300	-2		
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	2	300	600		
	IIL2	VIL2=V_{SS}	-1	—	—		
Input current 3 (P00 to P03) (P35) (P42 to P47)	IIH3	VIH3=V_{DD}, V_{DD}=1.8 to 3.6V (when pulled-down)	2	30	200		
		VIH3=V_{DD}, V_{DD}=1.25 to 3.6V (when pulled-down)	0.01	30	200		
	IIL3	VIL3=V_{SS}, V_{DD}=1.8 to 3.6V (when pulled-up)	-200	-30	-2		
		VIL3=V_{SS}, V_{DD}=1.25 to 3.6V (when pulled-up)	-200	-30	-0.01		
	IIH3Z	VIH3=V_{DD} (in high-impedance state)	—	—	1		
	IIL3Z	VIL3=V_{SS} (in high-impedance state)	-1	—	—		

*1: Characteristics for ML610471/ML610Q471.
*2: Characteristics for ML610472/ML610Q472.
*3: Characteristics for ML610473/ML610Q473.

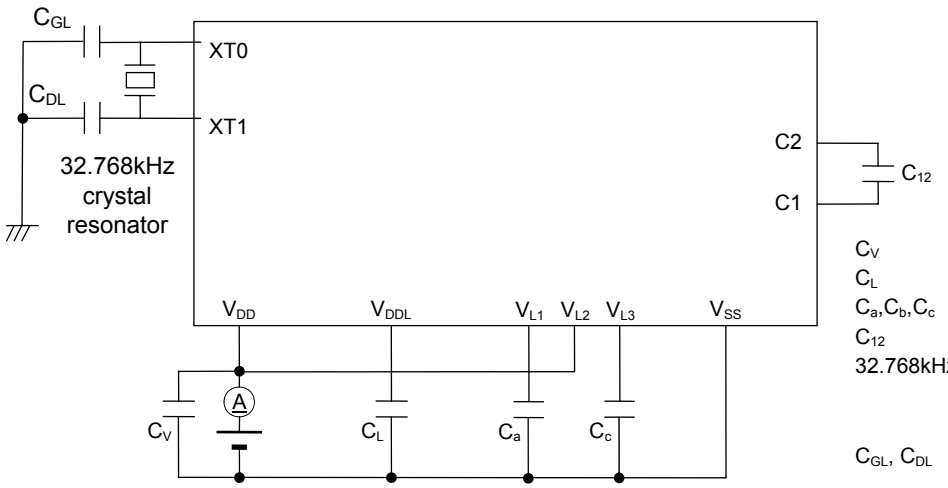
DC Characteristics (6/6)

(VDD=1.25 to 3.6V, VSS=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measurement circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST0) (P00 to P03) (P35) (P42 to P47)	VIH1	—	0.7 ×V_{DD}	—	V_{DD}	V	5
	VIL1	V_{DD}=1.25 to 3.6V	0	—	0.2 ×V_{DD}		
Input pin capacitance (P00 to P03) (P35) (P42 to P47)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	—	—	5	pF	—

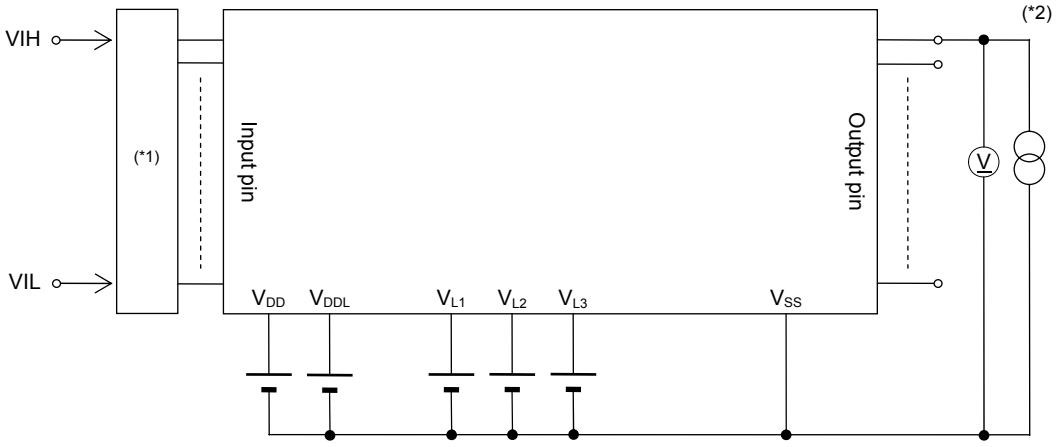
Measuring Circuits

Measuring Circuit 1



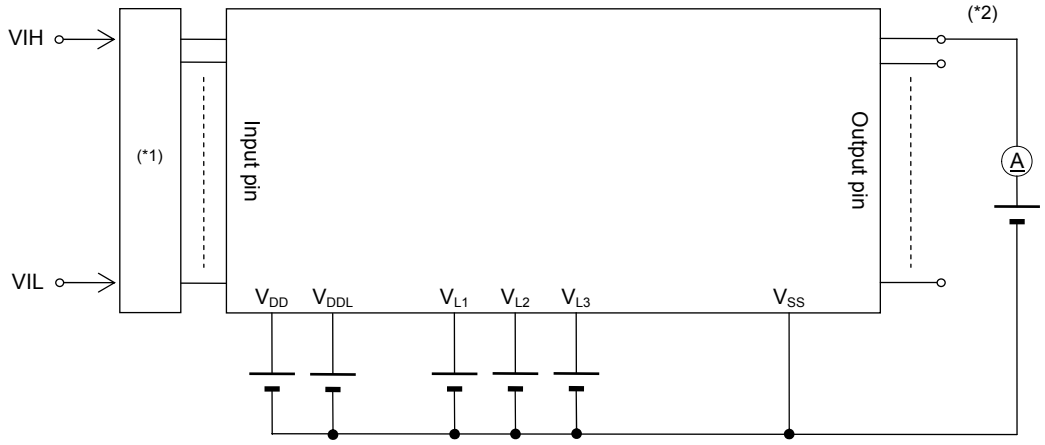
C_V : 1µF
C_L : 0.47uF
C_a,C_b,C_c : 0.1µF
C_{12} : 0.47µF
32.768kHz crystal resonator
: DT-26 (Load capacitance 6pF)
(Made by KDS:DAISHINKU CORP.)
C_{GL}, C_{DL} : 6pF

Measuring Circuit 2



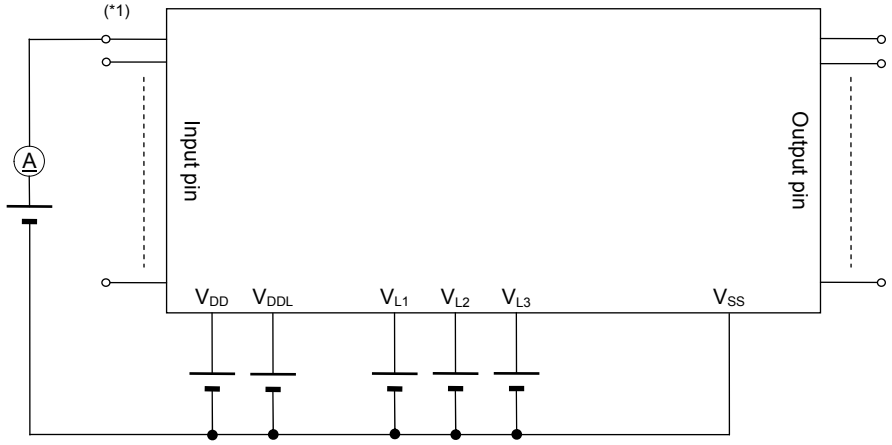
*1: Input logic circuit to determine the specified measuring conditions.
*2: Repeats for the specified output pin

Measuring Circuit 3



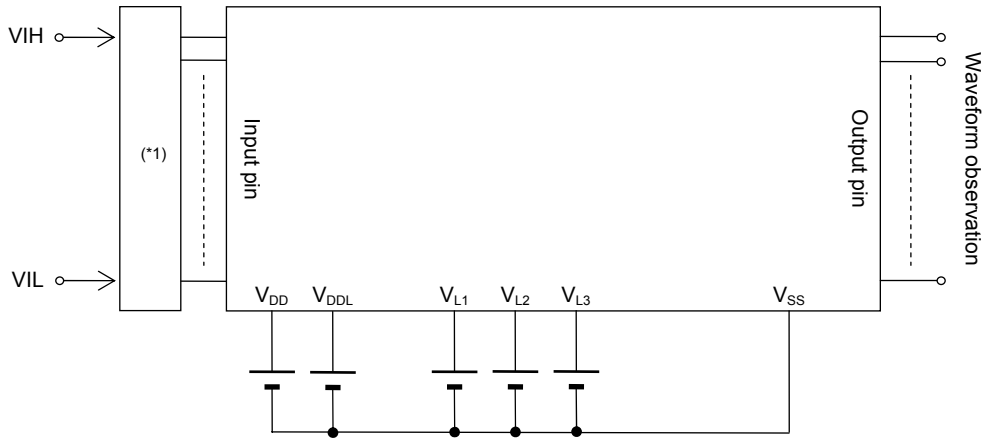
*1: Input logic circuit to determine the specified measuring conditions.
*2: Repeats for the specified output pin

Measuring Circuit 4



*1: Repeats for the specified input pin

Measuring Circuit 5

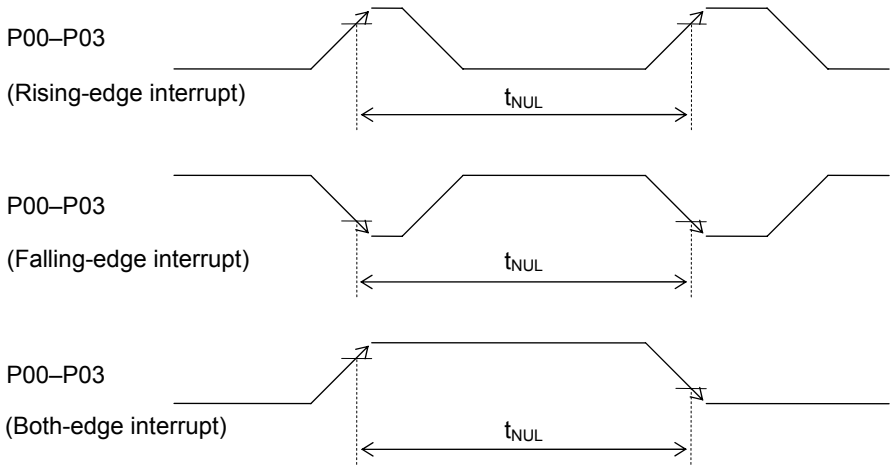


*1: Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation, System clock: 32.768kHz	76.8	—	106.8	μs

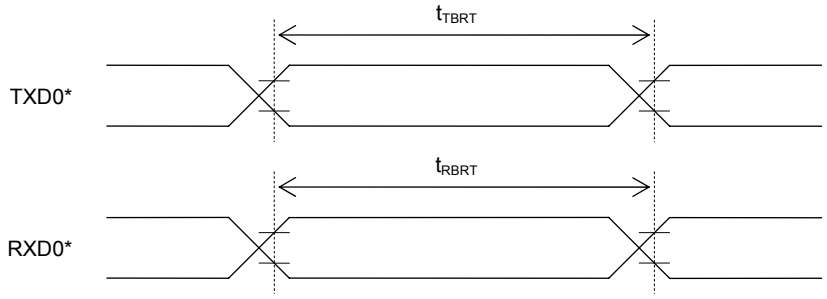


AC Characteristics (UART)

(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*1	—	s
Receive baud rate	t_{RBRT}	—	BRT*1 -3%	BRT*1	BRT*1 +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).



*: Indicates the secondary function of the port.

AC Characteristics (RC Oscillation A/D Converter)

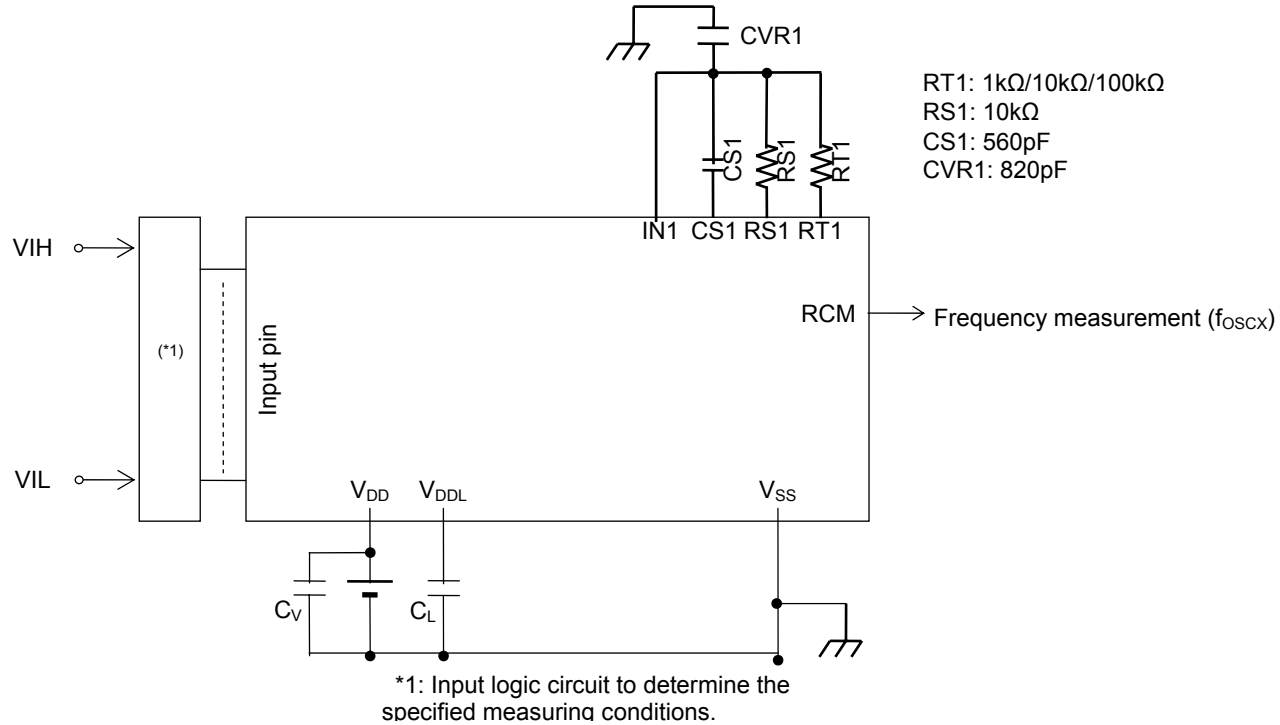
Condition for V_{DD}=1.8 to 3.6V

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=1kΩ	457.3	525.2	575.1	kHz
	f_{OSC2}	Resistor for oscillation=10kΩ	53.48	58.18	62.43	kHz
	f_{OSC3}	Resistor for oscillation=100kΩ	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V	Kf1	RT1=1kΩ	7.972	9.028	9.782	—
	Kf2	RT1=10kΩ	0.981	1	1.019	—
	Kf3	RT1=100kΩ	0.099	0.101	0.104	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(\text{RT1-CS1 oscillation})}{f_{OSCx}(\text{RS1-CS1 oscillation})} \quad , \quad (x = 1, 2, 3)$$



*1: Input logic circuit to determine the specified measuring conditions.

Condition for V_{DD}=1.25 to 3.6V

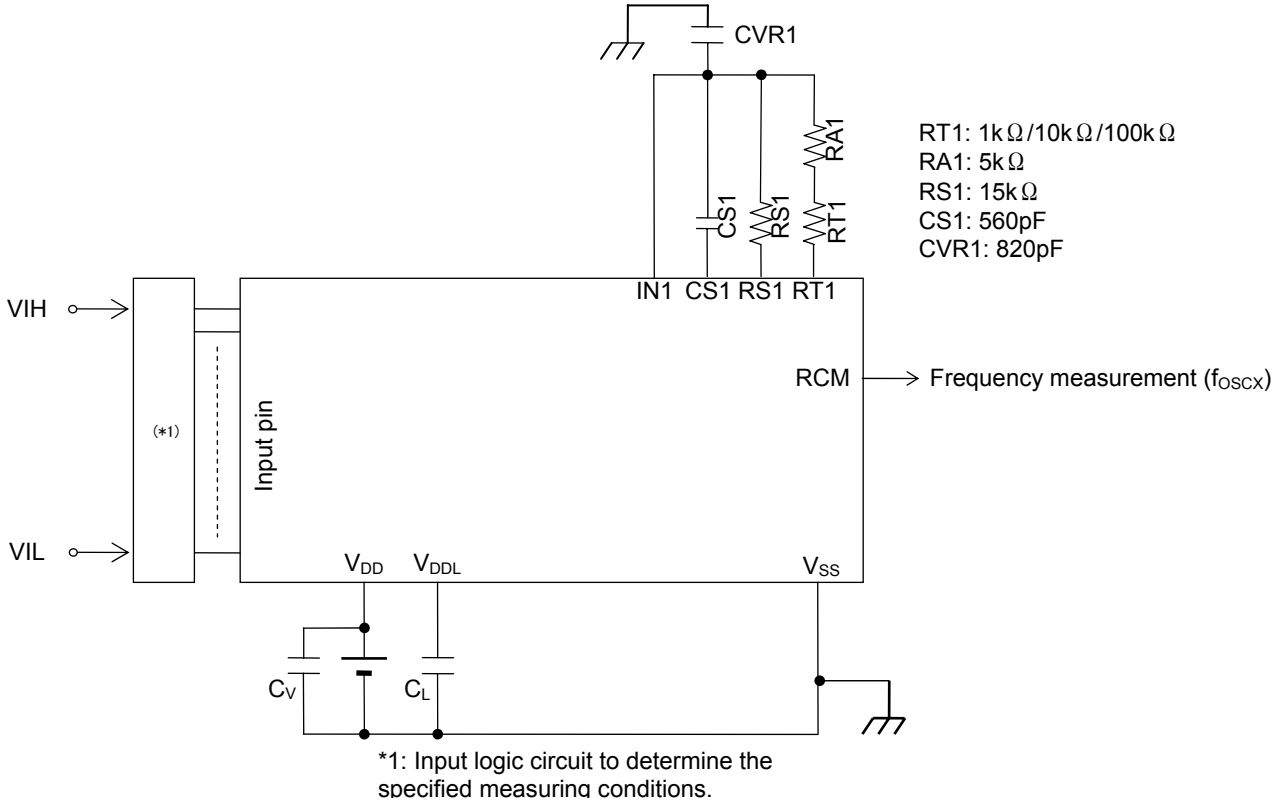
(V_{DD}=1.25 to 3.6V, V_{SS}=0V, Ta=-20 to +70°C, Ta=-40 to +85°C for P version, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS1,RT1	CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 1.5V	f_{OSC1}	Resistor for oscillation=6kΩ	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 1.5V	Kf1	RT1=1kΩ	2.139	2.381	2.632	—
	Kf2	RT1=10kΩ	0.973	1	1.028	—
	Kf3	RT1=100kΩ	0.142	0.147	0.152	—
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=6kΩ	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V	Kf1	RT1=1kΩ	2.227	2.432	2.626	—
	Kf2	RT1=10kΩ	0.982	1	1.018	—
	Kf3	RT1=100kΩ	0.141	0.145	0.149	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(\text{RT1-CS1 oscillation})}{f_{OSCx}(\text{RS1-CS1 oscillation})} \quad (x = 1, 2, 3)$$

,



*1: Input logic circuit to determine the specified measuring conditions.

Note:

・Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN1 pin), including CVR1. Especially, do not have long wiring between IN1 and RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

・When RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have V_{SS}(GND) trace next to the signal.

・Please make wiring to components (capacitor, resistor, and so on) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

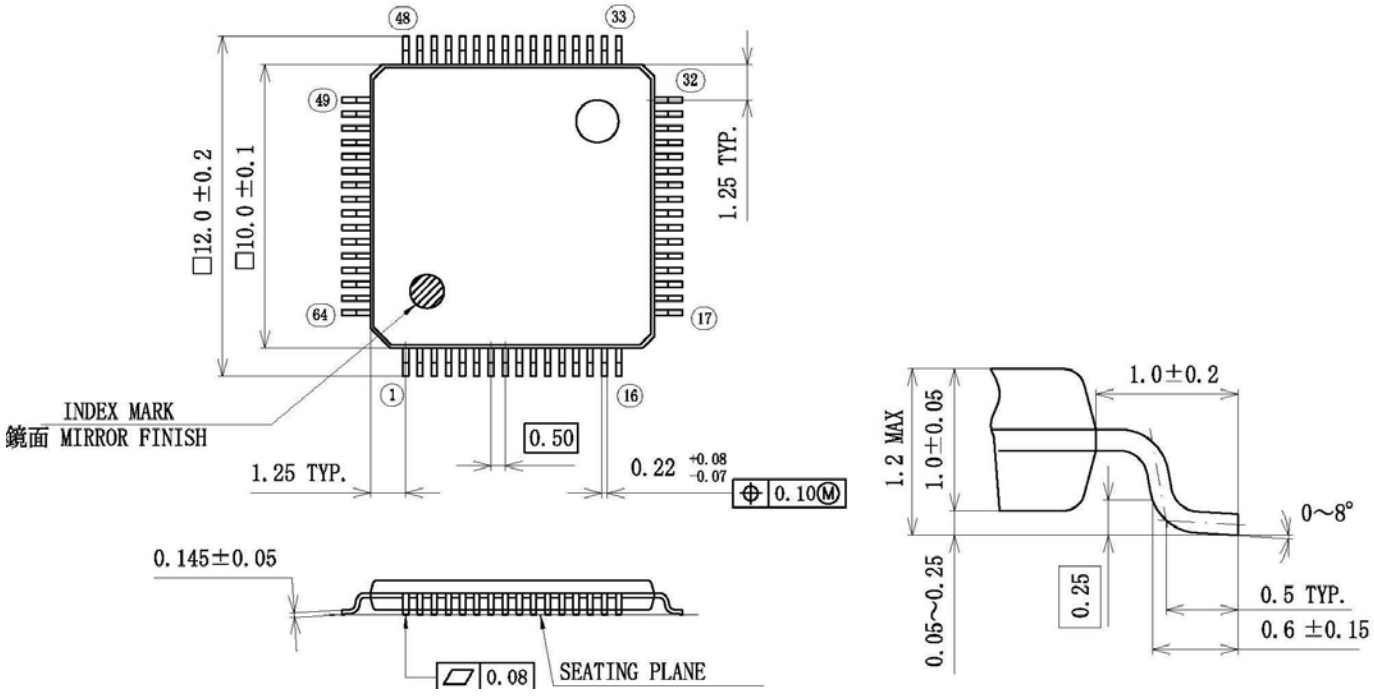
PACKAGE DIMENSIONS

(Unit: mm)

64pin TQFP Package

(Unit: mm)

P-TQFP64-1010-0.50-ZK1



Package material	Epoxy resin
Lead frame material	Cu alloy
Lead finish	Sn-2Bi (Bi 2%typ.)
Solder thickness	More than 5μm
Package weight (g)	0.26typ.
Rev. No./Last Revised	2 / Feb. 16,2011

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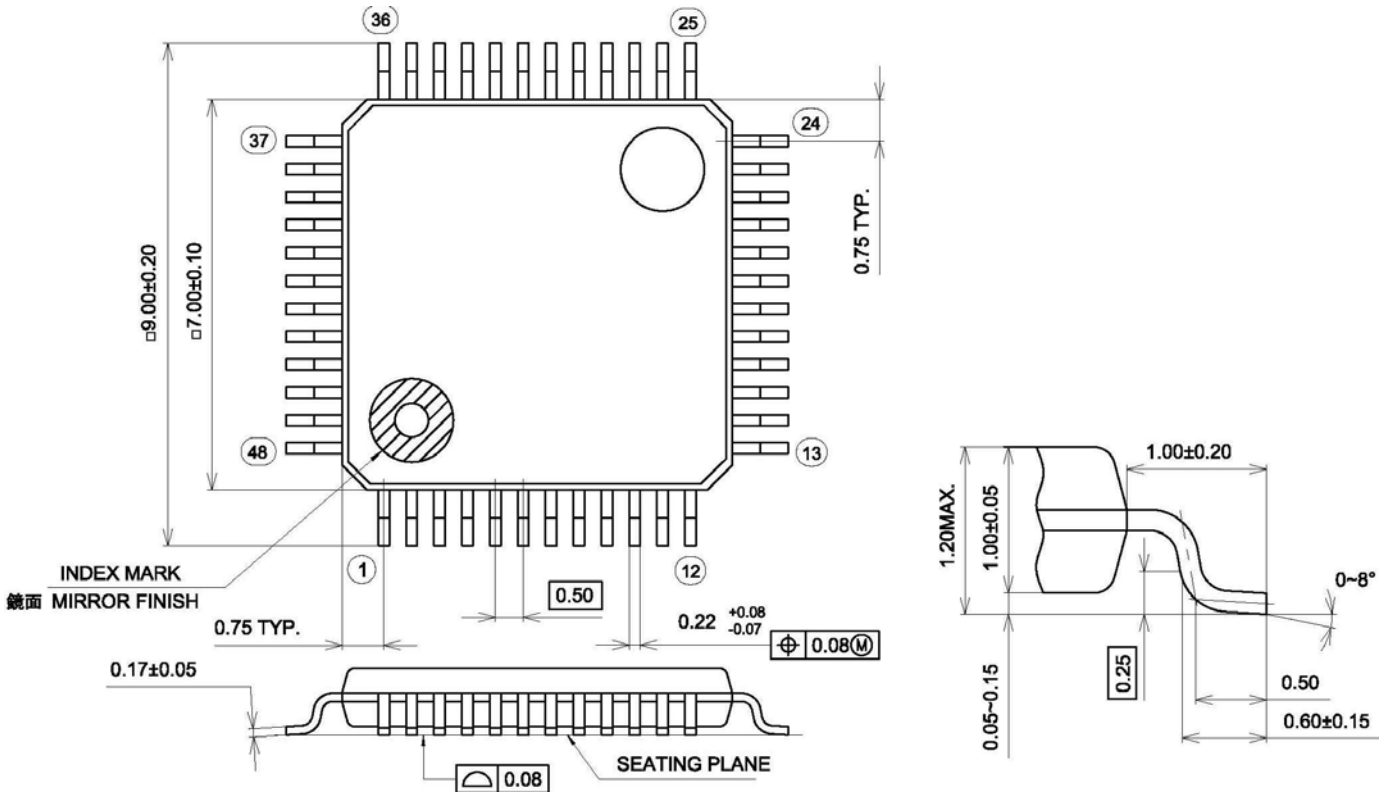
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

48 pin TQFP Package

P-TQFP48-0707-0.50-K



LAPIS Semiconductor Co.,Ltd.

Package material	Epoxy resin
Lead frame material	42 alloy
Lead finish	Sn-2Bi (Bi 2%typ.)
Solder thickness	More than 5μm
Package weight (g)	0.13typ.
Rev. No./Last Revised	2 / Feb. 17,2010

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact our responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVESION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610473-01	Apr.25,2011	–	–	Formally edition 1
FEDL610473-02	May.10,2011	1,2,3	1,2,3	Add Mask ROM version(ML610471/ML610472/ML610473)
		–	4	Add Block Diagram (Mask ROM version)
		–	12,13,14	Add Chip Pad Layout and Dimensions (Mask ROM version)
		15,16	20,21	Add Pad No of Mask ROM version into PIN list.
FEDL610473-03	Sep.13,2011	3	3	The package name of TQFP48 was changed.
		15-17, 19-21	15-17, 19-21	The pads number were changed.
		28	29	Add DC Characterristics (ML610471/ML610472/ML610473)
FEDL610473-04	Sep.28,2011	15-17	15-17	The figures were revised.

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