Integrated Device Technology, Inc.

256KB/ 1MB/ 4MB IDT79R4000 SECONDARY CACHE MODULE BLOCK FAMILY

PRELIMINARY
IDT7MP6074
IDT7MP6084
IDT7MP6094

FEATURES:

- High-speed BiCMOS/CMOS secondary cache module block constructed to support the IDT79R4000 CPU
- Available as a pin compatible family to build 256KB (unified), 1MB (unified) and 4MB (unified or split) secondary caches
- Zero wait-state operation
- Four-word line size
- Operating frequencies to support 50MHz and 75MHz IDT79R4000
- Available as a set of four identical high-density 80-lead (gold-plated fingers) SIMMs (Single In-Line Memory Modules)
- Surface mounted plastic components on a multilayer epoxy laminate (FR-4) substrate
- Multiple ground pins and decoupling capacitors for maximum noise immunity
- TTL compatible I/Os
- Single 5V (±10%) power supply

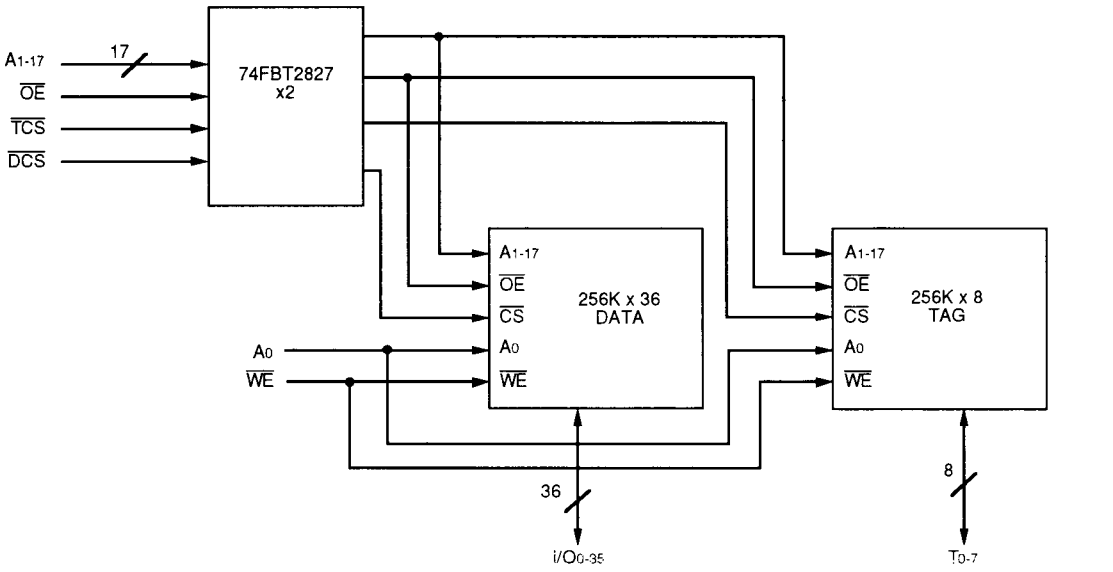
DESCRIPTION:

The IDT7MP6074 is a 256KB IDT79R4000 secondary cache module block constructed on a multilayer epoxy laminate substrate (FR-4), using eleven 16K x 4 SRAMs and two IDT74FBT2827 drivers. The IDT7MP6084 is a 1MB IDT79R4000 secondary cache module block using eleven 64K x 4 SRAMs, and the IDT7MP6094 is a 4MB IDT79R4000 secondary cache module block using eleven 256K x 4 static RAMs. The IDT74FBT2827 has internal 25W series resistors and BiCMOS I/Os resulting in the fastest propagation times with minimal overshoot and ringing. Four identical cache module blocks comprise a full secondary cache.

The IDT7MP6074/84/94 support use in an IDT79R4000-based system at speeds of 50MHz and 75MHz with zero wait-state operation. These modules support a four word line size. For other line sizes, please consult factory.

All inputs and outputs of the IDT7MP6074/84/94 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refresh for operation.

FUNCTIONAL BLOCK DIAGRAM



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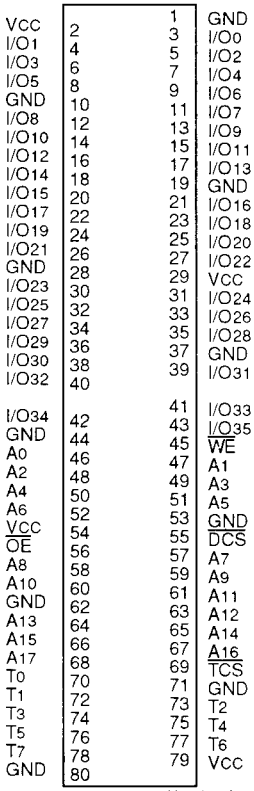
PIN CONFIGURATION



2833 drw 02

SIMM
TOP VIEW

PIN NAMES

I/O0-35	Data Inputs/Outputs
T0-7	Tag Inputs/Outputs
A0-17	Address Inputs
$\overline{DCS}$	Data Chip Select
$\overline{TCS}$	Tag Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground

2833 tbl 02

CAPACITANCE

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN(D)	Input Capacitance (Data)	VIN = 0V	10	pF
CIN(A)	Input Capacitance (A1-15, $\overline{OE}$, $\overline{TCS}$, $\overline{DCS}$)	VIN = 0V	10	pF
CIN(B)	Input Capacitance (A0, $\overline{WE}$)	VIN = 0V	100	pF
COUT	Output Capacitance	VOUT = 0V	10	pF

NOTE:
1. This parameter is guaranteed by design, but not tested.

2833 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6	V
VIL	Input Low Voltage	−0.5[1]	—	0.8	V

NOTE:
1. VIL = −1.5V for pulse width less than 10ns.

2833 tbl 04

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating[1]	Value	Unit
VTERM	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	−10 to +85	°C
TSTG	Storage Temperature	−55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2833 tbl 05

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%

2833 tbl 01

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DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI1}\|$	Input Leakage (except A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	10	µA
$\|I_{LI2}\|$	Input Leakage (A_0, $\overline{WE}$)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	110	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	10	µA
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}; V_{CC} = Max., Outputs Open	—	2200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V

2833 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 - 4

2833 tbl 07

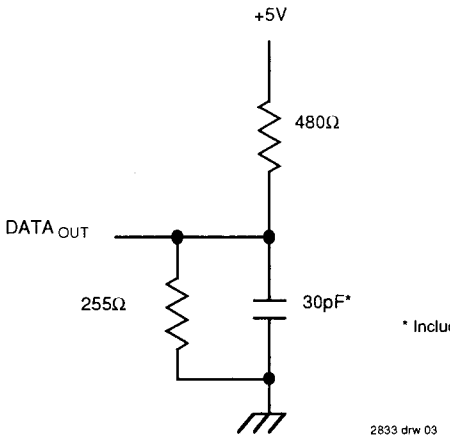

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Figure 1. Output Load

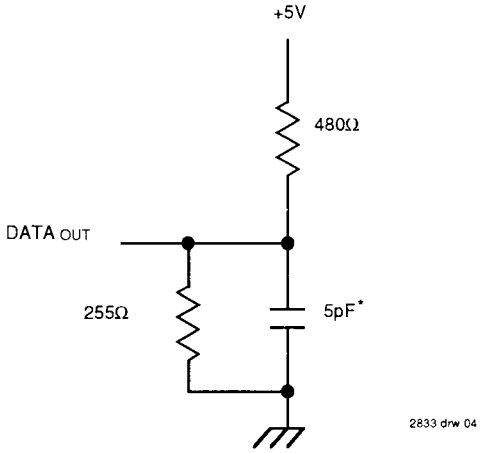

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Figure 2. Output Load (for t_{OLZ} and t_{OHZ})

* Including scope and jig.

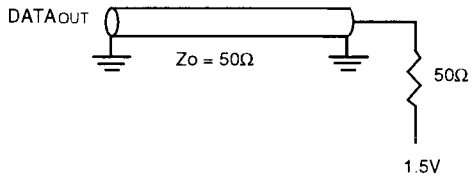

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Figure 3. Alternate Output Load

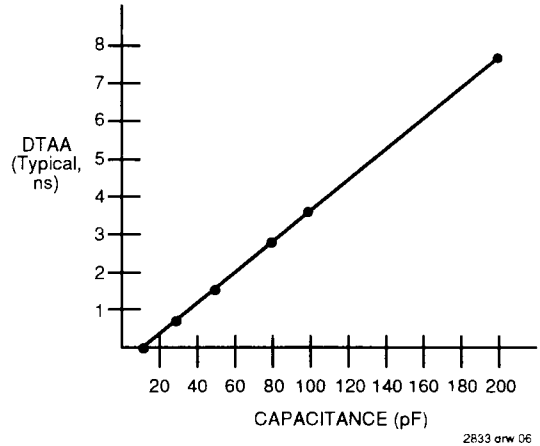

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Figure 4. Alternate Lumped Capacitive Load, Typical Derating

AC ELECTRICAL CHARACTERISTICS

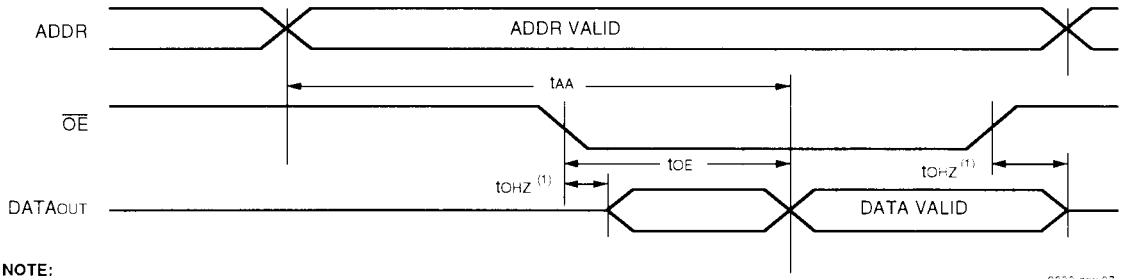
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP6074/6084/6094SxxM												Unit
		-12		-15		-17		-20		-25		-30		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{AA}	Address Access Time	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{A0A}	A_0 Access Time	—	10	—	12	—	14	—	16	—	21	—	26	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	17	—	20	—	25	—	30	ns
t_{OHZ}[1]	Output Disable to Output in High-Z	—	10	—	12	—	13	—	15	—	17	—	20	ns
t_{OLZ}[1]	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	2	—	2	—	ns
WRITE CYCLE														
t_{AW}	Address Valid to End-of-Write	12	—	15	—	17	—	20	—	25	—	30	—	ns
t_{A0W}	A_0 Valid to End-of-Write	10	—	12	—	14	—	16	—	21	—	26	—	ns
t_{WP}	Write Pulse Width	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DW}	Data Valid to End-of-Write	7	—	10	—	12	—	15	—	20	—	25	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns

NOTE:
1. This parameter is guaranteed by design but not tested.

2833 tbl 08

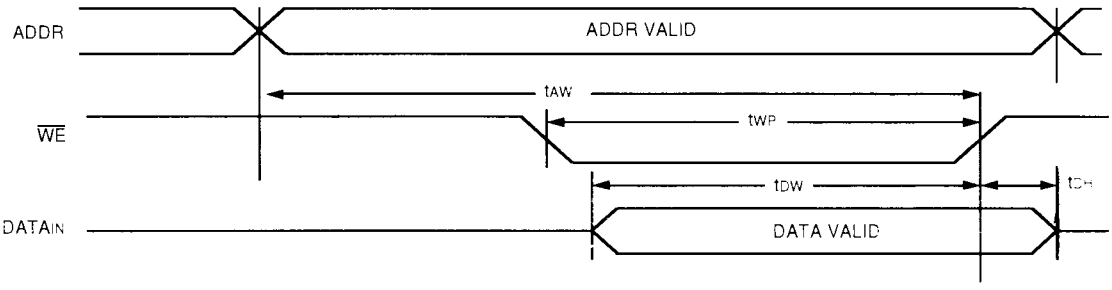
TIMING WAVEFORM OF READ CYCLE[1]



NOTE:
1. This parameter is guaranteed by design, but not tested.

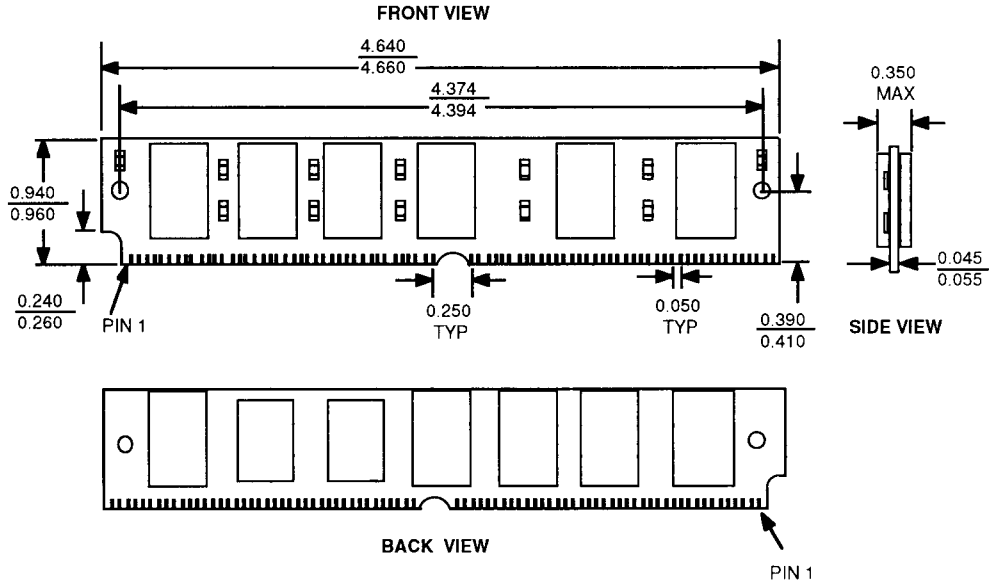
2833 drw 07

TIMING WAVEFORM OF WRITE CYCLE



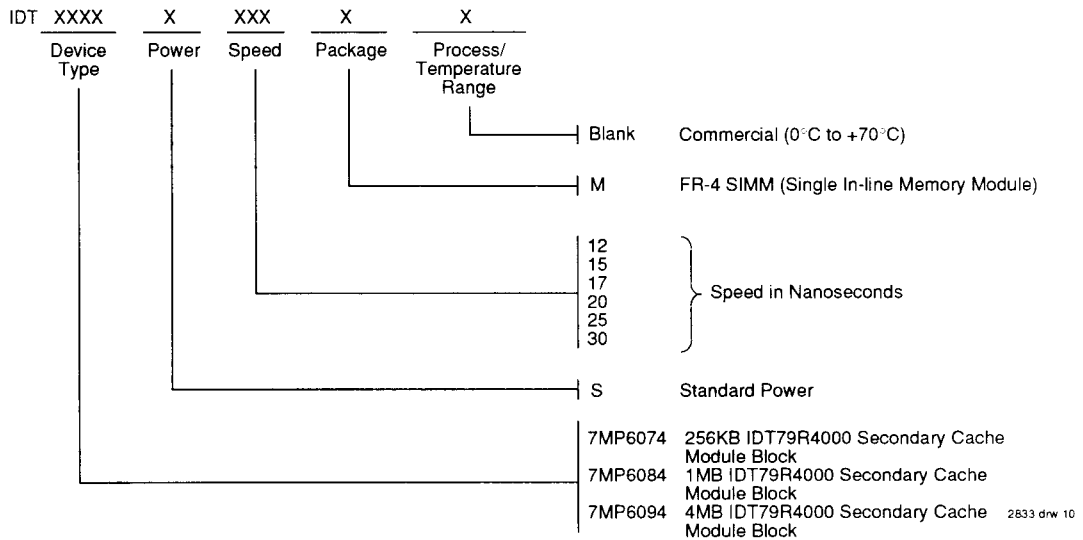
2833 drw 08

PACKAGE DIMENSIONS



2833 drw 09

ORDERING INFORMATION



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