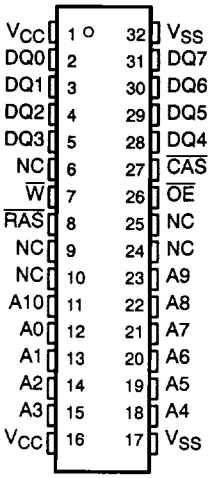
- **Organization . . . 2 097 152 × 8**
- **Single 5-V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

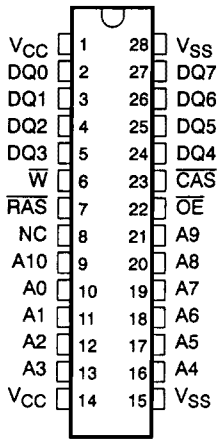
	ACCESS TIME (t_{RAC}) (MAX)	ACCESS TIME (t_{CAC}) (MAX)	ACCESS TIME (t_{AA}) (MAX)	READ OR WRITE CYCLE (MIN)
'417800/P-60	60 ns	15 ns	30 ns	110 ns
'417800/P-70	70 ns	18 ns	35 ns	130 ns
'417800/P-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . .**
  - **2048-Cycle Refresh in 32 ms (Max)**
  - **256 ms for Low Power, Self-Refresh Version (TMS417800P)**
- **3-State Unlatched Output**
- **Low Power Dissipation**
- **Self-Refresh With Low-Power**
- **All Inputs/Outputs and Clocks are TTL Compatible**
- **High-Reliability Plastic 28-Pin, J-Lead 400-Mil-Wide Surface Mount Package (SOJ), and 32-Pin, Plastic Thin Small Outline Package (TSOP)**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Texas Instruments EPIC™ CMOS Process**

DE PACKAGE† (TOP VIEW)



DZ PACKAGE† (TOP VIEW)



† Packages are shown for pinout reference only.

PIN NOMENCLATURE	
A0–A10	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ7	Data In/Data Out
NC	No Internal Connection
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
$\overline{W}$	Write-Enable
V_{CC}	5-V Supply
V_{SS}	Ground

PRODUCT PREVIEW

description

The TMS417800 series are high-speed 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

The TMS417800P series are high-speed, low-power, self-refresh, 16 777 216-bit dynamic random-access memories, organized as 2 097 152 words of eight bits each.

They employ state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at low cost.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. Maximum power dissipation is as low as 578 mW operating and 11 mW standby for 80 ns devices.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS417800 and TMS417800P series are offered in a 400-mil 28-lead plastic surface mount SOJ package (DZ suffix) and a 32-lead plastic surface mount TSOP package (DE suffix). These packages are characterized for operation from 0°C to 70°C.

EPIC is a trademark of Texas Instruments Incorporated.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and the $\overline{CAS}$ page cycle time used. With minimum $\overline{CAS}$ page cycle time, all 1024 columns specified by column addresses A0 through A9 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS417800 and TMS417800P to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as *enhanced page mode.* Valid column address may be presented immediately after row address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low), if t_{AA} max (access time from column address) has been satisfied. In the event that column addresses for the next cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CAC} or t_{CPA} (access time from rising edge of $\overline{CAS}$).

address (A0–A10)

Twenty-one address bits are required to decode 1 of 2 097 152 storage cell locations. Eleven row-address bits are set up on inputs A0 through A10 and latched onto the chip by the row-address strobe ($\overline{RAS}$). The ten column-address bits are set up on pins A0 through A9 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffer.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pullup resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation independent of the state of $\overline{OE}$. This permits early write operation to be completed with $\overline{OE}$ grounded.

data in/out (DQ0–DQ7)

The three-state output buffer provides direct TTL compatibility (no pullup resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle the output becomes valid after all access times are satisfied. The output remains valid while $\overline{CAS}$ and $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfying t_{OED}.

output enable ($\overline{OE}$)

$\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state, they will remain in the low-impedance state until either $\overline{OE}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every thirty-two milliseconds (256 ms for TMS417800P) to retain data. This can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh.

hidden refresh

Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ (CBR) refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ (see parameter t_{CSR}) and holding it low after $\overline{RAS}$ falls (see parameter t_{CHR}). For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally.

A low-power battery-backup refresh mode that requires less than 500 µA refresh current is available on the TMS417800P. Data integrity is maintained using $\overline{CAS}$-before-$\overline{RAS}$ refresh with a period of 125 µs while holding $\overline{RAS}$ low for less than 1 µs. To minimize current consumption, all input levels need to be at CMOS levels ($V_{IL} \leq 0.2$ V, $V_{IH} \geq V_{CC} - 0.2$ V).

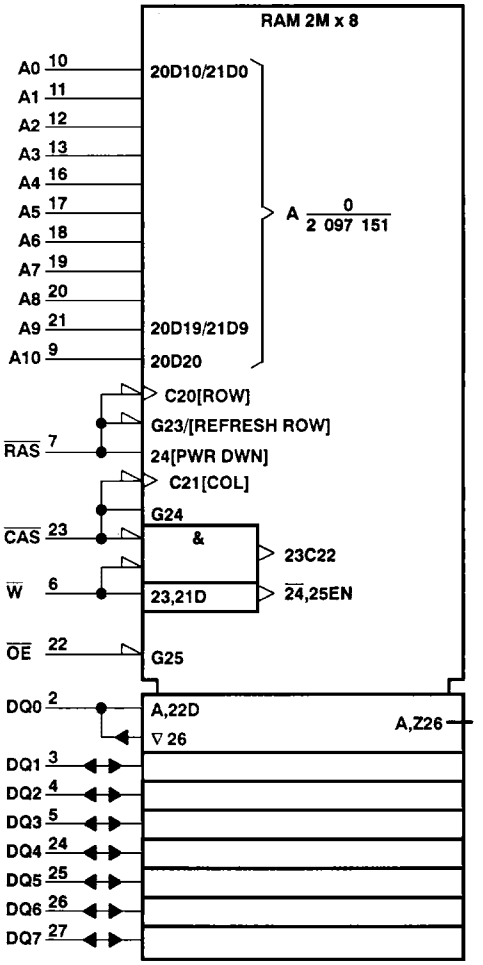
self refresh (TMS417800P)

The self-refresh mode is entered by dropping $\overline{CAS}$ low prior to $\overline{RAS}$ going low. Then $\overline{CAS}$ and $\overline{RAS}$ are both held low for a minimum of 100 µs. The chip is then refreshed by an on-board oscillator. No external address is required since the CBR counter is used to keep track of the address. To exit the self-refresh mode, both $\overline{RAS}$ and $\overline{CAS}$ are brought high to satisfy t_{CHS}. Upon exiting self-refresh mode, a burst refresh (refresh a full set of row addresses) must be executed before continuing with normal operation. The burst refresh ensures the DRAM is fully refreshed.

power up

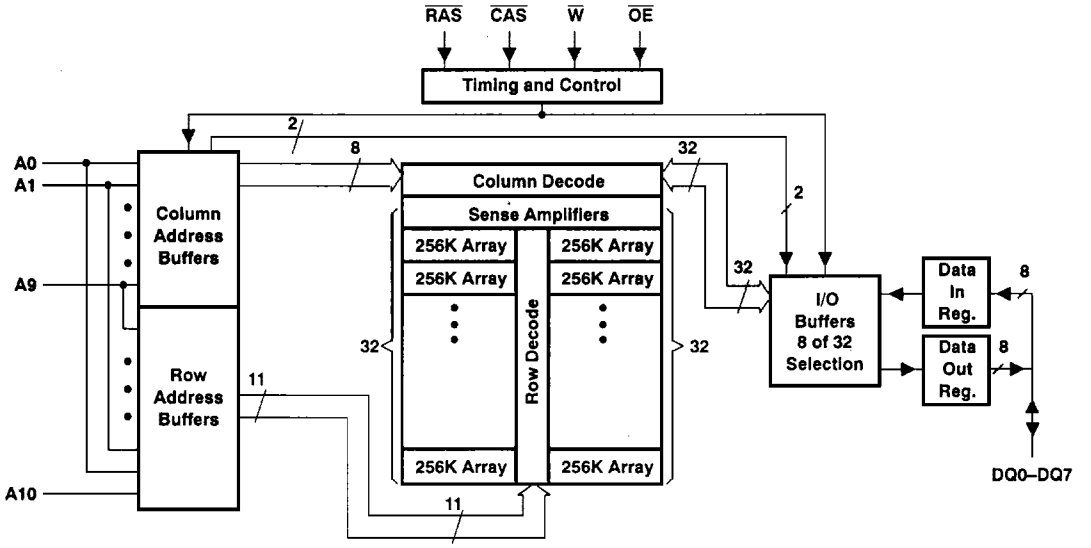
To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight $\overline{RAS}$ cycles is required after power-up to the full V_{CC} level.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
The pin numbers shown correspond to the DZ package.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Supply voltage range on V_{CC} . . . . . – 1 V to 7 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 55°C to 125°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

PRODUCT PREVIEW

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA		2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 to V_{CC}			± 10		± 10		± 10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, $\overline{CAS}$ high			± 10		± 10		± 10	µA
I_{CC1}†	Read or write cycle current (see Note 3)	V_{CC} = 5.5 V, Minimum cycle			125		115		105	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V (TTL)			2		2		2	mA
		V_{IH} = V_{CC} − 0.2 V (CMOS), After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high	'417800		1		1		1	mA
			'417800P		500		500		500	µA
I_{CC3}	Average refresh current ($\overline{RAS}$-only or CBR) (see Note 3)	V_{CC} = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high, ($\overline{RAS}$-only); $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)			125		115		105	mA
I_{CC4}†	Average page current (see Note 4)	V_{CC} = 5.5 V, t_{PC} = Minimum, $\overline{RAS}$ low, $\overline{CAS}$ cycling			125		115		105	mA
I_{CC10}‡	Battery backup operating current (equivalent refresh time is 256 ms) CBR only	t_{RC} = 125 µs, t_{RAS} ≤ 1 µs, V_{CC} − 0.2 V ≤ V_{IH} ≤ 6.5 V, 0 V ≤ V_{IL} ≤ 0.2 V, $\overline{W}$ and $\overline{OE}$ = V_{IH}, Address and Data stable			500		500		500	µA
I_{CC6}‡	Self refresh current	$\overline{CAS}$ ≤ 0.2 V, $\overline{RAS}$ < 0.2 V, Measured after t_{RASS} minimum			500		500		500	µA
I_{CC7}†	Standby current, outputs enabled	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL} Data out = Enabled			5		5		5	mA

† Measured with outputs open.
‡ For TMS417800P only.
NOTES: 3. Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}.
4. Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}.

PRODUCT PREVIEW

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz † (see Note 5)

PARAMETER		MIN	TYP	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs			5	pF
$C_{i(OE)}$	Input capacitance, output enable			7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs			7	pF
$C_{i(W)}$	Input capacitance, write-enable input			7	pF
C_O	Output capacitance			7	pF

NOTE 5: V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column-address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$ low		15		18		20	ns
t_{CPA}	Access time from column precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$ low		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$ low		15		18		20	ns
t_{CLZ}	$\overline{CAS}$ to output in low Z	0		0		0		ns
t_{OH}	Output disable time, start of $\overline{CAS}$ high	3		3		3		ns
t_{OHO}	Output disable time, start of $\overline{OE}$ high	3		3		3		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (see Note 6)	0	15	0	18	0	20	ns
t_{OEZ}	Output disable time after $\overline{OE}$ high (see Note 6)	0	15	0	18	0	20	ns

NOTE 6: t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Random read or write cycle (see Note 7)	110		130		150		ns
t_{RWC}	Read-modify-write cycle time	155		181		205		ns
t_{PC}	Page-mode read or write cycle time (see Note 8)	40		45		50		ns
t_{PRWC}	Page-mode read-modify-write cycle time	85		96		105		ns
t_{RASP}	Page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 9)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ low (see Note 10)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ high ($\overline{CAS}$ precharge)	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ high ($\overline{RAS}$ precharge)	40		50		60		ns
t_{WP}	Write pulse duration	15		15		15		ns
t_{ASC}	Column-address setup time before $\overline{CAS}$ low	0		0		0		ns
t_{ASR}	Row-address setup time before $\overline{RAS}$ low	0		0		0		ns
t_{DS}	Data setup time (see Note 11)	0		0		0		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low	0		0		0		ns
t_{CWL}	$\overline{W}$-low setup time before $\overline{CAS}$ high	15		18		20		ns
t_{RWL}	$\overline{W}$-low setup time before $\overline{RAS}$ high	15		18		20		ns
t_{WCS}	$\overline{W}$-low setup time before $\overline{CAS}$ low (Early write operation only)	0		0		0		ns

NOTES: 7. All cycle times assume t_T = 5 ns.
8. To assure t_{PC} min, t_{ASC} should be greater than or equal to t_{CP}.
9. In a read-modify-write cycle, t_{RWD} and t_{RWL} must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time (t_{RAS}).
10. In a read-modify-write cycle, t_{CWD} and t_{CWL} must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time (t_{CAS}).
11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

PARAMETER		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CAH}	Column-address hold time after $\overline{CAS}$ low	10		15		15		ns
t_{DH}	Data hold time (see Note 11)	10		15		15		ns
t_{RAH}	Row-address hold time after $\overline{RAS}$ low	10		10		10		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high (see Note 12)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high (see Note 12)	5		5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low (Early write operation only)	15		15		15		ns
t_{AWD}	Delay time, column address to $\overline{W}$ low (Read-modify-write operation only)	55		63		70		ns
t_{CHR}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	20		20		20		ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	60		70		80		ns
t_{CSR}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low ($\overline{CAS}$-before-$\overline{RAS}$ refresh only)	10		10		10		ns
t_{CWD}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	40		46		50		ns
t_{OEH}	$\overline{OE}$ command hold time	15		18		20		ns
t_{OED}	$\overline{OE}$ to data delay	15		18		20		ns
t_{ROH}	$\overline{RAS}$ hold time referenced to $\overline{OE}$	10		10		10		ns
t_{RAD}	Delay time, $\overline{RAS}$ low to column-address (see Note 13)	15	30	15	35	15	40	ns
t_{RAL}	Delay time, column-address to $\overline{RAS}$ high	30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ high	30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 13)	20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low	0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (Read-modify-write operation only)	85		98		110		ns
t_{CPW}	Delay time, $\overline{W}$ from $\overline{CAS}$ precharge	60		68		75		ns
t_{CPRH}	Hold time, $\overline{RAS}$ from $\overline{CAS}$ precharge	35		40		45		ns

NOTES: 11. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Either t_{RRH} or T_{RCH} must be satisfied for a read cycle.
13. The maximum value is specified only to assure access time.

PRODUCT PREVIEW

timing requirements over recommended ranges of supply voltage and operating free-air temperature (concluded)

PARAMETER		TMS417800-60 TMS417800P-60		TMS417800-70 TMS417800P-70		TMS417800-80 TMS417800P-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{CPR}	$\overline{CAS}$ precharge before self refresh	0		0		0		ns
t_{RPS}	$\overline{RAS}$ precharge after self refresh	110		130		150		ns
t_{RASS}	Self refresh entry from $\overline{RAS}$ low	100		100		100		µs
t_{CHS}	$\overline{CAS}$ low hold time after $\overline{RAS}$ high (self-refresh)	– 50		– 50		– 50		ns
t_{REF}	Refresh time interval (TMS417800)		32		32		32	ms
t_{REF}	Refresh time interval Low power (TMS417800P only)		256		256		256	ms
t_T	Transition time	3	30	3	30	3	30	ns

PARAMETER MEASUREMENT INFORMATION

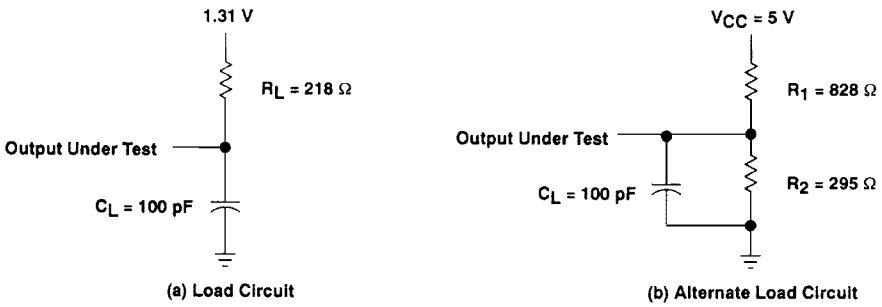


Figure 1. Load Circuits for Timing Parameters

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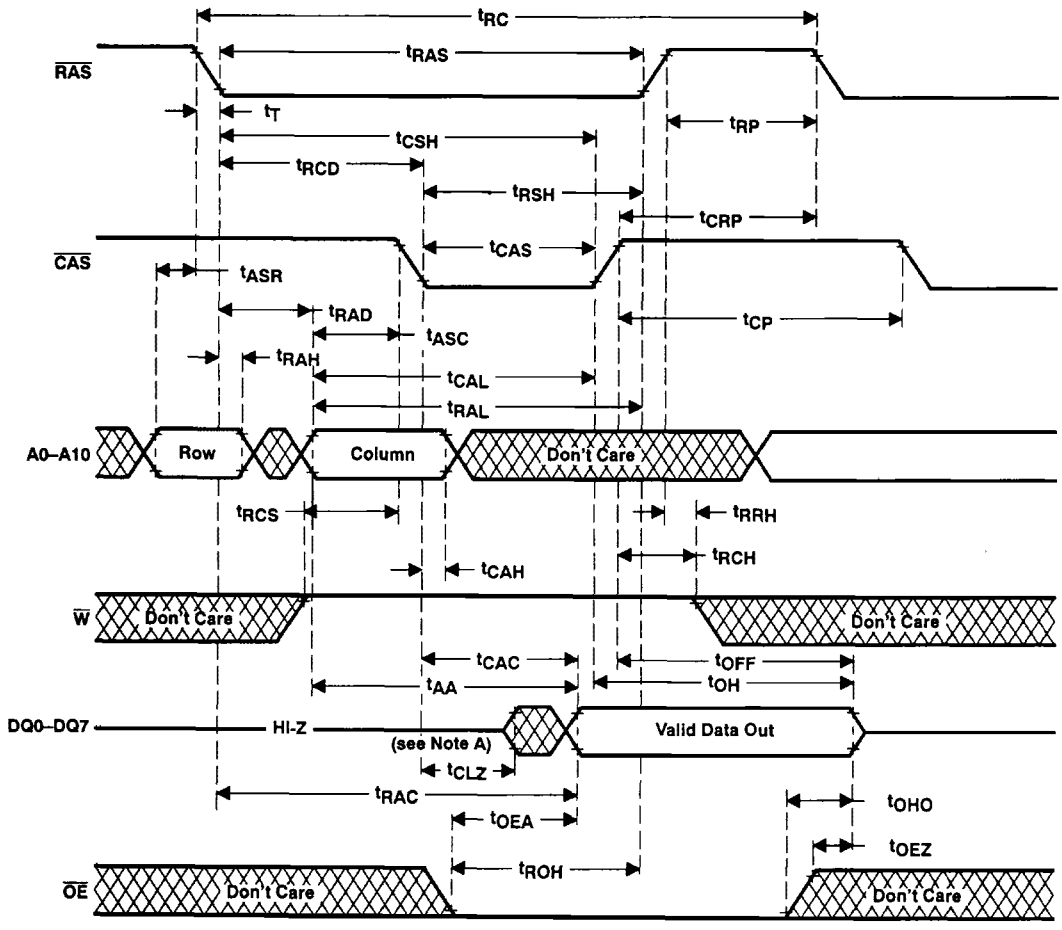
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 2. Read Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

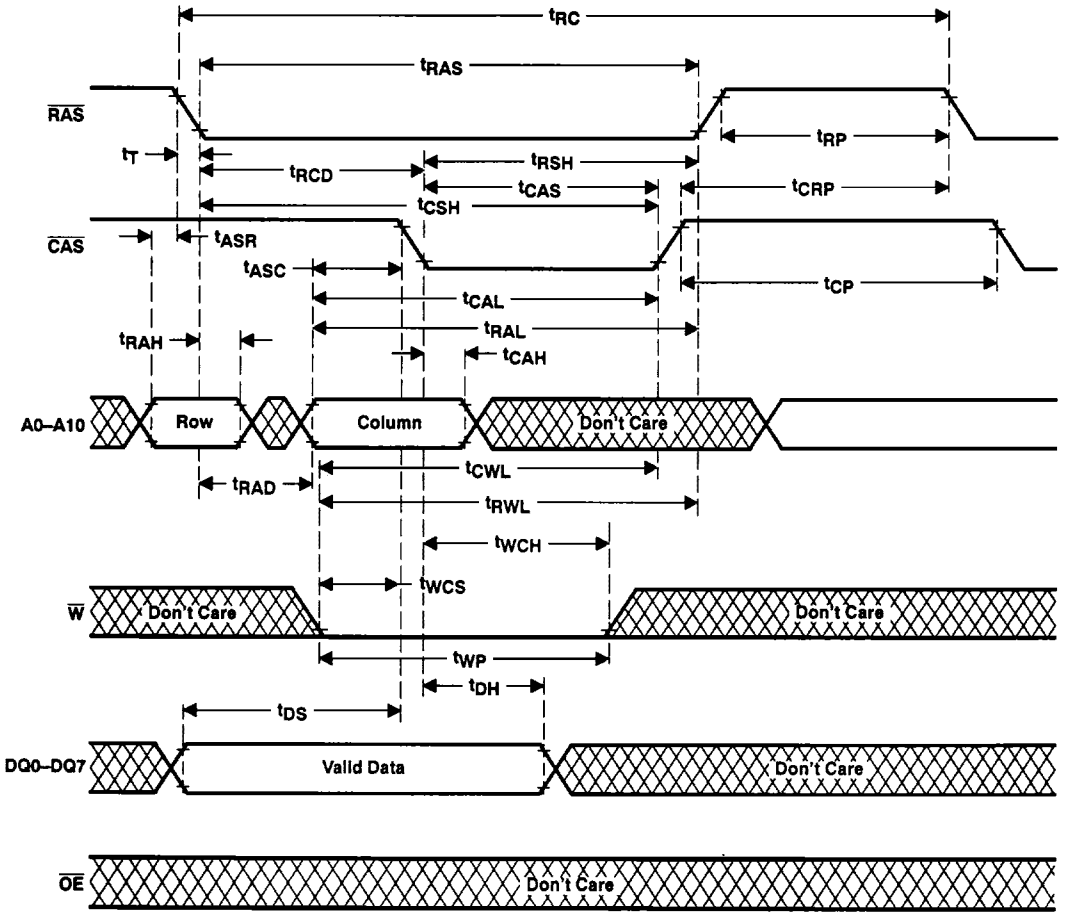
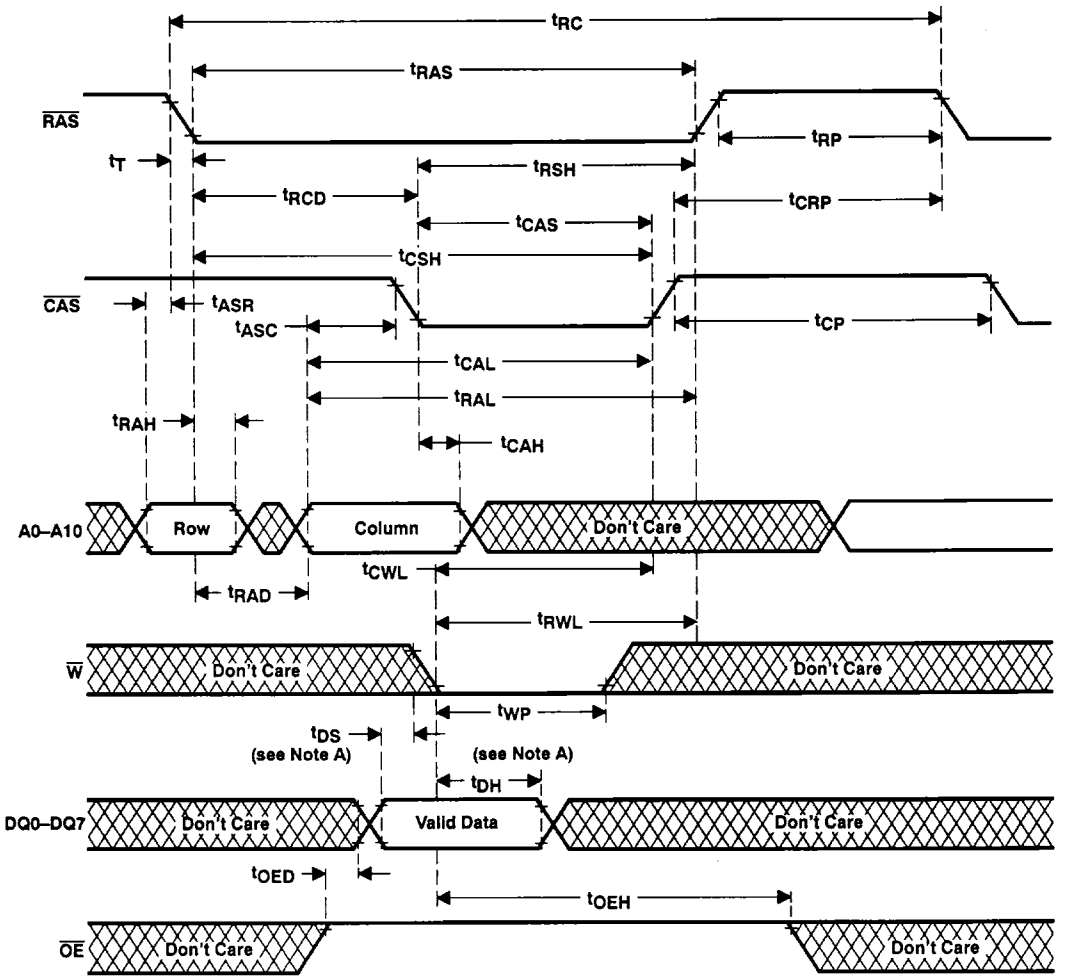


Figure 3. Early Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

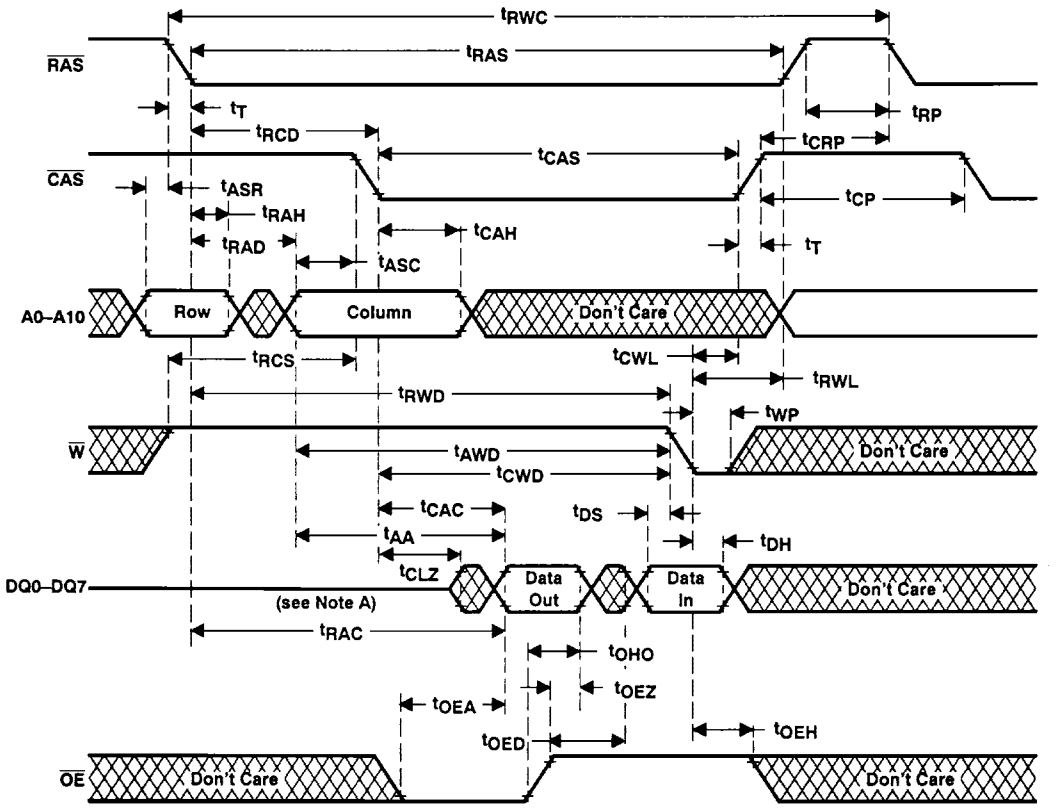


NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 4. Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

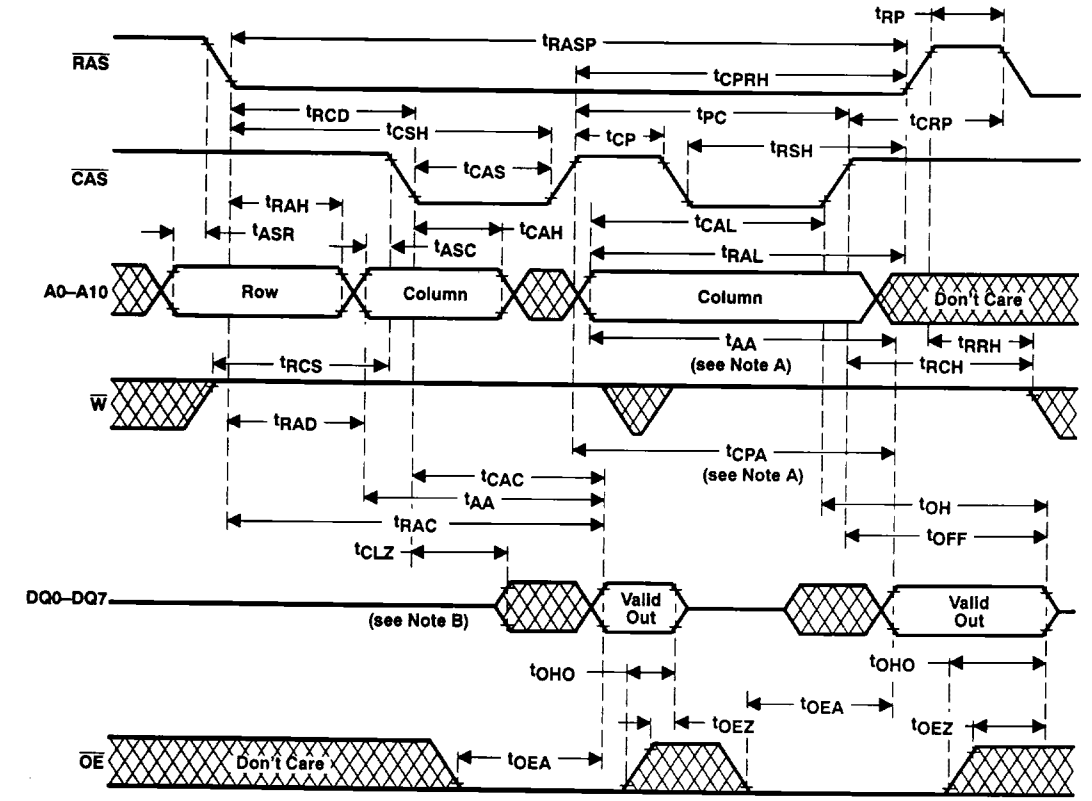


NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 5. Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

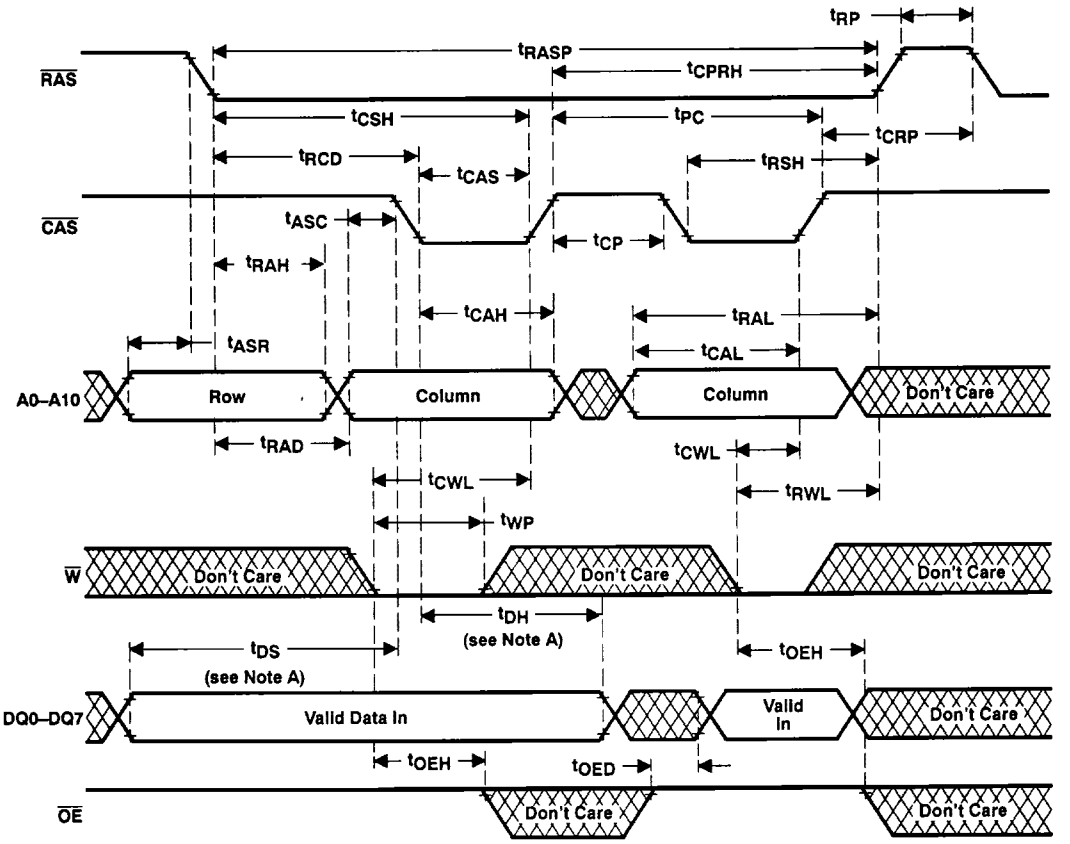


NOTES: A. Access time is t_{CPA} or t_{AA} dependent.
B. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
C. A write cycle or read-modify-write cycle can be intermixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.

Figure 6. Enhanced Page-Mode Read Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

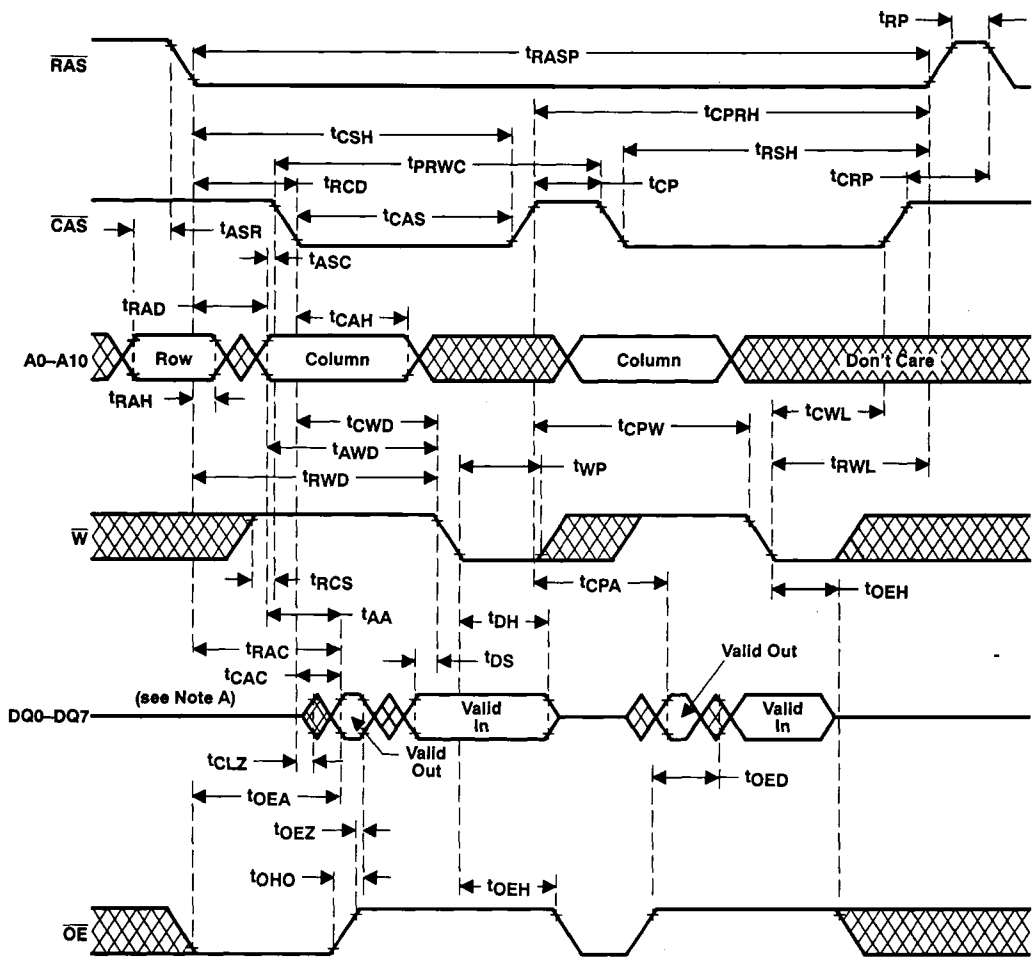


NOTES: A. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.
B. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.

Figure 7. Enhanced Page-Mode Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output may go from a high-impedance state to an invalid data state prior to the specified access time.
B. A read or write cycle can be intermixed with read-modify-write cycles as long as the read and write timing specifications are not violated.

Figure 8. Enhanced Page-Mode Read-Modify-Write Cycle Timing

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

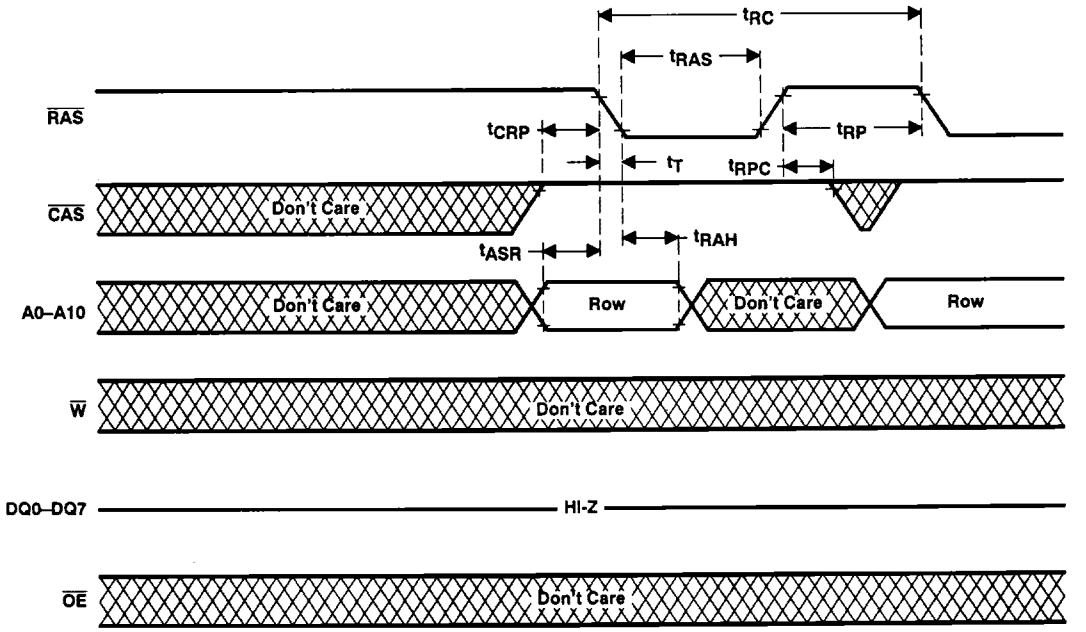


Figure 9. RAS-Only Refresh Timing

PARAMETER MEASUREMENT INFORMATION

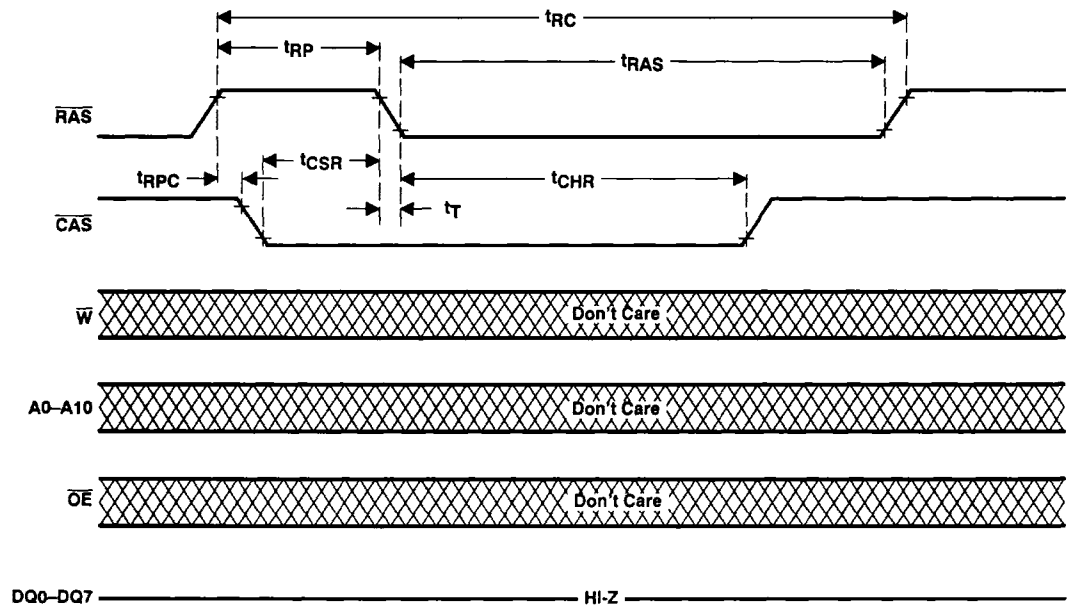
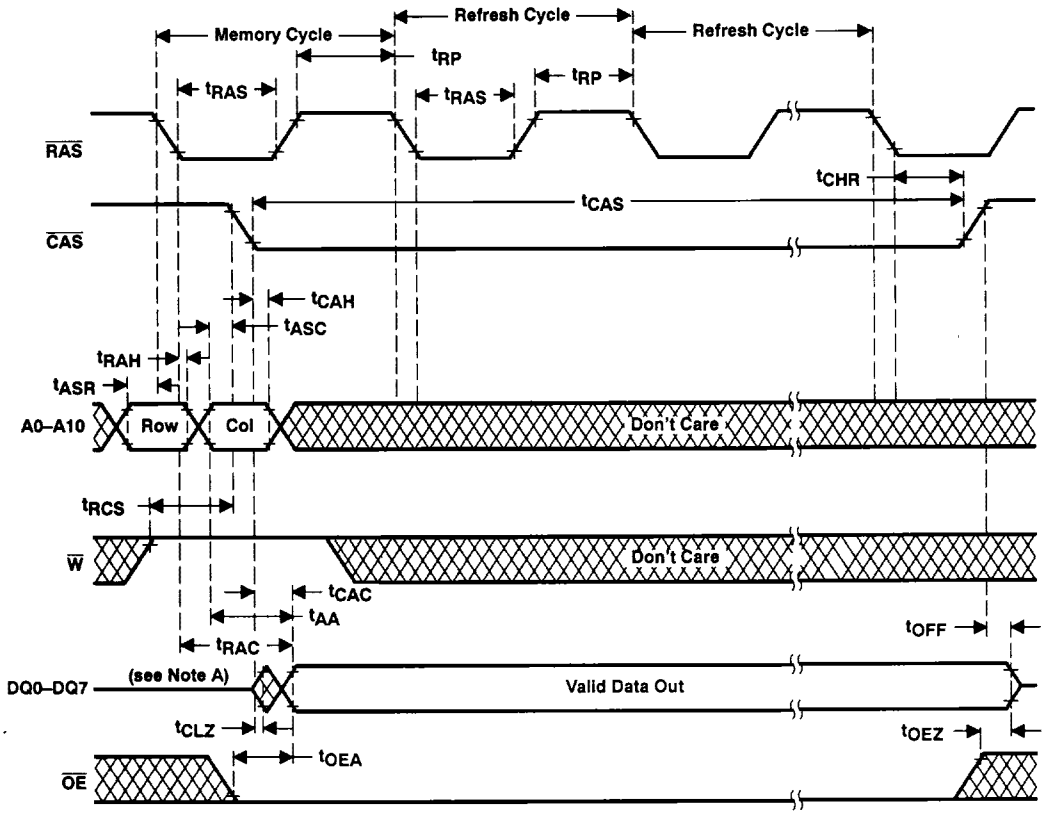


Figure 10. Automatic ($\overline{CAS}$-Before-$\overline{RAS}$) Refresh Cycle Timing

PRODUCT PREVIEW

PRODUCT PREVIEW

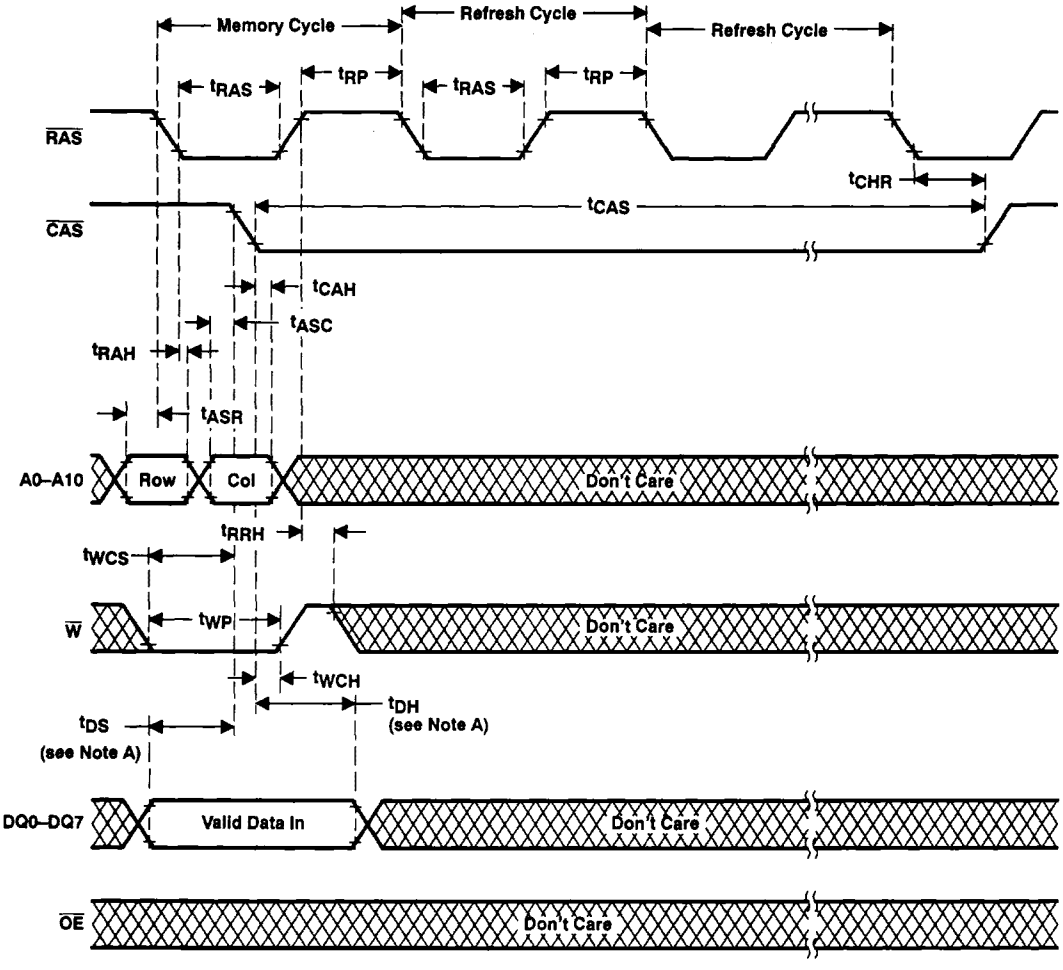
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output may go from a high-impedance state to an invalid data state prior to the specified access time.

Figure 11. Hidden Refresh Cycle (Read)

PARAMETER MEASUREMENT INFORMATION



NOTE A: Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations.

Figure 12. Hidden Refresh Cycle (Write)

PRODUCT PREVIEW

PARAMETER MEASUREMENT INFORMATION

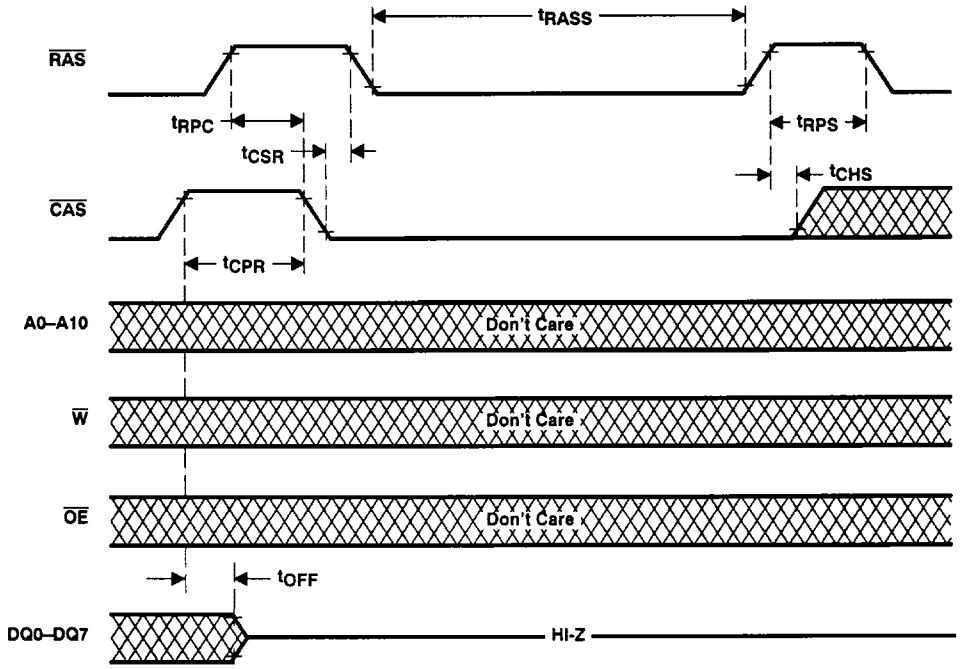
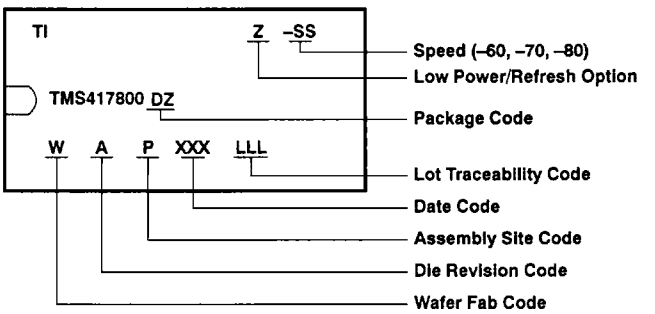


Figure 13. Self Refresh Timing

device symbolization



PRODUCT PREVIEW