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SSI 32D5362A
Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

November 1991

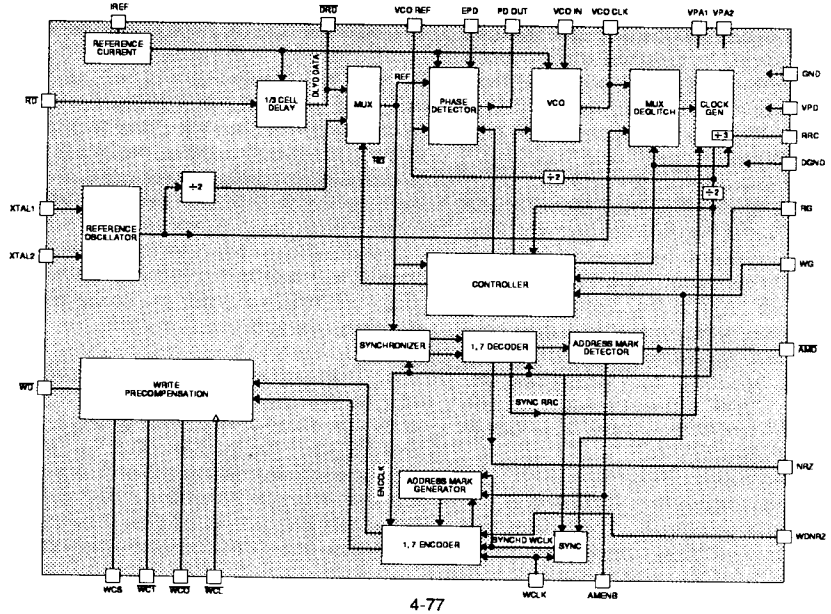
DESCRIPTION

The SSI 32D5362A Data Synchronizer/1, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 1, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D5362A has been optimized for operation as a companion device to the SSI 32C9000 controller. The VCO frequency setting elements are incorporated within the SSI 32D5362A for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5362A utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/3 cell delay or external devices. The SSI 32D5362A requires a single +5V supply.

FEATURES

- **Data Synchronizer and 1, 7 RLL ENDEC**
- **10 to 20 Mbit/s operation**
  - **Data Rate programmed with a single external resistor or current source**
- **Optimized for operation with the SSI 32C9000 controller.**
- **Fast acquisition phase lock loop**
  - **Zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Crystal controlled reference oscillator**
- **+5V operation**
- **28-pin PLCC package**
- **Test outputs - Allow drive margin testing with available test chip**

BLOCK DIAGRAM



OPERATION

The SSI 32D5362A is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1,7 RLL encoding format. In the Read Mode the SSI32D5362A performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect, and Data Decoding. In the Write Mode, the SSI 32D5362A converts NRZ data into the 1,7 RLL format described in Table 1, performs Write Precompensation, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D5362A have been optimized for use as a companion device to the SSI 32C9000 controller.

The SSI 32D5362A can operate with data rates ranging from 10 to 20 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = \frac{92.6}{DR} - 2.3(k\Omega)$$

where: DR = Data Rate in Mbit/s.

An internal crystal reference oscillator, operating at three times the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at three times the Data Rate. If a crystal oscillator is not desired, then an AC coupled ECL source may be applied to XTAL1, leaving XTAL2 open. A TTL compatible reference may also be used if suitably attenuated and AC coupled.

The SSI 32D5362A employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DYLD DATA pulse. In the Write and Idle modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE (RG), and WRITE GATE (WG) inputs control the device mode.

RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

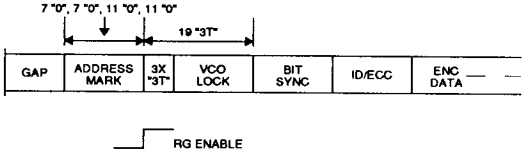
In the Read Mode the falling edge of $\overline{DRD}$ enables the Phase Detector while the rising edge is phase compared to the rising edge of the VCO/2. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO/2 clock. By utilizing a fully integrated symmetrical VCO running at three times the data rate, the decode window is insured to be accurate and centered symmetrically about the rising edges of $\overline{DRD}$. The accuracy of the 1/3 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner the acquisition time is substantially reduced.

After Read Mode is terminated (RG low), the VCO and RRC sources switch from $\overline{RD}$ and VCO/3, respectively, to the reference crystal. After a delay of one NRZ bit time (minimum) from when RG is low, write gate (WG) may be enabled (see figure 7 for timing diagram). NRZ is a tri-statable pin controlled by RG. NRZ will change states within one NRZ bit time. The NRZ pin can be connected to WDNRZ to form a bi-directional port.

SOFT SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Soft Sector Operation



ADDRESS MARK DETECT

In Soft Sector Read Operation the SSI 32D5362A must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark for the SSI 32D5362A consists of two (2) 7 "0" patterns followed by two 11 "0" patterns. To begin the read lock sequence the Address Mark Enable (AMENB) is asserted high by the controller. The SSI 32D5362A Address Mark Detect ($\overline{AMD}$) circuitry then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0's" within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0's." If $\overline{AMD}$ does not detect 9 "0's" within 5 $\overline{RD}$ bits after detecting 6 "0's" it will restart the Address Mark Detect sequence and look for 6 "0's." When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence the $\overline{AMD}$ transitions low disabling AMENB input. When AMENB is released, $\overline{AMD}$ will be released and reset by the SSI 32D5362A. The AMENB should be released prior to entering Read Mode.

PREAMBLE SEARCH

After the Address Mark (AM) has been detected, Read Gate (RG) can be asserted initiating the remainder of the read lock sequence. When RG is asserted an internal counter counts negative transitions of the incoming Read Data ($\overline{RD}$) looking for (3) consecutive 3T preamble. Once the counter reaches count 3 (finds (3) consecutive negative transistors) the internal read gate switches the phase detector input from the reference oscillator to the Delayed Read Data ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the Delayed Read Data. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

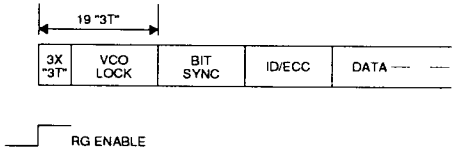
VCO LOCK & BIT SYNC ENABLE

When the internal counter counts 16 more negative transitions or a total of 19 "3T's" from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at the count of 19, the RRC source switches from the reference oscillator to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. The bit sync circuitry searches for a '1001001' pattern to align the proper decode boundaries. During this time, an RRC pulse may be stretched a maximum of 2 RRC time periods during the alignment process to prevent any glitches.

HARD SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Hard Sector Operation

In hard sector operation a low AMENB disables the SSI 32D5362A's Address Mark Detection circuitry and



$\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with the exception of the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the SSI 32D5362A converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. The SSI 32D5362A can operate with a soft or hard sector hard drive.

Serial NRZ data is clocked into the SSI 32D5362A and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In SCSI or IDE operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for intersymbol interference caused by media bit shift. The SSI 32D5362A recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external RC network on the WCS pin where the capacitor is connected from WCS to VPA1 and the resistor is connected from WCS to AGND. The equations is:

$$TPC = 0.053(Rc)(Cc + Cs)$$

When the write precompensation control latch, $\overline{WCL}$ is low, the SSI 32D5362A performs write precompensation according to the algorithm outlined in Table 4.

SOFT SECTOR

In soft sector operation, when Write Gate (WG) is asserted, the NRZ input (WDNRZ) must be kept low. To generate an Address Mark (consisting of 7 "0's", 7 "0's", 11 "0's", 11 "0's") the Address Mark Enable (AMENB) is toggled high for a minimum of 1 NRZ bit time. The toggling of AMENB must occur at least 1 NRZ bit time after WG is asserted. After the address mark is generated, WDNRZ must be kept low for an additional 44 NRZ bits to properly generate 19 x '3T' for the preamble plus three '3T' for the bit sync field. Data can then be written on the WDNRZ line with the encode data appearing on $\overline{WD}$ 5 NRZ bit times later. After writing is complete, WG should be held high for an additional 5 NRZ bit times to ensure that the encoder is flushed. See figure 9 for timing diagram.

HARD SECTOR

After WG is asserted, WDNRZ must be kept low for a minimum of 44 NRZ bit times to ensure a preamble field of at least 19 x "3T" plus 3 x "3T" for the bit sync field. Data can then be written as in the soft sector operation.

TEST POINTS

The SSI 32D5362A provides three (3) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{DRD}$, delayed read data – the positive edges represent the data bit position

(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder

(c) VCO CLK, the VCO clock output which represents the output of the VCO

The following figure describes the relationship between the various test points:

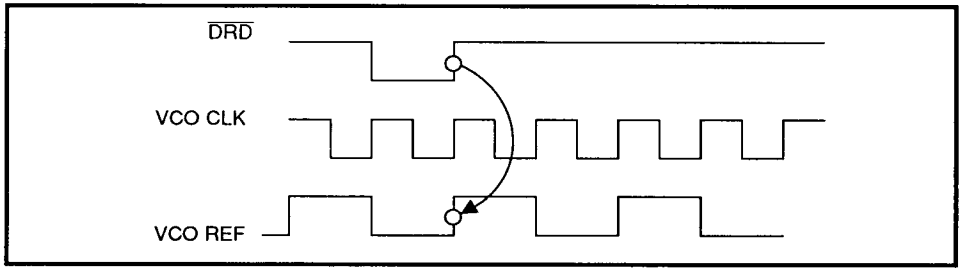


FIGURE 1: Test Point Relationships

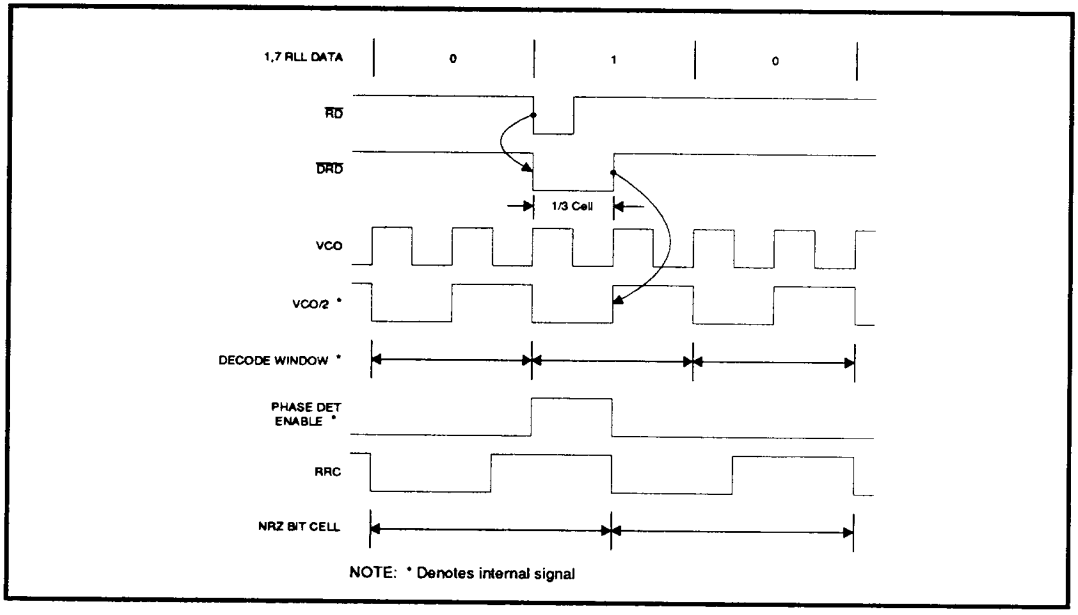


FIGURE 2: Data Synchronization Waveform

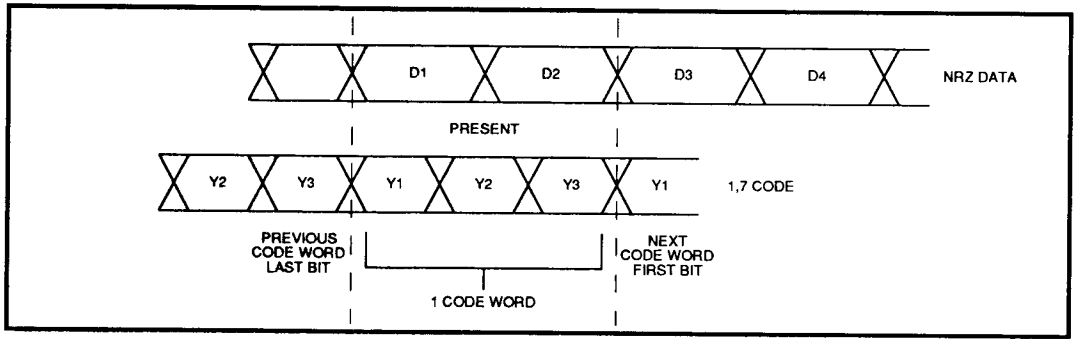


FIGURE 3: NRZ Data Word Comparision to 1, 7 Code Word
(See Tables 1, and 2 for Decode Scheme)

TABLE 1: Decode Table for (1, 7) RLL Code Set

ENCODED READ DATA			DECODED DATA
Previous	Present	Next	
Y Y	Y Y Y	Y Y Y	D D
2' 3'	1 2 3	1 2 3	1 2
0 0	0 0 0	X X X	0 1
1 0	0 0 0	X X X	0 0
0 1	0 0 0	X X X	0 1
X X	1 0 0	X X X	1 1
X 0	0 1 0	0 0	1 1
X 0	0 1 0	1 0	1 0
X 0	0 1 0	0 1	1 0
X 1	0 1 0	0 0	0 1
X 1	0 1 0	1 0	0 0
X 1	0 1 0	0 1	0 0
0 0	0 0 1	X X	0 1
1 0	0 0 1	X X	0 0
0 1	0 0 1	X X	0 0 (Preamble)
X X	1 0 1	X X	1 0

TABLE 2: Encode Table for (1, 7) RLL Code Set

NRZ DATA				ENCODED WRITE DATA			
Present		Next		Previous	Present		
D	D	D	D	Y	Y	Y	Y
1	2	3	4	3	1	2	3
0	0	0	X	X	0	0	1
0	0	1	X	0	0	0	0
0	0	1	X	1	0	1	0
1	0	0	X	0	1	0	1
1	0	1	X	0	0	1	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

NOTE: X = Don't Care

TABLE 3: Clock Frequency

WG	RG	VCO REF	RRC	DECCLK	ENCCLK	MODE
0	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	IDLE
0	1	$\overline{RD}$	VCO/3	VCO/2	XTAL/2	READ
1	0	XTAL/2	XTAL/3	XTAL/2	XTAL/2	WRITE
1	1	XTAL/2	XTAL/3	XTAL/2	XTAL/2	ILLEGAL

Note 1: Until the VCO locks to the new source, the VCO/2 entries will be XTAL/2.

2: Until the VCO locks to the new source, the VCO/3 entries will be XTAL/3.

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TABLE 4: Write Precompensation Algorithm

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

TABLE 5: Write Precompensation Magnitude

$\overline{WCI}$	$\overline{WCO}$	MAGNITUDE.WP
0	0	3
0	1	2
1	0	1
1	1	0

The nominal magnitude,
(TPC = WP x 0.053 (Rc) (Cc+Cs), is externally set with an R-C network on pin WCS.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RD}$	I	READ DATA: Encoded Read Data from the disk drive read channel, active low.
RG	I	READ GATE: Selects the PLL reference input (REF), see Table 1. A change in state on RG initiates the PLL synchronization sequence.
WG	I	WRITE GATE: Enables the write mode, see Table 2.
WCLK	I	WRITE CLOCK: Write Clock input. Must be synchronous with the NRZ Write Data input. For small cable delays, WCLK may be connected directly to pin RRC.
EPD	I	ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector. This opens the PLL and the VCO will run at the frequency commanded by the voltage on pin VCO IN. Pin EPD has an internal resistor pull up.
AMENB	I	ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry, active high.
$\overline{WC0}$, $\overline{WC1}$	I	WRITE PRECOMPENSATION CONTROL BITS: Pins $\overline{WC1}$, and $\overline{WC0}$ control the magnitude of the write precompensation, see Table 4. Internal resistor pull ups are provided.
$\overline{WCL}$	I	WRITE PRECOMPENSATION CONTROL LATCH: Used to latch the write precompensation control bits $\overline{WC1}$ and $\overline{WC0}$ into the internal DAC. An active low level latches the input bits. Pin $\overline{WCL}$ has an internal resistor pull up.
WDNRZ	I	NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ pin to form a bidirectional data port.

OUTPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{WD}$	O	WRITE DATA: Encoded write data output, active low. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to one edge of the XTAL 1 input clock.
RRC	O	READ/REFERENCE CLOCK: A multiplexed clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than two lost clock pulses will occur. When RG goes high, RRC is synchronized to the NRZ Read Data after 19 read data pulses.
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is high or AMENB is low. A latched low level output indicates that an address mark has been detected. A low level on pin AMENB resets pin $\overline{AMD}$.

OUTPUT PINS (Continued)

NAME	TYPE	DESCRIPTION
VCO REF	O	VCO REFERENCE: An open emitter ECL output test point. The VCO reference input to the phase detector, the negative edges are phase locked to DLYD DATA. The positive edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to perform this test, they should be removed during normal operation for reduced power dissipation.
VCO CLK	O	VCO CLOCK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
$\overline{\text{DRD}}$	O	DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this open emitter output signal indicates the data bit position. The positive edges of the $\overline{\text{DRD}}$ and the VCO REF signals can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit shift. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
NRZ	O	NRZ READ DATA OUTPUT: Tristate output pin that is enabled when read gate is high. This pin can be connected to the WDNRZ pin to form a bidirectional data port.

ANALOG PINS

NAME	TYPE	DESCRIPTION
IREF	I	TIMING PROGRAM PIN: The VCO center frequency and the 1/3 cell delay are a function of the current sourced into pin IREF.
XTAL1, 2	I	CRYSTAL OSCILLATOR CONNECTIONS: The pin frequency is at three times the data rate. If the crystal oscillator is used, an AC coupled parallel LC circuit must be connected from XTAL1 to ground. If the crystal oscillator is not desired, XTAL1 may be driven by a TTL source with XTAL2 open. The source duty cycle should be close to 50% as possible since its duty cycle will affect the RRC clock duty cycle when XTAL is its source. The additional RRC duty cycle error will be one third the source duty cycle error.
PD OUT	O	PHASE DETECTOR OUTPUT: Drives the loop filter input.
VCO IN	I	VCO CONTROL INPUT: Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET: Pin for RC network to program write precompensation magnitude value. C_P to VPA1, R_P to AGND.
DGND, AGND	I	Digital and Analog Ground
VPA1, VPA2	I	Analog +5V Supplies
VPD	I	Digital +5V Supply

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING	UNIT
Storage Temperature	-65 to + 150	°C
Junction Operating Temperature, Tj	0 to +130	°C
Supply Voltage, VPA1, VPA2, VPD	-0.5 to 7	V
Voltage Applied to Logic Inputs	-0.5 to VPD + 0.5	V
Maximum Power Dissipation	1.1	W

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING	UNIT
Supply Voltage, VPA1 = VPA2 = VPD = VCC	4.75 < VCC < 5.25	V
Ambient Operating Temperature, TA	0 < TA < +70	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75V< VCC <5.25V, 10 MHz< 1/TORC <20 MHz, 30 MHz< 1/TVCO <60 MHz, TA = 0°C to 70°C

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage		2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			2.0	µA
IIL	Low Level Input Current	VIL = 0.4V			-1.5	mA
VOH	High Level Output Voltage	IOH = 400 µA	2.4			V
VOL	Low Level Output Voltage	IOL = 4 mA			0.5	V
ICC	Power Supply Current	All outputs open,*		170	190	mA
PWR	Power Dissipation	Test point* pins open		0.85	1.0	W

* WG, RG ***CANNOT*** both be high

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOHT*	Test Point Output High Level $\overline{DRD}$, VCO CLK, VCO REF	262Ω to VPD 402Ω to GND VPD = 5.0V VOHT - VPD		-0.85		V
VOLT*	Test Point Output Low Level $\overline{DRD}$, VCO CLK, VCO REF	262Ω to VPD 402Ω to GND VPD = 5.0V VOLT - VPD		-1.75		V

* Monitor points only - Not tested

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DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 3)

TRD	Read Data Pulse Width	Measured at 1.5V	15		TORC-20	ns
RRC	Duty Cycle	Measured at 1.5V, 15 Mbit/s	43		57	%
TFRD	Read Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			15	ns
TRRC	Read Clock Rise Time	0.8V to 2.0V, $C_L \leq 15$ pF			8	ns
TFNRZ	NRZ Fall Time	0.8V to 2.0V, $C_L \leq 15$ pF			8	ns
TRNRZ	NRZ Rise Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
TFRC	Read Clock Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			5	ns
TPNRZ	NRZ (out) Set Up/Hold Time		0.31 TORC			ns
Decode Window Centering Accuracy					±1.5	ns
Decode Window			(2TORC/3) - 3			ns

WRITE MODE (See Figure 4)

TWD	Write Data Pulse Width	$C_L \leq 15$ pF	See Note 1		See Note 2	ns
TFWD	Write Data Fall Time	2.0V to 0.8V, $C_L \leq 15$ pF			8	ns
TRWC**	Write Data Clock Rise Time	0.8V to 2.0V			10	ns
TFWC**	Write Data Clock Fall Time	2.0V to 0.8V			8	ns
TSNRZ	WDNRZ Set up Time		5			ns
THNRZ	WDNRZ Hold Time		5			ns

Note 1: $\frac{2}{3}TOWC - 5 - 4.76TPCO - TPC$ Note 2: $\frac{2}{3}TOWC + 10 - 4.76TPCO - TPC$

** **INPUT** requirement - Not tested

WRITE MODE (Continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TPC	Precompensation Time Shift Magnitude Accuracy	TPCO=0.053 (Cc+Cs) (Rc) Rc=1k to 2k; Cc + Cs = 25pF to 40 pF; Cs=stray capacity				
		$\overline{WC0}$ = 1 $\overline{WC1}$ = 1		0		ns
		$\overline{WC0}$ = 0 $\overline{WC1}$ = 1		TPCO		ns
		$\overline{WC0}$ = 1 $\overline{WC1}$ = 0		(2)TPCO		ns
		$\overline{WC0}$ = 0 $\overline{WC1}$ = 0		(3)TPCO		ns

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCC = 5.0V, VCO_IN = 2.7V TO = 3.6 (RR + 2.3) TO (ns); RR (kΩ) RR = 2.3k to 7.0k	0.85 TO		1.15 TO	ns
	VCO Frequency Dynamic Range	1V ≤ VCO_IN ≤ VCC-0.6V	±20		±40	%
KVCO	VCO Control Gain	ωo = 2π/TVCO 1V ≤ VCO IN ≤ VCC 0.6V	0.12 ωo		0.24 ωo	rad/s-V
KD*	Phase Detector Gain	KD = 570/ (RR + 0.53) KD(μA/rad), RR (kΩ), PLL REF = $\overline{RD}$, 1T pattern	0.83 KD		1.17 KD	μA/rad
*KVCO •	KD Product Accuracy		-28		-28	%
TD	1/3 Cell Delay	TD0 = 5.05 (RR + 0.530) RR = kΩ	0.8TD0		1.2TD0	ns
*VCO	Phase Restart Error			6		ns

CONTROL CHARACTERISTICS (See Figure 5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TSWS	$\overline{WC0}$, $\overline{WC1}$ SET UP TIME		50			ns
THWS	$\overline{WC0}$, $\overline{WC1}$ HOLD TIME		0			ns

* Indirectly tested

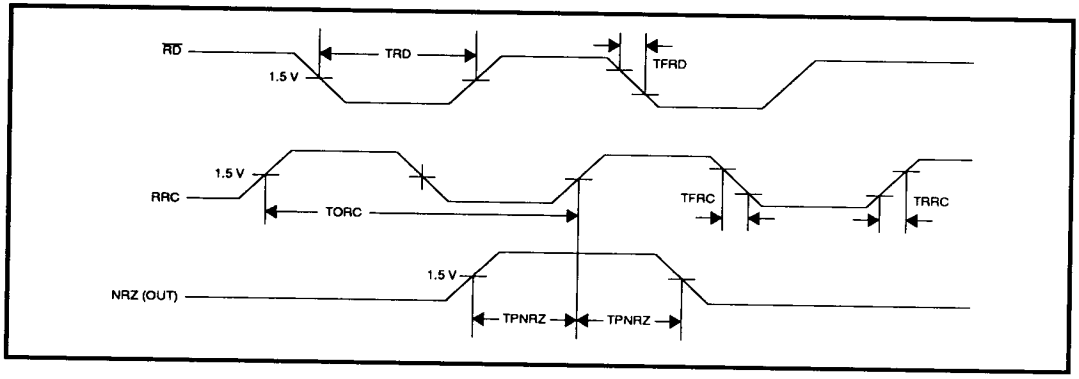


FIGURE 3: Read Timing

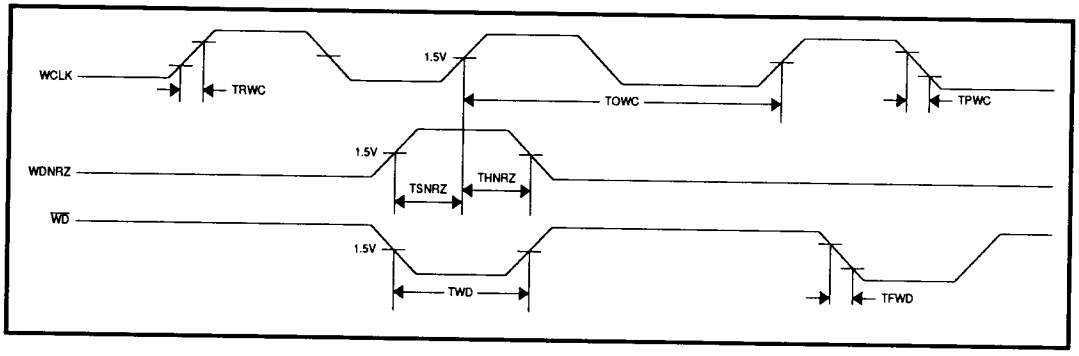


FIGURE 4: Write Timing

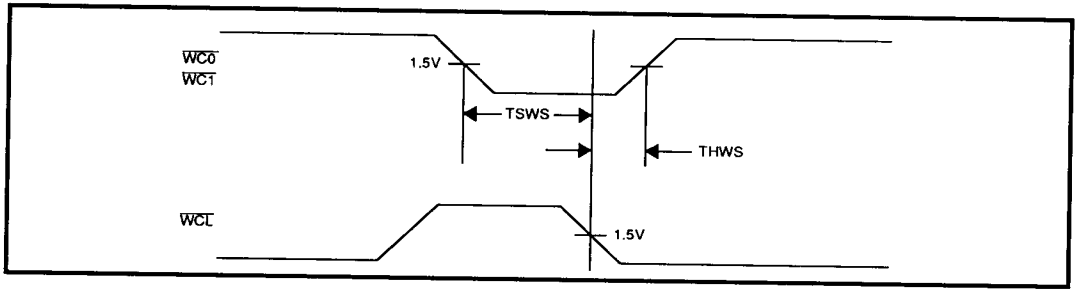


FIGURE 5: Control Timing

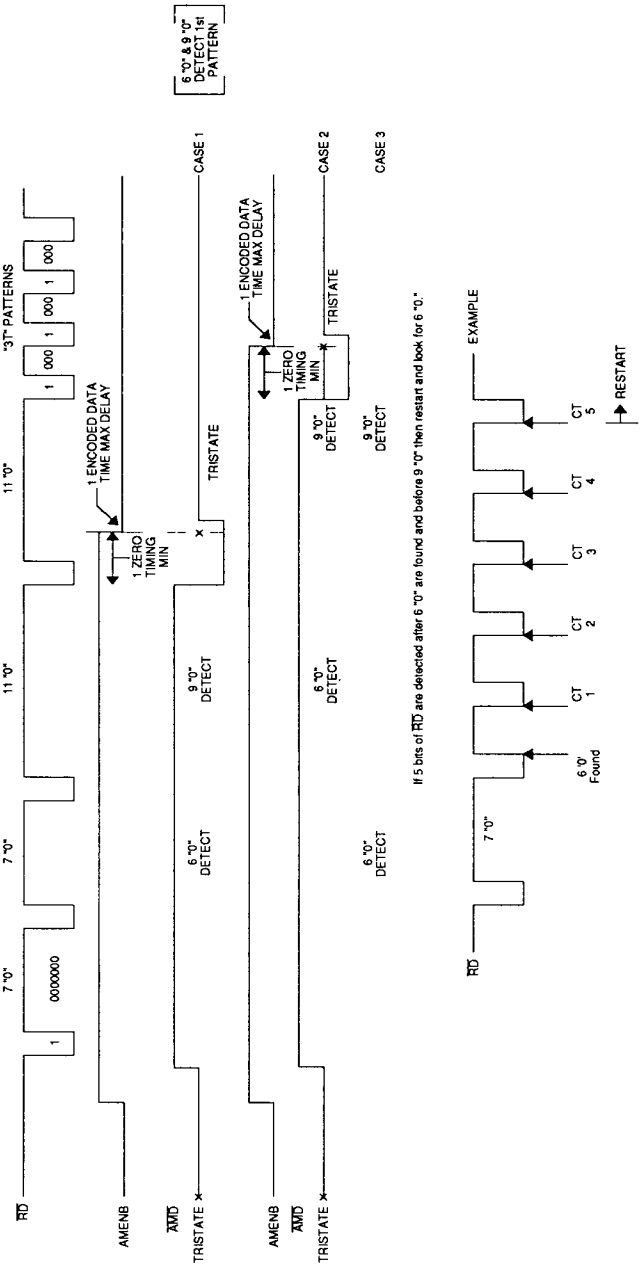


FIGURE 6: Address Mark Search

1191- rev.

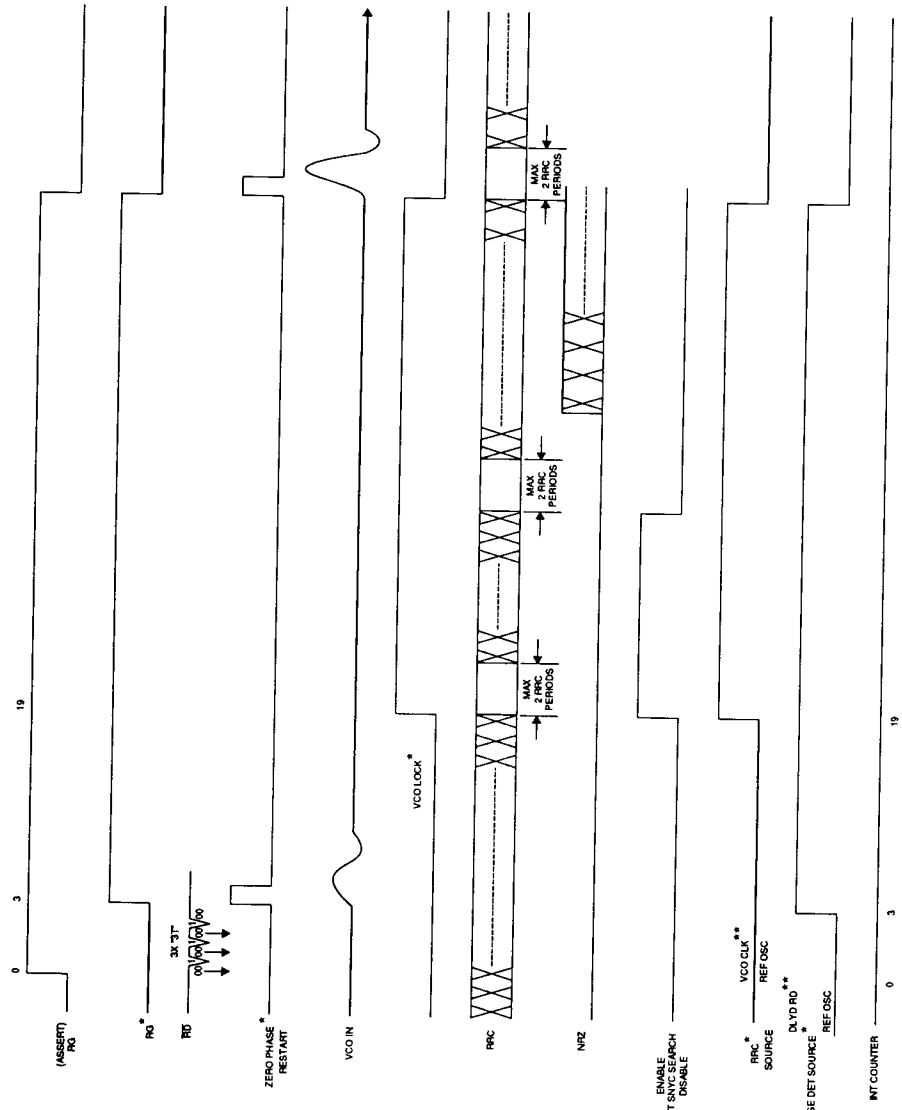


FIGURE 7: Read Mode Locking Sequence (Soft and Hard Sector)

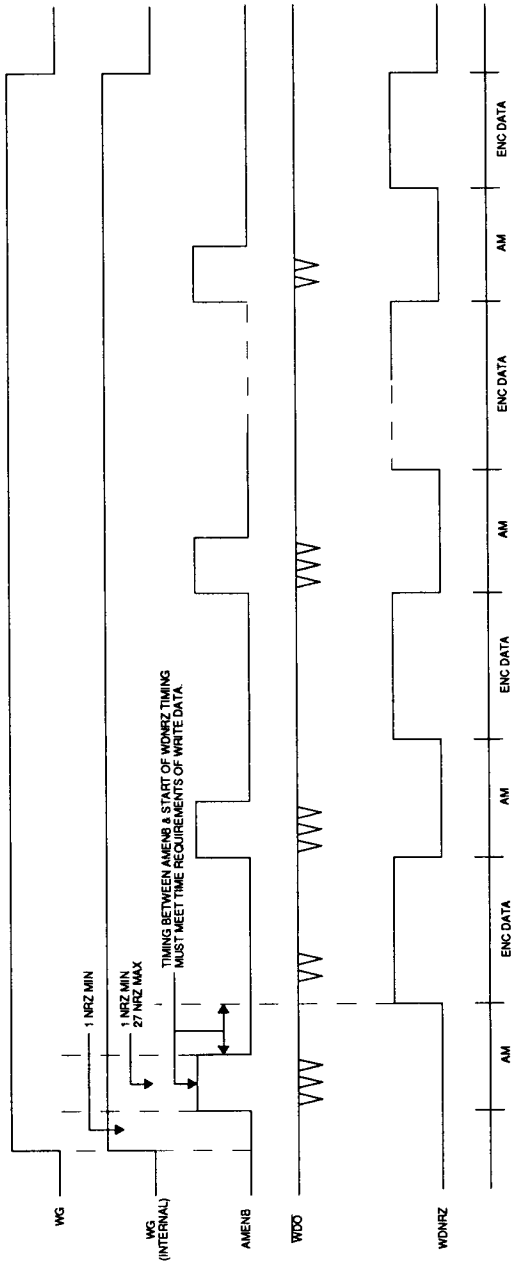


FIGURE 8: Multiple Address Mark Write

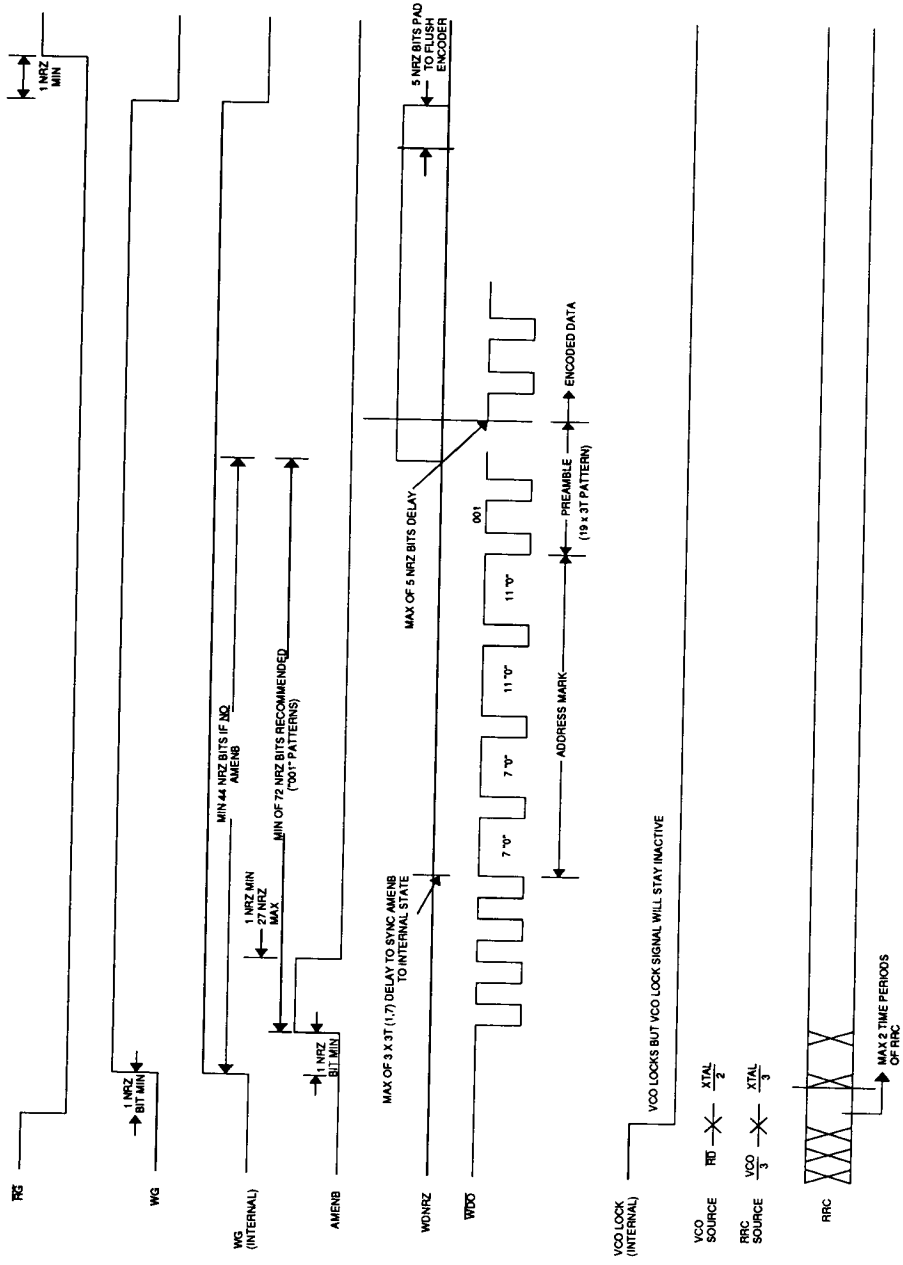
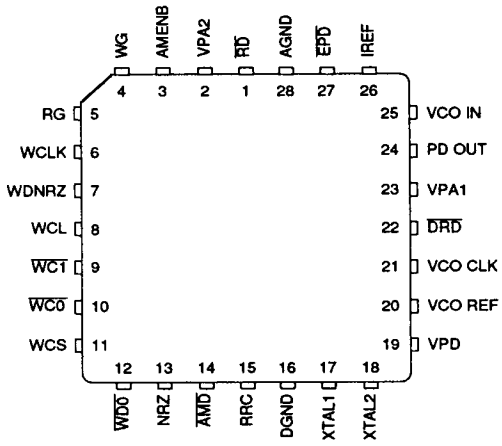


FIGURE 9: Write Data

SSI 32D5362A
Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32D5362A		
28-Pin PLCC	32D5362A-CH	32D5362A-CH

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 731-7110, FAX (714) 573-6914