



MT4C4258

T-46-23-17

DRAM

256K x 4 DRAM

STATIC COLUMN

DRAM

FEATURES

- Industry standard x4 pin-out, timing, functions and packages
- High performance, CMOS silicon gate process
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- All inputs, outputs and clocks are fully TTL and CMOS compatible
- 512 cycle refresh distributed across 8ms
- Refresh modes: $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$, and HIDDEN
- Optional Static Column access cycle

OPTIONS

- Timing
 - 80ns access
 - 100ns access
 - 120ns access
- Packages
 - Plastic DIP
 - Ceramic DIP
 - Plastic ZIP
 - Plastic SOJ

MARKING

- 8
- 10
- 12

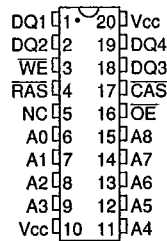
- None
- C
- Z
- DJ

GENERAL DESCRIPTION

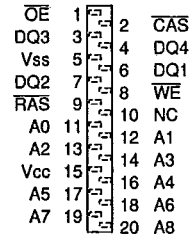
The MT4C4258 is a randomly accessed solid-state memory containing 1,048,576 bits organized in a x4 configuration. During READ or WRITE cycles each bit is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. $\overline{\text{RAS}}$ is used to latch the first 9 bits and $\overline{\text{CAS}}$ the latter 9 bits. A READ or WRITE cycle is selected with the $\overline{\text{WE}}$ input. A logic HIGH on $\overline{\text{WE}}$ dictates READ mode while a logic LOW on $\overline{\text{WE}}$ dictates WRITE mode. During a WRITE cycle data, in (D) is latched by the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. If $\overline{\text{WE}}$ goes LOW prior to $\overline{\text{CAS}}$ going LOW, the output pin(s) remain open (high Z) until the next $\overline{\text{CAS}}$ cycle. If $\overline{\text{WE}}$ goes LOW after data reaches the output pin(s), Q is activated and retains the selected cell data as long as $\overline{\text{CAS}}$ remains LOW (regardless of $\overline{\text{WE}}$ or $\overline{\text{RAS}}$). This late $\overline{\text{WE}}$ pulse results in a READ-WRITE cycle. The 4 data inputs and 4 data outputs are routed through 4 pins using common I/O and pin direction is controlled by $\overline{\text{WE}}$ and OE.

PIN ASSIGNMENT (Top View)

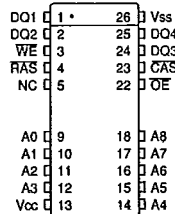
20 Pin DIP (PD, CD)



20 Pin ZIP (ZB)



20 Pin SOJ (DJA)



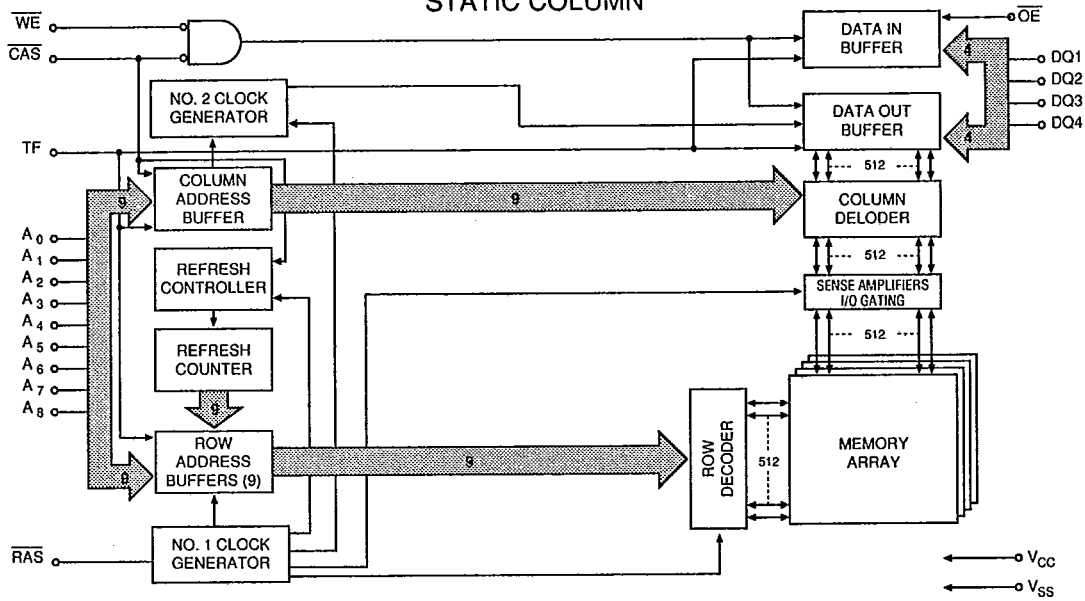
*TF = Test Function, V_{IN} must be disconnected or between Vss and Vcc for normal operation.

Returning $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{\text{RAS}}$ high time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{\text{RAS}}$ cycle (READ, WRITE, $\overline{\text{RAS}}$ ONLY, $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$, or HIDDEN refresh) so that all 512 combinations of $\overline{\text{RAS}}$ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

STATIC COLUMN operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A9) defined page boundary. The STATIC COLUMN cycle is always initiated with a row address strobed in by $\overline{\text{RAS}}$ followed by a column address strobed in by $\overline{\text{CAS}}$. By holding $\overline{\text{RAS}}$ LOW, the column address may be toggled strobing in different column addresses executing faster memory cycles. Returning $\overline{\text{RAS}}$ HIGH terminates the STATIC COLUMN operation.



FUNCTIONAL BLOCK DIAGRAM
STATIC COLUMN



DRAM

TRUTH TABLE

| Function | RAS | CAS | WE | OE | TF | Addresses | | |
|--------------------------|-------|-----|-------|-----|----|-----------|---------|--------------------------------|
| | | | | | | tR | tC | |
| Standby | H | H | H | H | X | X | X | High Impedance |
| READ | L | L | H | L | X | ROW | COL | Data Out |
| WRITE (EARLY-WRITE) | L | L | L | H | X | ROW | COL | Data In |
| READ-WRITE | L | L | H→L→H | L→H | X | ROW | COL | Valid Data Out, Valid Data In |
| STATIC COLUMN READ | L | L | H | L | X | ROW | COL→COL | Valid Data Out, Valid Data Out |
| STATIC COLUMN WRITE | L | L | L | H | X | ROW | COL→COL | Valid Data In, Valid Data In |
| STATIC COLUMN READ-WRITE | L | L | H→L→H | L→H | X | ROW | COL→COL | Valid Data Out, Valid Data In |
| RAS ONLY REFRESH | L | H | H | H | X | ROW | n/a | High Impedance |
| HIDDEN REFRESH | L→H→L | L | H | H | X | ROW | COL | Valid Data Out |
| CAS-BEFORE-RAS REFRESH | H→L | L | H | H | X | X | X | High Impedance |



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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss -1.0V to +7.0V
 Operating Temperature, TA(Ambient) 0°C to +70°C
 Storage Temperature (Ceramic) -65°C to +150°C
 Storage Temperature (Plastic) -55°C to +150°C
 Power Dissipation 1 Watt
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS
 (0°C ≤ TA ≤ 70°C)

| PARAMETER/CONDITION | SYMBOL | MIN | MAX | UNITS | NOTES |
|--|--------|------|-------|-------|-------|
| Supply Voltage | Vcc | 4.5 | 5.5 | V | 1 |
| Input High (Logic 1) Voltage, All Inputs | VIH | 2.4 | Vcc+1 | V | 1 |
| Input Low (Logic 0) Voltage, All Inputs | VIL | -1.0 | 0.8 | V | 1 |
| INPUT LEAKAGE CURRENT any input (0V ≤ VIN ≤ Vcc), all other pins not under test = 0 volts) | Ii | -10 | 10 | µA | |
| OUTPUT LEAKAGE CURRENT (Q is disabled, 0V ≤ Vout ≤ Vcc) | Ioz | -10 | 10 | µA | |
| OUTPUT LEVELS | | | | | |
| Output High voltage (Iout = -5mA) | VOH | 2.4 | | V | |
| Output Low voltage (Iout = 4.2mA) | VOL | | 0.4 | V | |

(Notes : 1, 3, 4, 6, 7) (0°C ≤ TA ≤ 70°C; Vcc = 5.0V ± 10%)

| PARAMETER/CONDITION | SYMBOL | MAX | | | UNITS | NOTES |
|---|--------|-----|-----|-----|-------|-------|
| | | -8 | -10 | -12 | | |
| OPERATING CURRENT (RAS and CAS = Cycling: trc = trc(MIN)) | Icc1 | 70 | 60 | 50 | mA | 3, 4 |
| OPERATING CURRENT: STATIC COLUMN (RAS = VIL, CAS = Cycling: tpc = tpc(MIN)) | Icc2 | 70 | 60 | 50 | mA | 3, 4 |
| STANDBY CURRENT: TTL INPUT LEVELS Power supply standby current (RAS = CAS = VIH after 8 RAS cycles min.) | Icc3 | 3 | 2 | 2 | mA | |
| STANDBY CURRENT: CMOS INPUT LEVELS Power supply standby current (RAS = CAS = Vcc - 0.2V after 8 RAS cycles min. All other inputs at Vcc-0.2V or Vss + 0.2V) | Icc4 | 1 | 1 | 1 | mA | |
| REFRESH CURRENT: RAS ONLY (RAS = Cycling; CAS = VIH) | Icc5 | 70 | 60 | 50 | mA | 3 |
| REFRESH CURRENT: CAS-BEFORE-RAS (RAS and CAS = Cycling) | Icc6 | 70 | 60 | 50 | mA | 3, 5 |

MICRON

MT4C4258

CAPACITANCE

| PARAMETER | SYMBOL | MIN | MAX | UNITS | NOTES |
|--|-----------------|-----|-----|-------|-------|
| Input Capacitance: A ₀ -A ₈ | C _{I1} | | 5 | pF | 2 |
| Input Capacitance: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$ | C _{I2} | | 7 | pF | 2 |
| Input/Output Capacitance: DQ | C _{I0} | | 7 | pF | 2 |

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C; V_{CC} = 5.0V ± 10%)

| A.C. CHARACTERISTICS PARAMETER | SYM | -8 | | -10 | | -12 | | UNITS | NOTES |
|---|------------------|-----|--------|-----|--------|-----|--------|-------|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| Random READ or WRITE cycle time | ^t RC | 150 | | 180 | | 220 | | ns | |
| READ-MODIFY-WRITE cycle time | ^t RWC | 205 | | 245 | | 255 | | ns | |
| Access time from $\overline{\text{RAS}}$ | ^t RAC | | 80 | | 100 | | 120 | ns | 14 |
| Access time from $\overline{\text{CAS}}$ | ^t CAC | | 25 | | 30 | | 30 | ns | 15 |
| Output Enable | ^t OE | | 25 | | 25 | | 25 | ns | |
| Access time from column address | ^t AA | | 40 | | 50 | | 60 | ns | |
| Access time from $\overline{\text{CAS}}$ precharge | ^t CPA | | 45 | | 55 | | 65 | ns | |
| $\overline{\text{RAS}}$ pulse width | ^t RAS | 80 | 10,000 | 100 | 10,000 | 120 | 10,000 | ns | |
| $\overline{\text{RAS}}$ hold time | ^t RSH | 25 | | 25 | | 30 | | ns | |
| $\overline{\text{RAS}}$ precharge time | ^t RP | 60 | | 70 | | 90 | | ns | |
| $\overline{\text{CAS}}$ pulse width | ^t CAS | 25 | 10,000 | 30 | 10,000 | 30 | 10,000 | ns | |
| $\overline{\text{CAS}}$ hold time | ^t CSH | 80 | | 100 | | 120 | | ns | |
| $\overline{\text{CAS}}$ precharge time | ^t CPN | 10 | | 15 | | 20 | | ns | 16 |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time | ^t RCD | 20 | 55 | 25 | 70 | 15 | 90 | ns | 17 |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time | ^t CRP | 10 | | 15 | | 10 | | ns | |
| Row address set-up time | ^t ASR | 0 | | 0 | | ns | | | |
| Row address hold time | ^t RAH | 10 | | 15 | | 15 | | ns | |
| $\overline{\text{RAS}}$ to column address delay time | ^t RAD | 15 | 40 | 20 | 50 | 15 | 60 | ns | 18 |
| Column address set-up time | ^t ASC | 0 | | 0 | | ns | | | |
| Column address hold time | ^t CAH | 15 | | 20 | | 20 | | ns | |
| Column address hold time (referenced to $\overline{\text{RAS}}$) | ^t AR | 95 | | 115 | | 130 | | ns | |
| Column address to $\overline{\text{RAS}}$ lead time | ^t RAL | 40 | | 50 | | 60 | | ns | |
| Read command set-up time | ^t RCS | 0 | | 0 | | 0 | | ns | |
| Read command hold time (referenced to $\overline{\text{CAS}}$) | ^t RCH | 0 | | 0 | | 0 | | ns | 19 |
| Read command hold time (referenced to $\overline{\text{RAS}}$) | ^t RRH | 0 | | 0 | | 0 | | ns | 19 |
| $\overline{\text{CAS}}$ to output in low-Z | ^t CLZ | 0 | | 0 | | 0 | | ns | |
| Output buffer turn-off delay | ^t OFF | 0 | 20 | 0 | 30 | 0 | 25 | ns | 20 |
| Output Disable | ^t OD | | 20 | | 30 | | 25 | ns | |
| $\overline{\text{WE}}$ command set-up time | ^t WCS | 0 | | 0 | | ns | 21 | | |
| Write command hold time | ^t WCH | 15 | | 20 | | 25 | | ns | |



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C, V_{CC} = 5.0V ± 10%)

DRAM

| A.C. CHARACTERISTICS | | -8 | | -10 | | -12 | | | |
|---|-------------------|-----|---------|-----|---------|-----|---------|-------|-------|
| PARAMETER | SYM | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| Write command hold time (referenced to RAS) | t _{WCR} | 60 | | 75 | | 80 | | ns | |
| Write command pulse width | t _{WP} | 15 | | 20 | | 25 | | ns | |
| Write command to RAS lead time | t _{RWL} | 20 | | 25 | | 30 | | ns | |
| Write command to CAS lead time | t _{CWL} | 20 | | 25 | | 30 | | ns | |
| Write inactive time | t _{WI} | 10 | | 10 | | 10 | | ns | |
| Data-in set-up time | t _{DS} | 0 | | 0 | | 0 | | ns | 22 |
| Data-in hold time | t _{DH} | 15 | | 20 | | 20 | | ns | 22 |
| Data-in hold time (referenced to RAS) | t _{DHR} | 70 | | 80 | | 90 | | ns | |
| RAS to WE delay time | t _{RWD} | 110 | | 135 | | 150 | | ns | 21 |
| Column address to WE delay time | t _{AWD} | 70 | | 85 | | 100 | | ns | 21 |
| CAS to WE delay time | t _{CWD} | 55 | | 65 | | 80 | | ns | 21 |
| Transition time (rise or fall) | t _T | 3 | 50 | 3 | 50 | 3 | 50 | ns | 9, 10 |
| Refresh Period (512 cycles) | t _{REF} | | 8 | | 8 | | 8 | ms | |
| RAS to CAS Precharge time | t _{RPC} | 0 | | 0 | | 0 | | ns | |
| CAS set-up time (CAS-BEFORE-RAS refresh) | t _{CSR} | 10 | | 10 | | 10 | | ns | 5 |
| CAS hold time (CAS-BEFORE-RAS refresh) | t _{CHR} | 30 | | 30 | | 30 | | ns | 5 |
| STATIC COLUMN MODE cycle time | t _{SC} | 45 | | 55 | | 65 | | ns | |
| RAS pulse width (STATIC COLUMN) | t _{RASC} | 80 | 100,000 | 100 | 100,000 | 120 | 100,000 | ns | |
| CAS precharge time (STATIC COLUMN) | t _{CP} | 10 | | 10 | | 15 | | ns | |
| STATIC COLUMN READ-MODIFY-WRITE cycle time | t _{SRMW} | 110 | | 135 | | 160 | | ns | |
| Last write to column address delay time | t _{LWAD} | 20 | 40 | 25 | 45 | 30 | 55 | ns | |
| Last write to column address hold time | t _{AHLW} | 75 | | 95 | | 115 | | ns | |
| RAS hold time referenced to OE | t _{ROH} | 10 | | 20 | | 20 | | ns | |
| Output data hold time from column address | t _{AOH} | 5 | — | 5 | — | 5 | — | ns | |
| Output data enable from write | t _{OW} | | 20 | | 30 | | 35 | ns | |
| OE to data delay | t _{OED} | 20 | | 25 | | 30 | | ns | |
| OE command hold time | t _{OEH} | 20 | | 25 | | 25 | | ns | |
| Access time from last write | t _{ALW} | | 75 | | 95 | | 115 | ns | |

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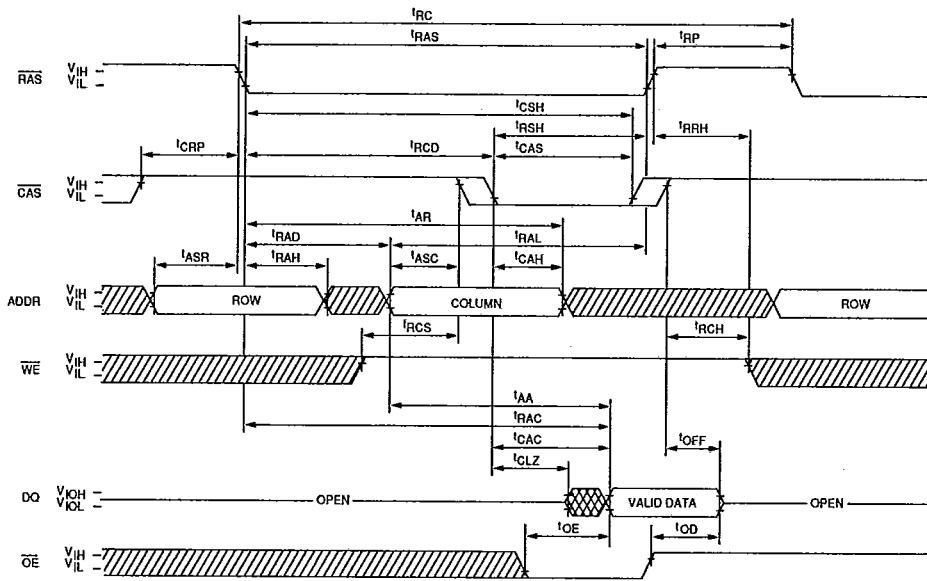
NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. Capacitance is calculated from the equation $C = \frac{I\Delta t}{\Delta V}$ with $\Delta V = 3V$ and $V_{CC} = 5V$.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{\circ}C \leq T_A \leq 70^{\circ}C$) is assured.
7. An initial pause of $100\mu s$ is required after power-up followed by any 8 \overline{RAS} cycles before proper device operation is assured. The 8 \overline{RAS} cycle wake-up should be repeated any time the 8ms refresh requirement is exceeded.
8. AC characteristics assume $t_T = 5ns$.
9. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS} = V_{IH}$, data output is high impedance.
12. If $\overline{CAS} = V_{IL}$, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and $100pF$.
14. Assumes that $t_{RCD} < t_{RCD}(\max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
16. If \overline{CAS} is LOW at the falling edge of \overline{RAS} , Q will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer \overline{CAS} must be pulsed HIGH for t_{CPN} .
17. Operation within the $t_{RCD}(\max)$ limit ensures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
18. Operation within the $t_{RAD}(\max)$ limit ensures that $t_{RCD}(\max)$ can be met. $t_{RAD}(\max)$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled exclusively by t_{AA} .
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. $t_{OFF}(\max)$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
21. t_{WCS} , t_{RWD} , t_{AWD} and t_{CWD} are restrictive operating parameters in late WRITE, READ-WRITE and READ-MODIFY-WRITE cycles only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(\min)$, $t_{AWD} \geq t_{AWD}(\min)$ and $t_{CWD} \geq t_{CWD}(\min)$, the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions are met, the state of data out (at access time and until \overline{CAS} goes back to V_{IH}) is indeterminate.
22. These parameters are referenced to \overline{CAS} leading edge in early WRITE cycles and \overline{WE} leading edge in late WRITE or READ-WRITE cycles.
23. During a READ cycle, if \overline{OE} is LOW then taken HIGH, Q goes open. If \overline{OE} is tied permanently LOW a READ-WRITE or READ-MODIFY-WRITE operation is not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE} = \text{LOW}$ and $\overline{OE} = \text{HIGH}$.

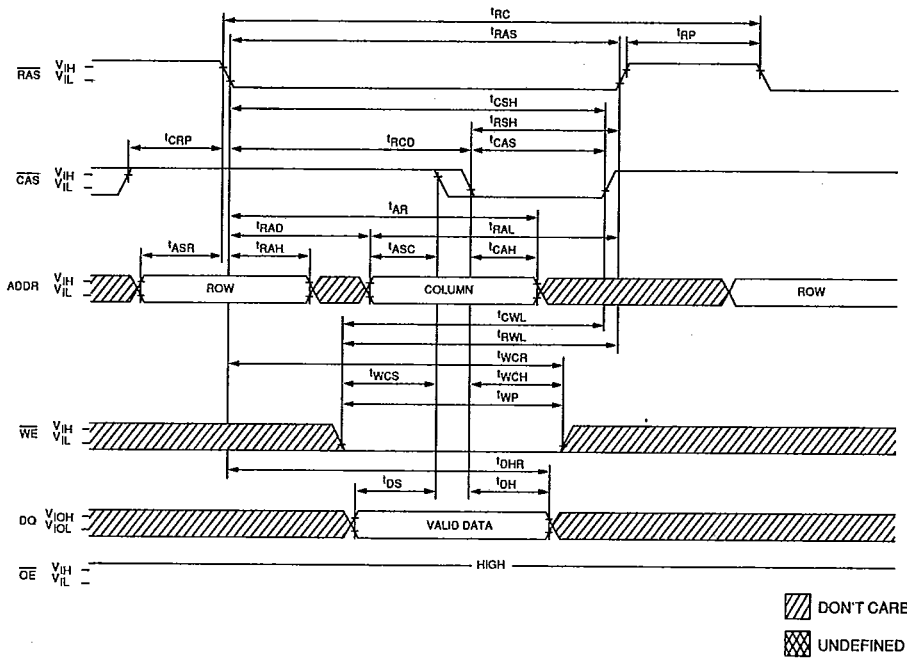


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READ CYCLE



EARLY-WRITE CYCLE



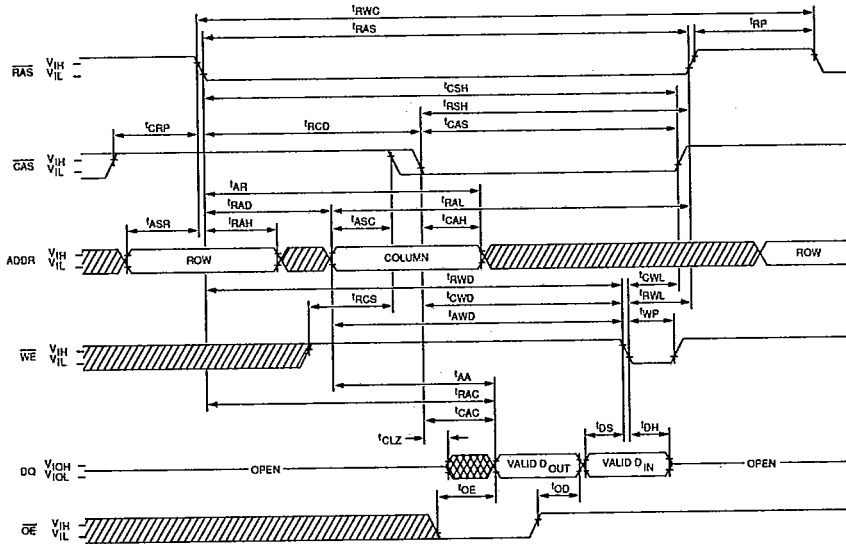
DONT CARE
 UNDEFINED

MICRON

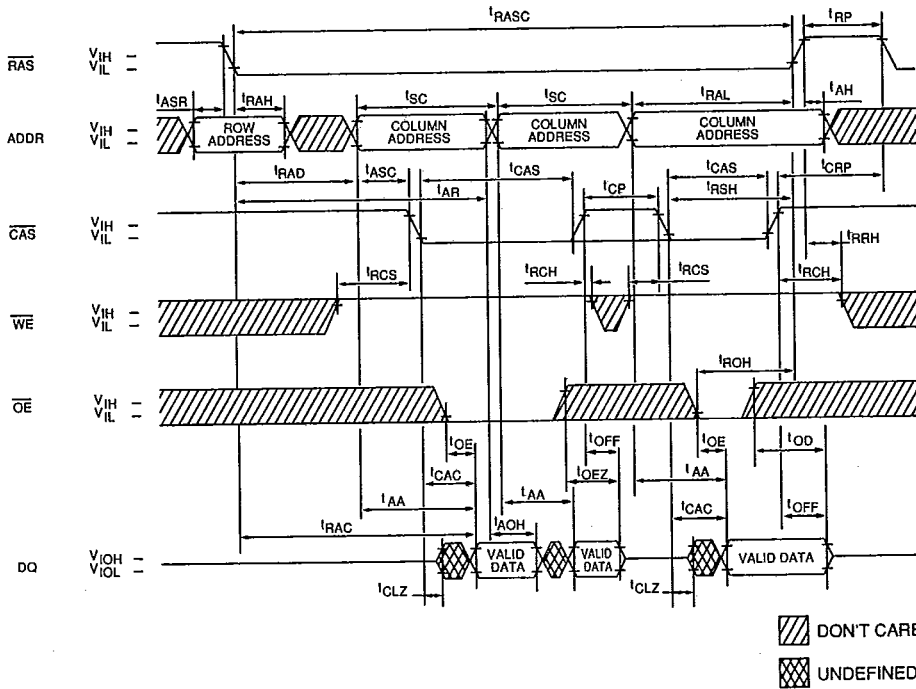
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READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



STATIC COLUMN READ CYCLE

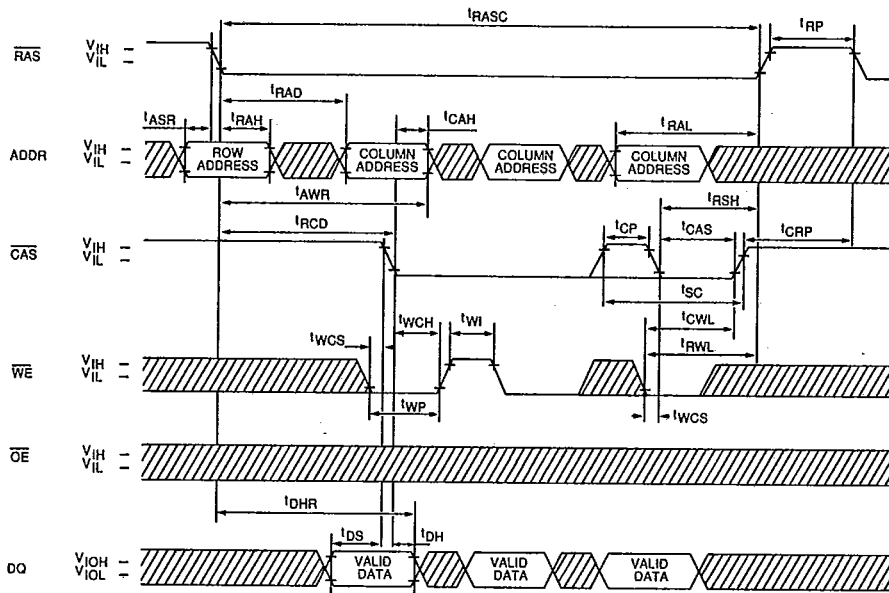


▨ DON'T CARE
▩ UNDEFINED

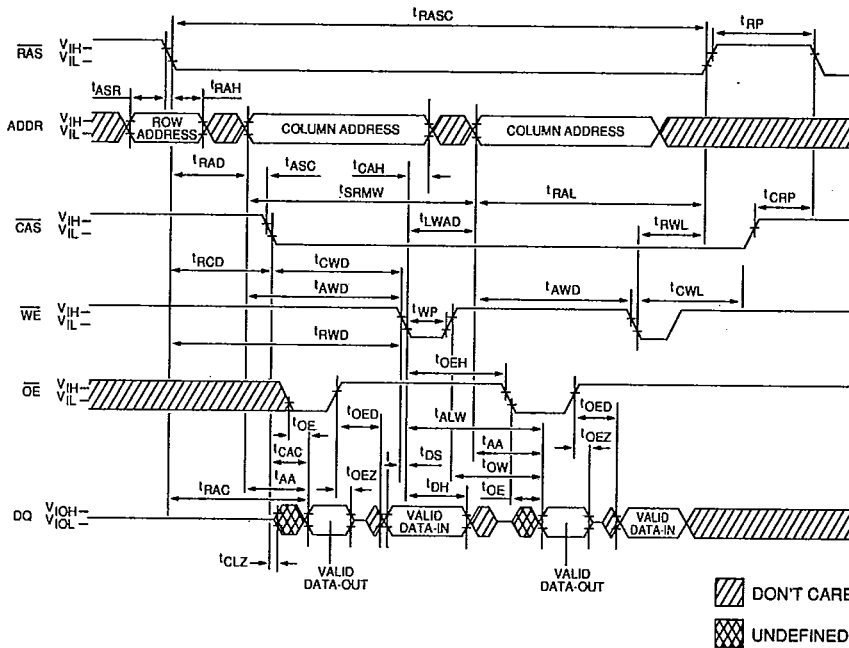
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STATIC COLUMN EARLY-WRITE CYCLE



**STATIC COLUMN READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)**

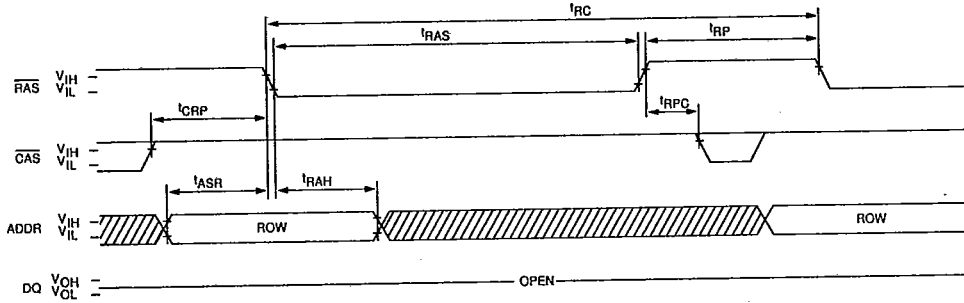




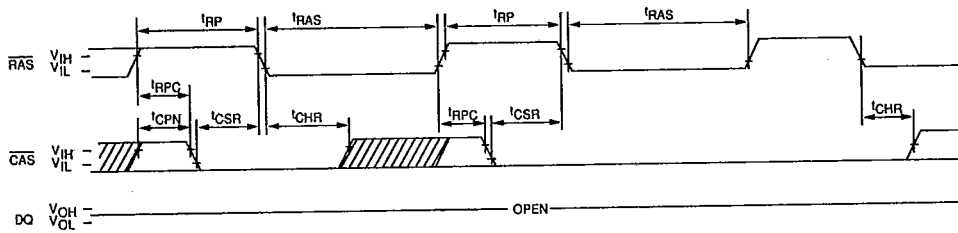
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RAS ONLY REFRESH CYCLE (ADDR = A₀ - A₈; WE = DON'T CARE.)



CAS-BEFORE-RAS REFRESH CYCLE (A₀ - A₈, WE and OE = DON'T CARE)



HIDDEN REFRESH CYCLE (WE = HIGH, OE=LOW)²⁴

