UCN-5800A AND UCN-5801A
BiMOS II LATCHED DRIVERS

FEATURES

- 4.4 MHz Minimum Data Input Rate
- High-Voltage, High-Current Outputs
- Output Transient Protection
- CMOS, PMOS, NMOS, TTL Compatible Inputs
- Internal Pull-Down Resistors
- Low-Power CMOS Latches

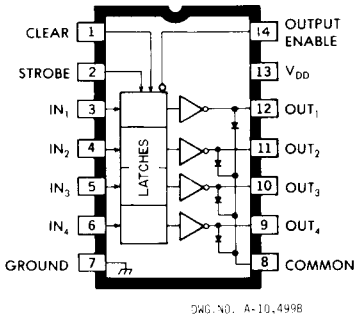
THE UCN-5800A and UCN-5801A latched drivers are high-voltage, high-current integrated circuits comprised of four or eight CMOS data latches, a bipolar Darlington transistor driver for each latch, and CMOS control circuitry for the common CLEAR, STROBE, and OUTPUT ENABLE functions.

The bipolar/MOS combination provides an extremely low-power latch with maximum interface flexibility. Type UCN-5800A contains four latched drivers; Type UCN-5801A contains eight latched drivers.

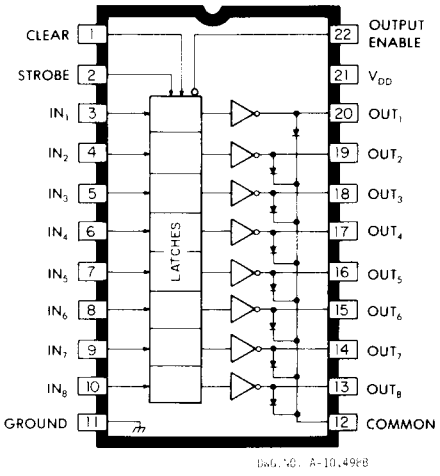
BiMOS II devices have much faster data input rates than the original BiMOS circuits. With a 5 V supply, they will typically operate at better than 5 MHz. With a 12 V supply, significantly higher speeds are obtained.

The CMOS inputs are compatible with standard CMOS, PMOS, and NMOS circuits. TTL or DTL circuits may require the use of appropriate pull-up resistors. The bipolar outputs are suitable for use with relays, solenoids, stepping motors, LED or incandescent displays, and other high-power loads.

Both units have open-collector outputs and integral diodes for inductive load transient suppression. The output transistors are capable of sinking 500 mA and will sustain at least 50 V in the OFF state. Because of limitations on package power dissipation, the simultaneous operation of all drivers at maximum rated current can only be accomplished by a reduction in duty cycle. Outputs may be paralleled for higher load current capability.



UCN-5800A



UCN-5801A

UCN-5800A, the 4-latch device, is furnished in a standard 14-pin dual in-line plastic package. UCN-5801A, the 8-latch device, is supplied in a 22-pin dual in-line plastic package with lead spacing on 0.400" (10.16 mm) centers. To simplify circuit board layout, all outputs are opposite their respective inputs.

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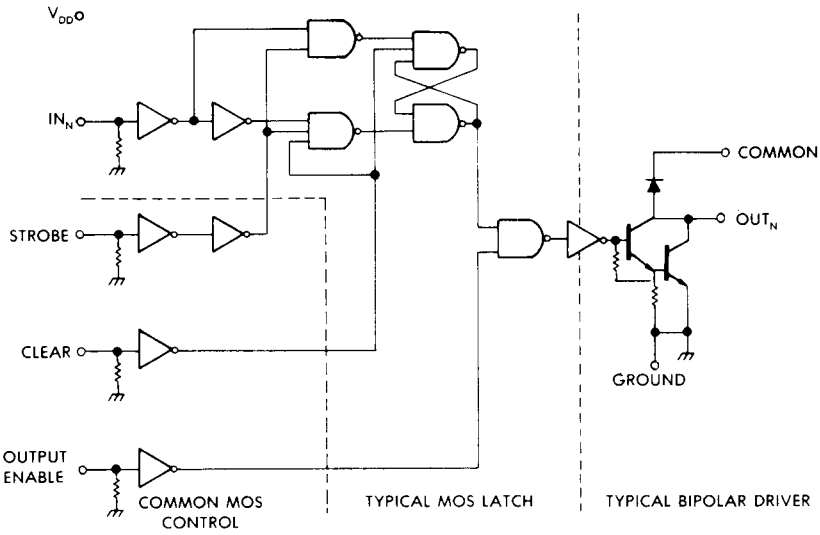
FUNCTIONAL BLOCK DIAGRAM



DWG. NO. A-10,495A

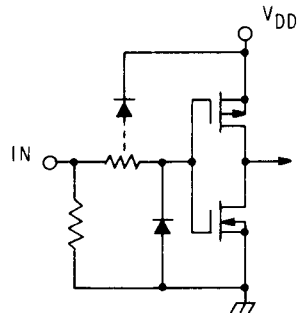
ABSOLUTE MAXIMUM RATINGS
at +25°C Free-Air Temperature

Output Voltage, V_{CE}	50 V
Supply Voltage, V_{DD}	15 V
Input Voltage Range, V_{IN}	−0.3 V to V_{DD} + 0.3 V
Continuous Collector Current, I_C	500 mA
Package Power Dissipation, P_D	
(UCN-5800A)	1.6 W*
(UCN-5801A)	2.0 W**
Operating Temperature Range, T_A	−20°C to +85°C
Storage Temperature Range, T_S	−55°C to +125°C

*Derate at the rate of 16.7 mW/°C above T_A = +25°C.
**Derate at the rate of 20 mW/°C above T_A = +25°C.

Caution: Sprague CMOS devices have input-static protection but are susceptible to damage when exposed to extremely high static electrical charges.

TYPICAL INPUT CIRCUIT



Dwg. No. A-12,520

ELECTRICAL CHARACTERISTICS at $T_A = +25°C$, $V_{DD} = 5\ V$ (unless otherwise noted)

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	$V_{CE} = 50\ V, T_A = +25°C$	—	—	50	µA
		$V_{CE} = 50\ V, T_A = +70°C$	—	—	100	µA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 100\ mA$	—	0.9	1.1	V
		$I_C = 200\ mA$	—	1.1	1.3	V
		$I_C = 350\ mA, V_{DD} = 7.0\ V$	—	1.3	1.6	V
Input Voltage	$V_{IN(0)}$		—	—	1.0	V
	$V_{IN(1)}$	$V_{DD} = 12\ V$	10.5	—	—	V
		$V_{DD} = 10\ V$	8.5	—	—	V
		$V_{DD} = 5.0\ V$ (See Note)	3.5	—	—	V
Input Resistance	R_{IN}	$V_{DD} = 12\ V$	50	200	—	kΩ
		$V_{DD} = 10\ V$	50	300	—	kΩ
		$V_{DD} = 5.0\ V$	50	600	—	kΩ
Supply Current	$I_{DD(ON)}$ (Each Stage)	$V_{DD} = 12\ V$, Outputs Open	—	1.0	2.0	mA
		$V_{DD} = 10\ V$, Outputs Open	—	0.9	1.7	mA
		$V_{DD} = 5.0\ V$, Outputs Open	—	0.7	1.0	mA
	$I_{DD(OFF)}$ (Total)	$V_{DD} = 12\ V$, Outputs Open, Inputs = 0 V	—	—	200	µA
		$V_{DD} = 5.0\ V$, Outputs Open, Inputs = 0 V	—	50	100	µA
Clamp Diode Leakage Current	I_R	$V_R = 50\ V, T_A = +25°C$	—	—	50	µA
		$V_R = 50\ V, T_A = +70°C$	—	—	100	µA
Clamp Diode Forward Voltage	V_F	$I_F = 350\ mA$	—	1.7	2.0	V

NOTE: Operation of these devices with standard TTL or DTL may require the use of appropriate pull-up resistors to insure a minimum logic "1".

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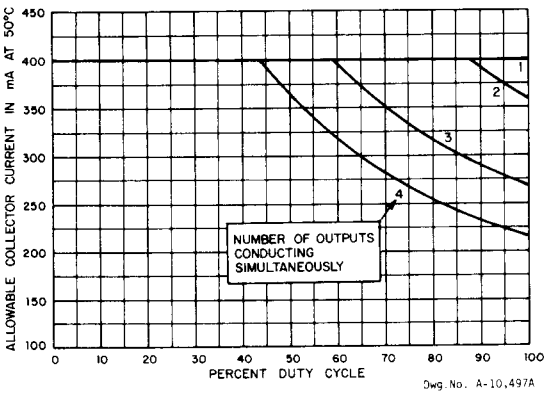
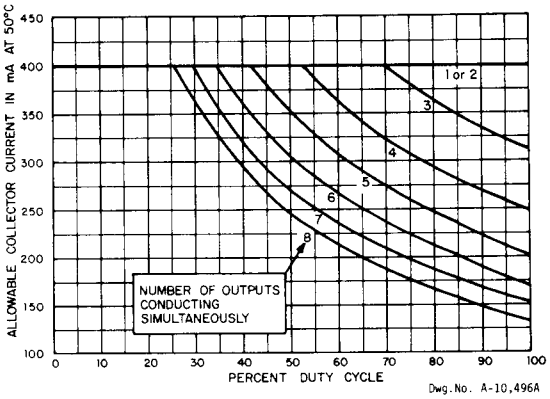
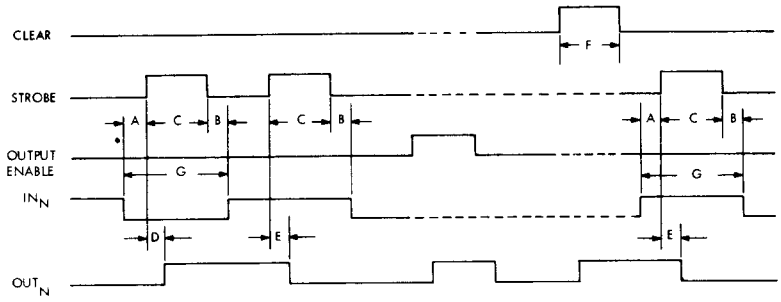
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

UCN-5800A



UCN-5801A





TIMING CONDITIONS

(Logic Levels are V_{DD} and Ground)

A. Minimum data active time before strobe enabled (data set-up time) . . . . . 50 ns
B. Minimum data active time after strobe disabled (data hold time) . . . . . 50 ns
C. Minimum strobe pulse width . . . . . 125 ns
D. Typical time between strobe activation and output on to off transition . . . . . 500 ns
E. Typical time between strobe activation and output off to on transition . . . . . 500 ns
F. Minimum clear pulse width . . . . . 300 ns
G. Minimum data pulse width . . . . . 225 ns

TRUTH TABLE

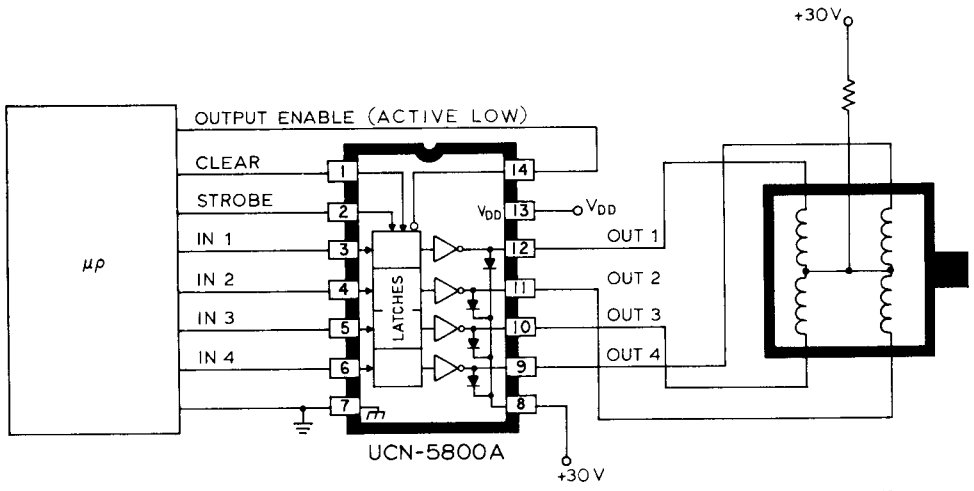
IN_N	STROBE	CLEAR	OUTPUT ENABLE	OUT_N	
				t-1	t
0	1	0	0	X	OFF
1	1	0	0	X	ON
X	X	1	X	X	OFF
X	X	X	1	X	OFF
X	0	0	0	ON	ON
X	0	0	0	OFF	OFF

X = irrelevant.
t-1 = previous output state.
t = present output state.

Information present at an input is transferred to its latch when the STROBE is high. A high CLEAR input will set all latches to the output OFF condition regardless of the data or STROBE input levels. A high OUTPUT ENABLE will set all outputs to the OFF condition, regardless of any other input conditions. When the OUTPUT ENABLE is low, the outputs depend on the state of their respective latches.

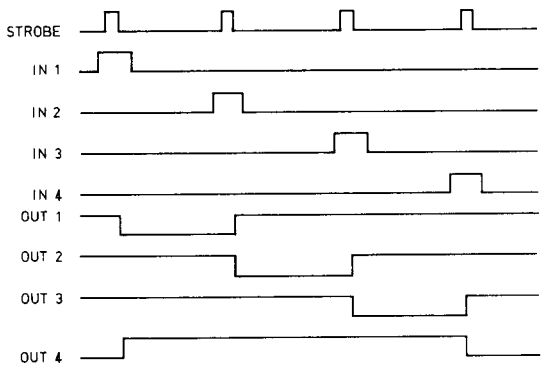
TYPICAL APPLICATION

UNIPOLAR STEPPER-MOTOR DRIVE



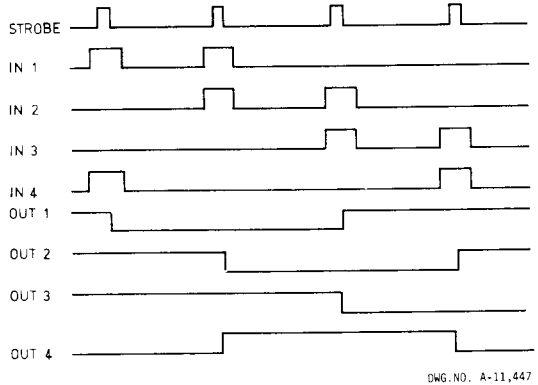
Dwg. No. B-1537

UNIPOLAR WAVE DRIVE



DWG.NO. A-11,446

UNIPOLAR 2-PHASE DRIVE



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