LSI LOGIC

CW900006 Triple 10-bit Video Cell LCB/LEA500K

Advance Datasheet

Introduction

The CW900006 is a complete triple 10-bit video digital-to-analog converter (VDAC) that is implemented as a standard cell in LSI Logic's 0.5 µm 500K process technology. It is designed for use in video systems such as computer video monitors that use the RGB video input standard. The CW900006 VDAC is suitable for integration into any cell-based or embedded-array design that uses LSI Logic's LCB500K or LEA500K process technology.

The CW900006 VDAC's current-output, triple DAC cell provides sufficient output to drive the double-terminated 75-ohm transmission lines found in most RGB video systems. Maximum current drive for each output is 17.6 mA. This is divided into 1,023 levels in a 10-bit system, so that the least-significant bit (LSB) of current is (17.6/1023) mA.

An individual blanking input (BLANKN) for each of the three colors controls the superposition of an additional 83.5 LSBs of current onto each output. A SYNCN input controls the superposition of an additional 442.5 LSBs of current onto the GREEN output. Excellent transient performance is facilitated with a segmented architecture, as well as the capability to both connect each video transmission line's ground to each DAC's complementary output, while keeping these signal return paths isolated from each other. Built-in multiplexers control the connection of the DAC to either the color input buses or the test input bus.

Features

- Triple 10-bit VDAC with Red, Green, and Blue (RGB) outputs
- 220 MHz operation
- Segmented architecture
- Pin-configurable to use either an on-chip voltage reference, an off-chip voltage reference, or an off-chip current reference
- Test mode simplifies test vector generation and production testing
- Blank on Red, Green, and Blue
- Sync on Green
- Wide V_{DD} operating range of 2.7 V to 3.6 V
- Power-down function
- Integrated analog output comparators
- Compatible with LSI Logic's 0.5 µm 500K process
- Cell size is 1291 µm x 2485 µm (0.051" x 0.098")

Order Number B15037
March 1996

Block Diagram The block diagram for the CW900006 triple 10-bit video DAC cell is provided in Figure 1.

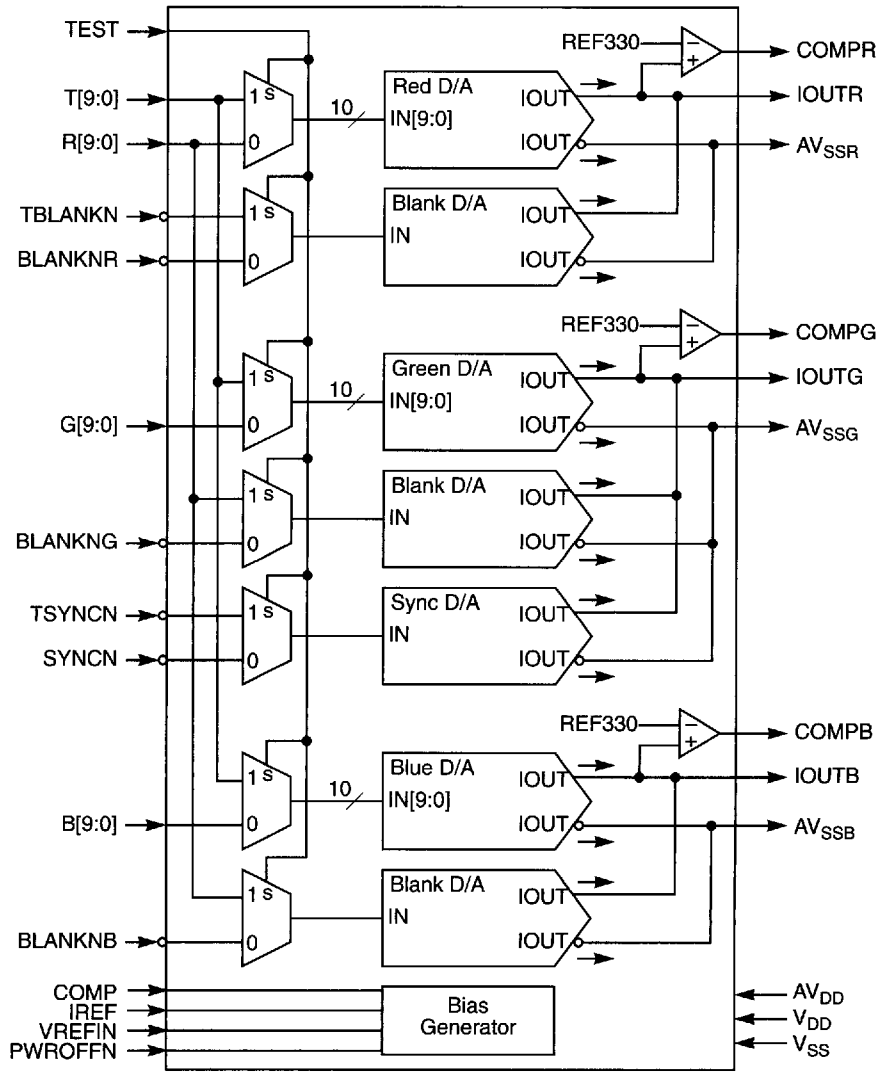


Figure 1. CW900006 VDAC Block Diagram

Signal Descriptions

This section describes the CW900006 triple 10-bit video DAC cell signals and contains the following subsections:

- Analog Signals
- Digital Signals
- Digital Buses

Analog Signals

ASUB — **Analog Substrate Connection**
Connects to the analog substrate of the CW900006 VDAC.

AV_{DD} — **Analog Power**
Provides power to the analog portions of the CW900006 VDAC.

$AV_{SS}R$ — **Red DAC Complementary Output**
This output is typically connected to the grounded shield of the Red video transmission line.

$AV_{SS}G$ — **Green DAC Complementary Output**
This output is typically connected to the grounded shield of the Green video transmission line.

$AV_{SS}B$ — **Blue DAC Complementary Output**
This output is typically connected to the grounded shield of the Blue video transmission line.

COMP — **Reference Loop Compensation Pin**
When using an external current reference, connect this pin to the IREF pin. When using a 1.235 volt reference, this pin may be left open or capacitively coupled to AV_{DD}.

IOUTR — **Red DAC Output**
Red analog output.

IOUTG — **Green DAC Output**
Green analog output.

IOUTB — **Blue DAC Output**
Blue analog output.

IREF — **VDAC Current Reference Input**
When using an external current reference, connect the current reference between this pin and V_{SS}. When using a voltage reference, connect RSET = 374 ohm between this pin and V_{SS}.

PWROFFN — **VDAC Power Off**
The CW900006 VDAC is powered off when this pin is low. All output currents will be zero.

VREFIN — **VDAC Voltage Reference Input**
When using an external voltage reference, connect this pin to the reference voltage. When using an external current reference, connect this pin to V_{SS}.

Digital Signals

BLANKNR — **Blank Red**
When this input is high, 83.5 LSBs of current are added to the Red output. When it is low, the Red output reflects the data on R[9:0]. See Video Output Truth Tables on page 5 and discussion in Chip Design and Layout on page 8 for a detailed description. RED inputs must be masked to zeros to give zero output.

BLANKNG — **Blank Green**
When this input is high, 83.5 LSBs of current are added to the Green output. Note that when it is low, the Red output continues to reflect the data on G[9:0] rather than going to 0. See Video Output Truth Tables on page 5 and discussion in Chip Design and Layout on page 8 for a detailed description. GREEN inputs must be masked to zeros to give zero output.

BLANKNB — **Blank Blue**
When this input is high, 83.5 LSBs of current are added to the Blue output. When it is low, the Red output reflects the data on B[9:0]. See Video Output Truth Tables on page 5 and discussion in Chip Design and Layout on page 8 for a detailed description. BLUE inputs must be masked to zeros to give zero output.

COMPR — **Compare Red**
This output is high when the voltage at IOUTR is 330 mV or higher. Is is low when the voltage is below 330 mV.

COMPG — **Compare Green**
This output is high when the voltage at IOUTG is 330 mV or higher. It is low when the voltage is below 330 mV.

COMPB — **Compare Blue**
This output is high when the voltage at IOUTB is 330 mV or higher. It is low when the voltage is below 330 mV.

SYNCN — **Synch**
When this input is high, 442.5 LSBs of current are added to the Green output.

TEST — **Test Mode**
Puts the CW900006 VDAC into test mode so that it is controlled by the T[9:0], TBLANKN, and TSYNCN signals. This signal is active high.

TBLANKN — **Test Blank**
When this input and TEST are high, 83.5 LSBs of current are added to each color output.

TSYNCN — **Test Synch**
When this input and TEST are high, 442.5 LSBs of current are added to the Green output.

V_{DD} — **Digital Power**
Digital operating power input.

V_{SS} — **Digital Ground**
Digital ground connection.

Digital Buses

R[9:0] — **Red Digital Input Bus**
This bus carries the digital value for the Red input to the CW900006 VDAC.

G[9:0] — **Green Digital Input Bus**
This bus carries the digital value for the Green input to the CW900006 VDAC.

B[9:0] — **Blue Digital Input Bus**
This bus carries the digital value for the Blue input to the CW900006 VDAC.

T[9:0] — **Test Data Bus**
This input bus controls all three color DACs when the TEST input is high.

Video Output Truth Tables

Table 1 - Table 4 define the output currents for the three DACs under normal operation and test conditions.

Table 1. Red Output (IOUTR)

R[9:0]	TEST	BLANKNR	SYNCN	IOUTR (mA)
$3FF	0	0	x	17.62
data	0	1	x	(data/1023) · 17.62 + 1.44
data	0	0	x	(data/1023) · 17.62
$000	0	0	x	0.00

Table 2. Green Output (IOUTG)

G[9:0]	TEST	BLANKNG	SYNCN	IOUTG (mA)
$3FF	0	0	0	17.62
data	0	1	1	(data/1023) · 17.62 + 9.06
data	0	0	1	(data/1023) · 17.62 + 7.62
data	0	1	0	(data/1023) · 17.62 + 1.44
data	0	0	0	(data/1023) · 17.62
$000	0	0	0	0.00

Table 3. Blue Output (IOUTB)

B[9:0]	TEST	BLANKNB	SYNCN	IOUTB (mA)
$3FF	0	0	x	17.62
data	0	1	x	(data/1023) · 17.62 + 1.44
data	0	0	x	(data/1023) · 17.62
$000	0	0	x	0.00

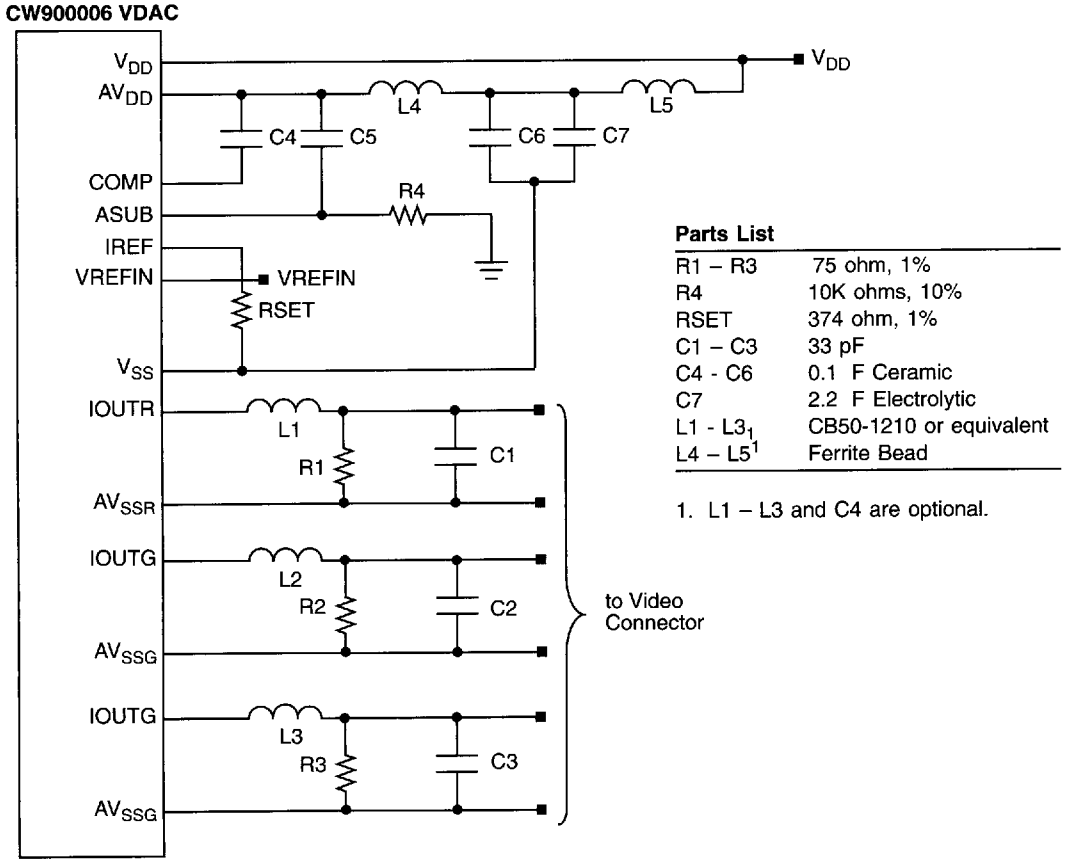
Table 4. Test Mode Outputs for All Three Colors

Test Conditions: 75 ohm doubly-terminated load, VREFIN = 1.235V, RSET = 374 ohm

T[9:0]	TEST[1]	TBLANKN	TSYNCN	IOUTR (mA)	IOUTG (mA)	IOUTB (mA)
$3FF	1	0	0	17.62	17.62	17.62
data	1	1	1	(data/1023) · 17.62 + 1.44	(data/1023) · 17.62 + 9.06	(data/1023) · 17.62 + 1.44
data	1	0	1	(data/1023) · 17.62	(data/1023) · 17.62 + 7.62	(data/1023) · 17.62
data	1	1	0	(data/1023) · 17.62 + 1.44	(data/1023) · 17.62 + 1.44	(data/1023) · 17.62 + 1.44
data	1	0	0	(data/1023) · 17.62	(data/1023) · 17.62	(data/1023) · 17.62
$000	1	0	0	0.00	0.00	0.00

1. When TEST = 0, the test control signals T[9:0], TBLANKN, and TSYNCN have no effect on the VDAC's output currents. When TEST = 1, the normal control signals R[9:0], G[9:0], B[9:0], BLANKNR, BLANKNG, BLANKNB, and SYNC have no effect on the VDAC's output currents.

A typical connection diagram and components for internal and external voltage reference are shown in Figure 2 and Figure 3.

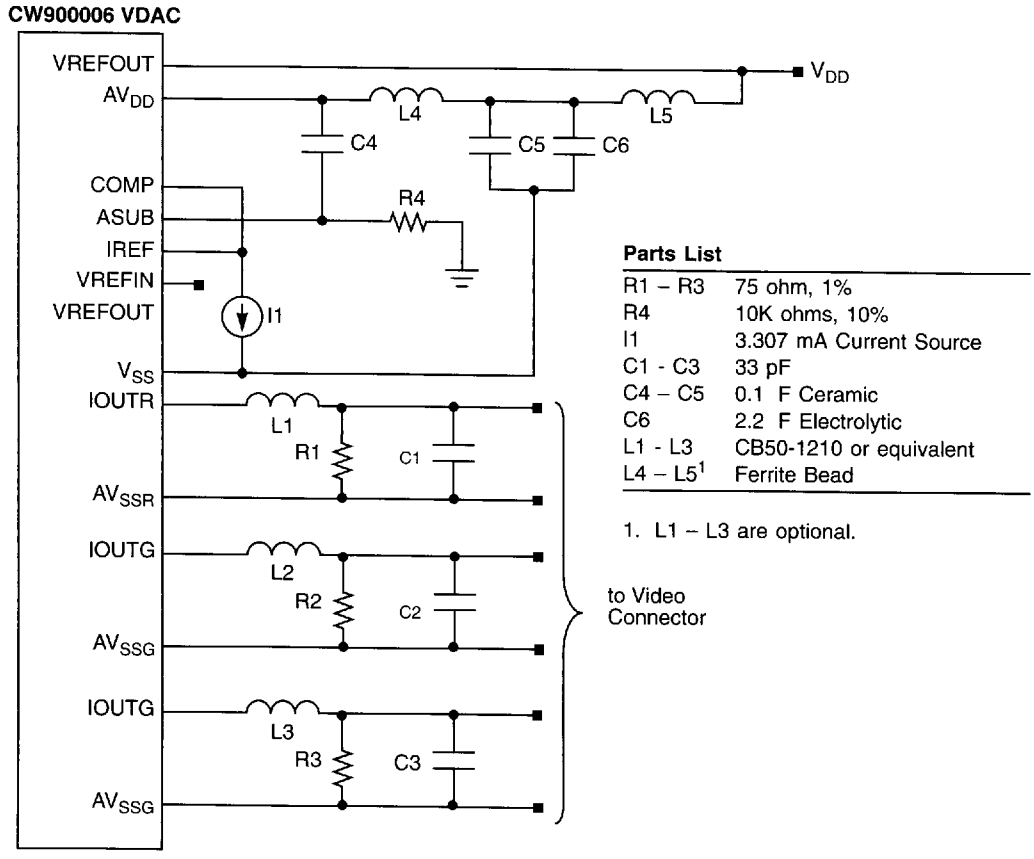


Parts List

R1 – R3	75 ohm, 1%
R4	10K ohms, 10%
RSET	374 ohm, 1%
C1 – C3	33 pF
C4 - C6	0.1 F Ceramic
C7	2.2 F Electrolytic
L1 - L3[1]	CB50-1210 or equivalent
L4 – L5[1]	Ferrite Bead

1. L1 – L3 and C4 are optional.

Figure 2. Typical Connection Diagram and Components, Internal Voltage Reference



Parts List

R1 – R3	75 ohm, 1%
R4	10K ohms, 10%
I1	3.307 mA Current Source
C1 - C3	33 pF
C4 – C5	0.1 F Ceramic
C6	2.2 F Electrolytic
L1 - L3	CB50-1210 or equivalent
L4 – L5[1]	Ferrite Bead

1. L1 – L3 are optional.

Figure 3. Typical Connection Diagram and Components, External Current Reference

Chip Design and Layout

The integration of the CW900006 VDAC into a larger ASIC requires that a few precautions and design requirements be followed.

Input Register Configuration

Color buses and VDAC control signals must be latched in registers outside of the CW900006 VDAC itself. To minimize input data skew, color input buses (R[9:0], G[9:0], and B[9:0]) should be driven by registers placed, as close as possible, to the CW900006 VDAC. D flip-flops that include a clear function, such as the FD2QP, should be used to construct the registers. The appropriate BLANKN signal can then be connected to the flip-flop's CLEAR input. Figure 4 shows the recommended CW900006 VDAC input register configuration.

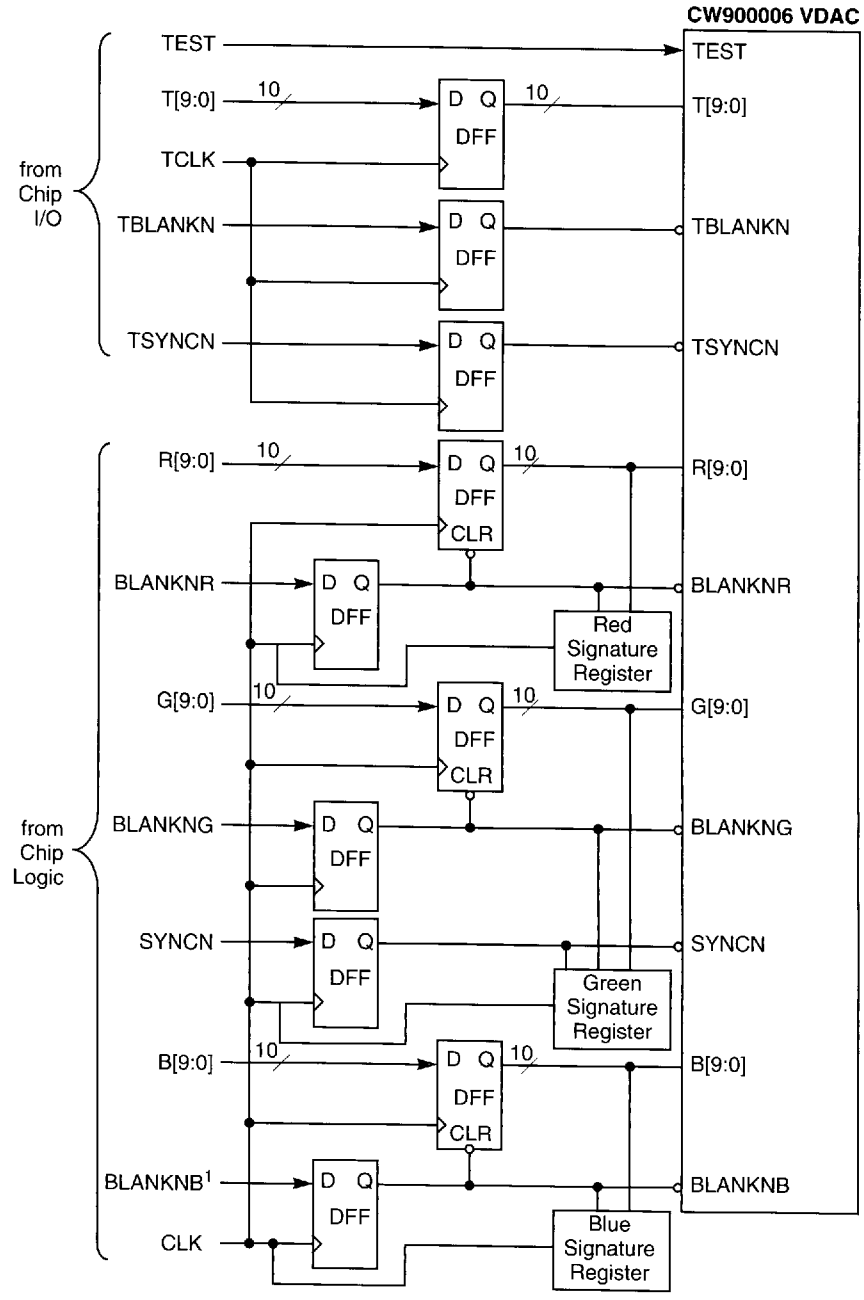
Test Configuration

Production test equipment must be able to access the CW900006 VDAC inputs, therefore, the test bus T[9:0] and test signals TBLANKN and TSYNCN must connect to device pins. These pins may be dual-use pins that have other functions during normal operation (TEST = 0). If possible, the TEST pin itself should connect to a dedicated device pin. If that is not possible, the TEST signal can be asserted through an otherwise unused combination of existing device pins.

The use of scannable registers, or otherwise readable registers, to improve test coverage is recommended. The configuration shown in Figure 4, where a signature register is connected to each color bus, is one possible test mode.

Minimize Noise

To minimize noise pickup on-chip, the CW900006 VDAC cell should be placed next to the pad ring. No digital signals should cross any analog connections made between the CW900006 VDAC and the pad ring. The AV_{DD}, AV_{SSR}, AV_{SSG}, and AV_{SSB} signals should be brought out to separate pads. COMP and IREF may be connected on chip if an external current reference is to be used; otherwise, they should be brought out to a pad.



1. Red and green blank like blue blanks.

Figure 4. Recommended CW900006 VDAC Input Register Configuration

PC Board Design and Layout

For proper operation of the CW900006 VDAC, careful PC board layout is necessary.

Analog Power

A small local analog power plane is necessary to minimize noise induced by the power supply on the VDAC outputs.

Connectors

Proper termination of the 75-ohm transmission lines will keep reflections and crosstalk to a minimum. In addition, the CW900006 VDAC should be located as close to the video connector on the board as possible to minimize noise pickup. A small ferrite bead in series with each VDAC output may be needed to reduce radiated electromagnetic energy.

Shield Connections

The shields for the on-board 75-ohm video transmission lines (typically microstrip or stripline) should be generally isolated from each other and from digital ground. If shields are connected to digital ground on the PC board, the connection should be made at a single point close to the device pins AV_{SSR}, AV_{SSG}, and AV_{SSB}.

Better performance may be possible with no connection of the shields to ground on the PC board at all, relying only on the shield connection to ground at the monitor. In this case, the shield of each color's transmission line should connect to its corresponding AV_{SS} pin. For ESD protection, a resistor from each of these connections to ground is recommended.

Test Vectors

Production test vectors delivered to LSI Logic must include the sequence of vectors as shown in Table 5. The chip-level pin names which correspond to the CW900006 VDAC test inputs must be identified, as well as the location of the vectors within the overall vector set.

Table 5. Sequence of Vectors

TEST	TBLANKN	TSYNCN	T[9:0]
1	0	0	$000
1	0	1	$000
1	1	0	$000
1	1	1	$001
1	1	1	$002
.	.	.	.
.	.	.	.
.	.	.	.
1	1	1	$3FF

Specifications

This section specifies the CW900006 VDAC's electrical characteristics and has two sections.

- AC Electrical Specifications
- Electrical Requirements

AC Electrical Specifications

Table 6. AC Timing

Test Conditions: 50 ohm doubly-terminated load, VREFIN = 1.235 V, RSET = 374 ohms

Parameter	Symbol	Min	Typ	Max	Units
Analog Output Rise Time[1, 2]	tr		2		ns
Analog Output Settling Time[1, 3]	ts		5		ns
Analog Output Settling Time[3, 1]	ts		7		ns
Glitch Impulse Area[1, 4]			40		pV-s

1. $AV_{DD} \geq 3.1$ V.
2. 10% to 90% of full-scale transition.
3. Full-scale transition; time from output at 50% to ± 2 LSB of final value, not including clock and data feedthrough.
4. At major-carry transition, not including clock and data feedthrough.

Electrical Requirements

This section specifies the electrical requirements for the CW900006 VDAC. Two tables list the electrical data in the following categories:

- Recommended Operating Conditions (Table 7)
- DC Characteristics (Table 8)

Table 7. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Power Supply (AV_{DD}, V_{DD})	2.7	3.3	3.6	V
Ambient Operating Temperature (TA)	0	25	70	C
Output Load (RL)		37.5		ohms
Full-Scale Adjust Resistor (RSET)[1]		374		ohms
Voltage Reference (VREF)[1]	1.1	1.235	1.4	V
Current Reference (IREF)[2]	-2	-3.307	-4	mA

1. Configured with a voltage reference connected to VREFIN and RSET connected to the IREF pin.
2. Configured with a current reference connected to IREF and COMP (shorted together) and VREFIN = V_{SS}.

Table 8. DC Characteristics

Test Conditions: 75 ohm doubly-terminated load, VREFIN = 1.235 V, RSET = 374 ohm

Parameter	Condition	Min	Typ	Max	Units
Resolution			10		Bits
Integral Linearity Error	INL		± 1		LSB
Differential Linearity Error	DNL		± 1		LSB
Coding					Binary
White Level Relative to Black		16.74	17.62	18.50	mA
Black Level Relative to Black		1.37	1.44	1.52	mA
Sync Level (Green Output Only)		7.24	7.62	8.00	mA
Sync Level (Red and Blue Outputs)		0	5	50	µA
LSB Size			17.2		µA
DAC to DAC Matching			2	5	%
Output Compliance[1]	VOC	-1		1.05	V
VREF Input Current			2		µA
Voltage Reference Output Voltage	VREFOUT	1.24	1.32	1.40	V
Analog Comparator Compare Voltage		0.27	0.33	0.39	V
AV_{DD} Supply Current	IAV_{DD}		68		mA
V_{DD} Supply Current[2]	IV_{DD}		10		mA

1. $AV_{DD} \geq 3.1$ V.
2. 220 MB/S input data rate.