MA525

MICROPROCESSOR CONTROLLED LD/DTMF DIALLER

The MA525 is a microprocessor controlled Loop Disconnect (LD) and Dual Tone Multi-Frequency (DTMF) dialler device with a last number redial facility.

The MA525 is directly controlled via a MOTEL™ interface which automatically adapts to either Motorola or Intel format, thereby allowing interfacing to most common microprocessors and microcontrollers. The bus design allows both 4 and 8-bit bus systems to be used and the device is designed to allow the bus to be shared with other peripheral devices.

All dialling conditions and timings are programmable via on-chip registers in order to allow the device to meet the specifications of virtually any telephone network with one standard product. Blocks of up to 21 digits at a time (including TBR and Pause) can be loaded for dialling. The device will retain the last number dialled for redialling if required.

Dialling and associated control signals are generated by the device in both LD and DTMF modes using a low-cost 560kHz ceramic resonator as an accurate timing reference.The A,B,C,D tone pairs are available in DTMF mode. In addition, a 'single tone' output is provided.

The MA525 can be operated in either 'Phone' or 'Modem' mode, generating appropriate control signals for the application.

The polarity of all output signals may be inverted, making the MA525 suitable for use with virtually any line interfacing technique.

A chip select (CS) input is also provided, allowing the MA525 to share a common microprocessor bus with other microprocessor peripherals.

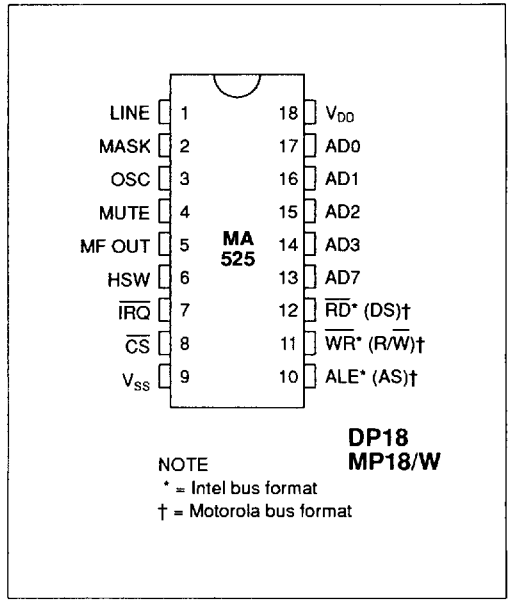


Figure 1 Pin connections - top view

APPLICATIONS

- Feature Telephones
- Auto-Dialling Modems
- Auto-Dialling Telephones
- Pay Phones
- Security Products
- Cordless Telephone Base Stations
- Banking Facilities

FEATURES

- MOTEL™ Microprocessor Interface for Direct Connection to Motorola or Intel Derived Buses
- Loop-Disconnect and DTMF dialling
- Modem and Phone Modes.
- Last Number Redial Facility.
- All Timing Parameters Programmable to meet International Signalling Requirements
- Reloadable 21-digit Store Including Access Pause and Timed Break Recall (Flash).
- Reliable Power-on Reset.
- Uses a Low-cost 560kHz Ceramic Resonator

PIN FUNCTIONS

Pin no.	Name	Type	Function
1	LINE	O	Dialling pulse output and modem line control.
2	MASK	O	Output to disable speech circuit during LD dialling and TBR.
3	OSC	I/O	Connection for 560kHz ceramic resonator
4	MUTE	O	Output to inhibit microphone during DTMF dialling. In Modem mode it can be used to switch DTMF tones or the modem to the line
5	MF OUT	O	DTMF tone output.
6	HSW	I	Hookswitch sense input. '1' = Off-hook. No direct control for modem use but status still available.
7	$\overline{IRQ}$	O	Interrupt request N-channel open-drain output.
8	$\overline{CS}$	I	Chip select input. Used to activate MOTEL interface.
9	V_{SS}	SUPPLY	Negative supply
10	AS ALE	I	Motorola Mode Address Strobe Intel Mode: Address Latch Enable
11	R/$\overline{W}$ $\overline{WR}$	I	Motorola Mode: Read/Write Intel Mode: Write Strobe
12	DS RD	I	Motorola Mode: Data Strobe Intel Mode. Read Strobe
13	AD7	I/O	Available for servicing interrupt request
14	AD3	I/O	Multiplexed address/data bi-directional bus. MSB
15	AD2	I/O	Multiplexed address/data bi-directional bus.
16	AD1	I/O	Multiplexed address/data bi-directional bus.
17	AD0	I/O	Multiplexed address/data bi-directional bus LSB.
18	V_{DD}	SUPPLY	Positive supply.

Table 1: Pin functions

MICROPROCESSOR INTERFACE

The MA525 interfaces to the controlling microprocessor by means of a multiplexed bus of the MOTEL format. This interface bus has the ability to adapt itself automatically to the format and timing of both MOTorola and IntEL interface busses (hence MOTEL). Internally, the detection circuitry latches the status of the DS/$\overline{RD}$ line when AS/ALE goes high. If the result is high, then the Intel mode is used; if the result is low then the Motorola mode is used. This procedure is carried out each time that AS/ALE goes high. Note that the MA525 defaults to Intel mode on power up and is reconfigured to the relevant mode after the first DS/ALE positive going edge.

In practice the MOTEL interface is transparent to the user. For bus connection and timing information simply refer to the description relevant to the particular microprocessor/ microcontroller used.

Industry standard microprocessors such as the 8085,8088 etc and microcontrollers such as the 8051 or 6805 are all compatible with the interface on the MA525 It is also possible to drive the microprocessor interface pins on the MA525 directly using port pins .

It should be noted that all bus timings are derived from the microprocessor and are independent of the MA525 clock input.

Registers 0 to 9 are write only whereas Register 10 is a read-only Status Register. An interrupt pin is provided ($\overline{IRQ}$) to speed microprocessor interfacing. This may be disabled at any point if necessary In addition, an Interrupt Request Flag Register 10 operates in exactly the same way as the $\overline{IRQ}$ pin (but is active high).

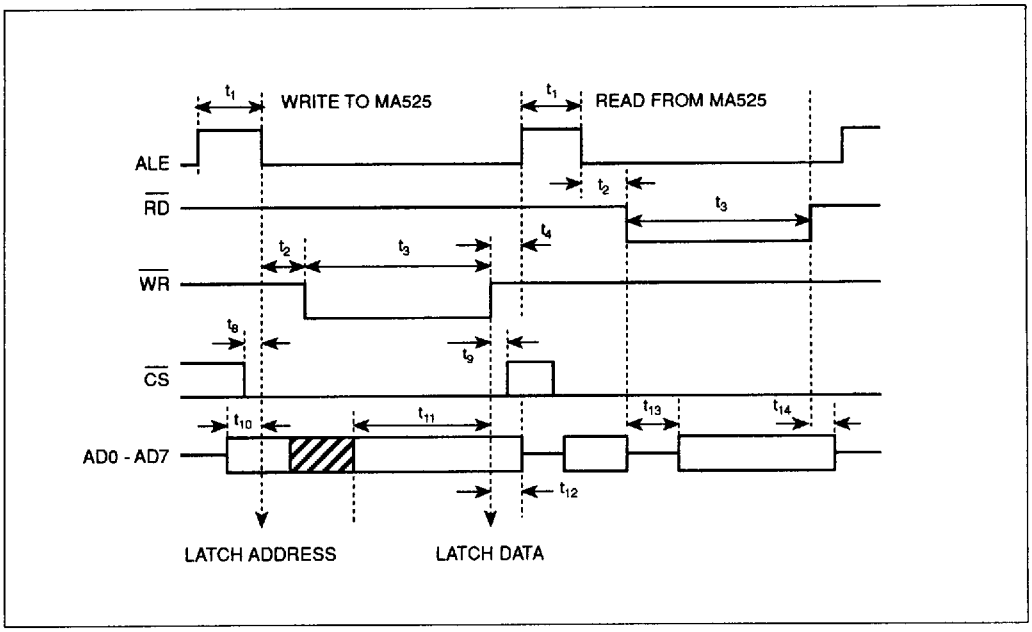


Figure 2: Intel bus timing diagram

Parameter	Symbol	Min.	Typ.	Max.	Units
ALE high period	t_1	70			ns
Delay time, ALE to $\overline{WR}$	t_2	40			ns
$\overline{WR}$ low period	t_3	50			ns
Delay time, WR high to ALE high	t_4	10		50µs	ns
$\overline{CS}$ setup time	t_8	40			ns
$\overline{CS}$ hold time	t_9	0			ns
Address setup time	t_{10}	30			ns
Address hold time	t_{15}	10			ns
Data setup time	t_{11}	50			ns
Data hold time	t_{12}	0			ns
Output data response time	t_{13}		60	85	ns
Output data removal time	t_{14}		30	50	ns

The address is latched by the falling edge of ALE. Data is written from the bus into the MA525 on the rising edge of $\overline{WR}$. Data can be read from the MA525 on the rising edge of $\overline{RD}$ providing that this follows the falling edge of $\overline{RD}$ by the minimum period, t_3. All bus timings are quoted with 30pF capacitance to V_{SS}.

Table 2: Intel bus timings at V_{DD} = 5V, T_{amb} = +25°C

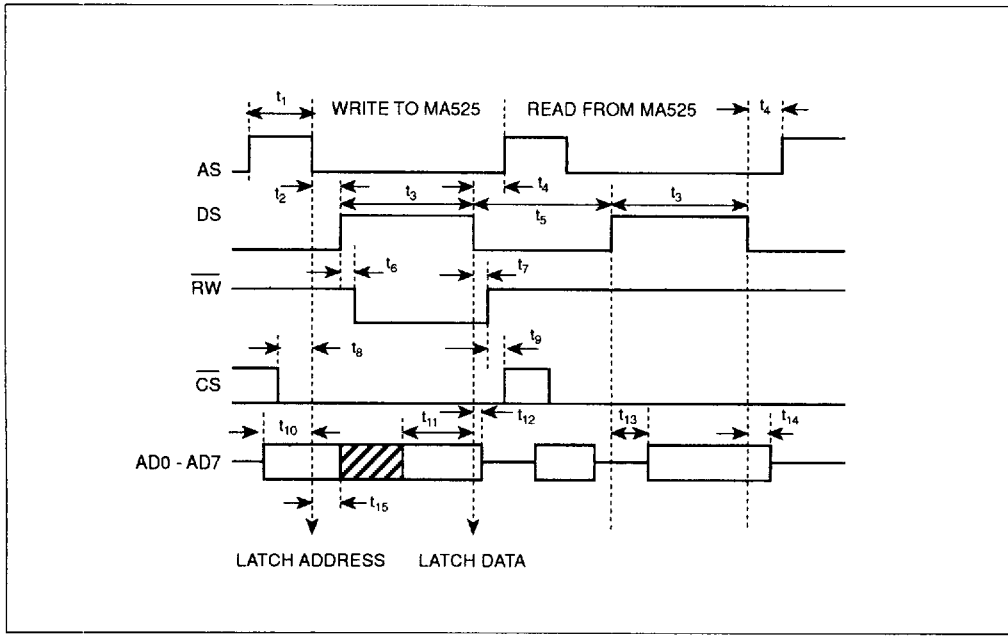


Figure 3: Motorola bus timing diagram

Parameter	Symbol	Min.	Typ.	Max.	Units
AS high period	t_1	50			ns
Delay time, AS low to DS high	t_2	40			ns
DS high period	t_3	40			ns
Delay time, DS low to AS high	t_4	10		50µs	ns
DS low period	t_5	165			ns
DS high to R/W low setup time	t_6	15			ns
R/$\overline{W}$ hold time	t_7	10			ns
$\overline{CS}$ setup time	t_8	40			ns
$\overline{CS}$ hold time	t_9	0			ns
Address setup time	t_{10}	30			ns
Address hold time	t_{15}	10			ns
Write data setup time	t_{11}	50			ns
Write data hold time	t_{12}	0			ns
Output data response time	t_{13}		55	80	ns
Output data removal time	t_{14}		35	50	

The address is latched by the falling edge of the AS line. Data is written from the bus into the MA525 when R/$\overline{W}$ is low on the falling edge of DS (providing $\overline{CS}$ is low). Data can be read from the MA525 when R/$\overline{W}$ is high on the falling edge of DS. All bus timings are quoted with 30pF capacitance to V_{SS}.

Table 3: Motorola bus timings at V_{DD} = 5V, T_{amb} = +25°C

REGISTER ADDRESSING

AD_3 - AD_0	Register	Type	Function
0000	R0	Write only	Digit buffer
0001	R1	Write only	Dial conditions
0010	R2	Write only	Control
0011	R3	Write only	Output Configuration
0100	R4	Write only	Access pause time
0101	R5	Write only	DTMF dialling
0110	R6	Write only	HSW response time
0111	R7	Write only	TBR (Flash) time
1000	R8	Write only	IDP time
1001	R9	Write only	Single tone O/P
1010	R10	Read only	Status

Table 4: MA525 register addressing

Default register conditions are automatically set in all programmable registers on power-up and remain valid until a register is reprogrammed In addition the dial store is cleared

Read commands to a 'write only' register and write commands to a 'read only' register will be ignored

Note that register 11 is provided for in-house test purposes and should not be used during normal device operation. If a register number greater than 11 is addressed, the command will be ignored and the ERROR bit raised.

REGISTER FUNCTIONS

(A summary showing register functions and calculations is given on page 1-85)

It is recommended that parameters set in Registers 1, 3, 4, 5, 7 and 8 should not be changed while dialling is in progress. However, parameters can be changed during the same call provided that dialling is not active (i.e. if the BUSY bit in the status register is at 0') at the time -there is no need to go on-hook or to set the DISCON bit before changing parameters.

If parameters in registers 1, 3, 4, 5, 7 or 8 are changed during dialling, misdialling may occur but the device will operate normally when the dial sequence is complete. The ERROR flag will not be raised in this case.

REGISTER 0 - DIGIT BUFFER

Digits to be sent to the dial store should be loaded into Register 0. To load a TBR or a Pause into the dial store the appropriate bits should be set in register 2. Digits will be sent to the dial store in the order in which they are loaded into registers 0 and 2.

Digits may be loaded into the dial store in blocks of up to 22 digits. If more than 22 digits are loaded in total it is important not to perform a last number redial to ensure correct operation.

Digits can be loaded into Register 0 either before or after the DIAL Bit is set in Register 2. Digits loaded after the DIAL bit is set will be concatenated with any digits yet to be dialled. However, if digits are loaded whilst a Last Number Redial is being dialled the digits will be ignored.

Each digit can be loaded into the dial store using a handshaking routine. As each digit is loaded into register 0 (or bits 2 and 3 in register 2) the BUF bit is set in the status register (Register 10). When the digit has been accepted into the dial store from Register 0, the BUF bit is cleared. indicating that the next digit can be loaded into register 0. Alternatively digils can be loaded directly without monitoring the BUF bit providing that the timing requirements are met (see a.c. conditions). In either case the ERROR bit in the Status Register will be set if an attempt is made to load a digit while the BUF bit is set to 1 and the digit will not be accepted.

Up to 21 undialled digits can be held in the dial store at a time. Once the dial store is full the BUF bit will be set to 1 and no further digits can be loaded until it is reset to 0 either because space becomes available (due to digits having been dialled out) or until the device is sent onhook (in Phone mode) or DISCON is set to 1 (Modem mode).

Codes *,A,B,C,D and # are illegal in LD mode and will not be accepted into Register 0 while the device is set to LD mode. If an attempt is made to do this the ERROR bit will be set in the Status Register.

Bits 3210	Code	Digit	Comment
0000	0	0	0 = 10 pulses in LD mode
0001	1	1	
0010	2	2	
0011	3	3	
0100	4	4	
0101	5	5	
0110	6	6	
0111	7	7	
1000	8	8	
1001	9	9	
1010	10	*	Not allowed in LD mode
1011	11	A	Not allowed in LD mode
1100	12	B	Not allowed in LD mode
1101	13	C	Not allowed in LD mode
1110	14	D	Not allowed in LD mode
1111	15	#	Not allowed in LD mode

Table 5: Register 0 - digit buffer

REGISTER 1 - DIAL CONDITION REGISTER

Bit	Name	Default	Function
0	USE	0	Phone or Modem use 0 = Phone, 1 = Modem
1	B/M	0	Break/Make ratio 0 = 2:1, 1 = 3:2
2	DS	0	Dialling Speed (LD) 0 = Normal, 1 = Double
3	MODE	0	LD/DTMF dialling 0 = LD, 1 = DTMF

Table 6: Register 1

If the USE bit is cleared whilst the LINE output is at a '1' state, the LINE output will not be cleared Normal Phone Mode operation will resume after the DISCON bit is next set.

Bit 2 of register 1 defines the dialling speed in LD only. If this bit is cleared the dialling speed will be set to 10 impulses per second and all other timings will be as per the relevant registers. If the DS bit is set however, the dialling speed will be 20 impulses per second and all other timings will also be halved.

REGISTER 2 - CONTROL REGISTER

Bit	Name	Default	Function
0	DIAL	0	Start dial sequence 1 = Start
1	DISCON	0 1	Disconnect 0 = Seize line, 1 = Disconnect line
2	ACCESS	0	Load access pause = 1
3	TBR	0	Load TBR (Flash) = 1

Table 7: Register 2

When the DIAL bit is set to 1, dialling will start, assuming DISCON is set to 0 If dialling is terminated either by the HSW being timed out (in Phone mode) or by sening the DISCON bit to 1 (in both modes), the dial bit is automatically reset to 0. Note that forcing the DIAL bit low using the microprocessor interface does *not* terminate dialling

In Phone mode, setting the DISCON bit simply terminates dialling immediately. The device outputs then revert to their normal 'off-hook and idle' states If, when programming Register 2 in Phone mode an attempt is made to set both the DIAL and DISCON bits to '0', the command will be ignored

In Modem mode, setting the dial bit causes LINE to make a low to high transition after 6.6ms. After dialling is completed, the LINE output will remain high, thereby holding the line for subsequent speech/data interchange DISCON may be used at any time to relinquish the line thus ending the call Further digits may be loaded and dialled at any time whilst LINE is high.

If, when programming register 2, an attempt is made to set both the DIAL and DISCON bits to '1', DIAL will be set to '0' and DISCON to '1', i.e. DISCON takes priority. The DIAL / DISCON protocol is shown in State Diagram form in Figs 4 and 5. If PAUSE and TBR bits are set simultaneously, the write operation will be ignored and the ERROR flag raised.

If an LNR is required after setting DISCON, simply set the DIAL bit In order to prevent the device redialling the previous number, it is necessary to clear the DISCON bit f irst .

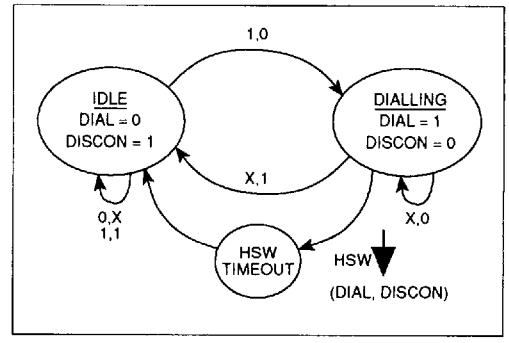


Figure 4: Finite state diagram - Phone mode

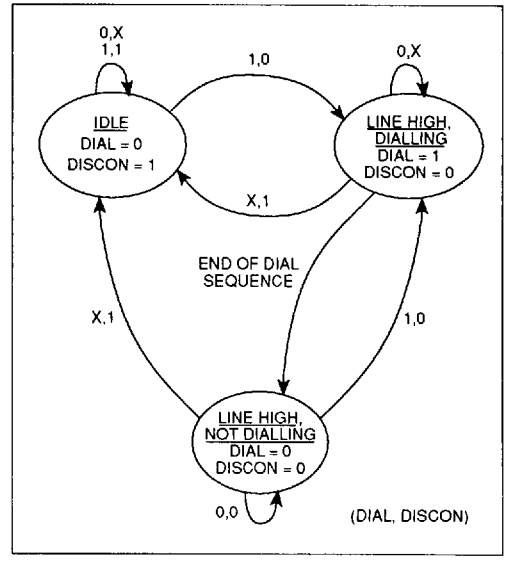


Figure 5: Finite state diagram - Modem mode

Note that since TBR and Pause are treated as normal digits, the device places a Pre-Digit Pause before, and an Inter-Digit Pause after the TBR/Pause whilst in LD mode. In DTMF mode, a tone pause period (as defined by register 5) is placed both before and after the TBR/Pause.

On power up, if the DIAL bit is set without first loading any digits in LD mode, the device defaults to dialling an access digit (9).

WARNING: No response will be obtained if Access Pause or TBR is entered as the first digit in a string with nondefault values in either Pause Duration register or TBR Duration register whilst in DTMF mode. If this condition is inadvertantly invoked it may be cleared by setting the DISCON bit (in both Phone and Modem modes), toggling the HSW input (in Phone mode only) or by powering down the MA525.

REGISTER 3 - OUTPUT CONFIGURATION REGISTER

Bit	Name	Default	Function
0	IE	0	Interrupt Enable 0 = Disable, 1 = Enable
1	LS	0	LINE output polarity 0 = Normal. 1 = Invert
2	MS	0	MUTE output polarity 0 = Normal, 1 = Invert
3	KS	0	MASK output polarity 0 = Normal, 1 = Invert

Table 8: Register 3

Disabling the Interrupt Enable simply disables both the IRQ output (i.e. high-impedance open-drain) and the IRQF bit in the Status Register.

REGISTER 4 - ACCESS PAUSE DURATION

Code	Default	Function
1 - 15	1 (ie. 500ms)	Set length of Access Pause. Duration = Code x 500ms.

Table 9: Register 4

If code 0 is loaded, the Access Pause duration will be set to the default value and the ERROR bit will be set in the status register.

If pauses longer than 7.5 seconds are required, Pauses may be programmed more than once in succession. This will give a longer 'seamless' pause with no transitions on any device outputs.

REGISTER 5 - DTMF DURATION

Bit	Name	Default	Function
0 - 3	Duration	15 (100ms)	Set tone on/off period. Period = (Code x 6.67) ms.

Table 10: Register 5

Register 5 sets both the active tone period and the pause time between tones. Note that if code 0 is loaded the DTMF duration is set to the default value and the ERROR bit will be raised in the Status Register.

REGISTER 6 - HOOKSWITCH RESPONSE TIME

Code	Default	Function
0 - 15	2 (ie. 200ms)	Set Hookswitch timeout period Duration = Code x 100ms.

Table 11: Register 6

The hookswitch timeout period is the time taken between the hookswitch going low and the on-hook condition being recognised by the MA525. It is used to differentiate between short line breaks due to electrical noise (or line polarity reversal) and the user placing the handset on-hook. If the HSW input returns high before the timeout period has elapsed then the on-hook condition is not recognised. The status of the HS bit in the status register reflects the immediate status of the HSW input rather than whether the device recognises the on-hook or off-hook condition. It should be noted that the actual hookswitch response time will vary between the nominal duration set and up to 100ms greater than this (eg. if 200ms is set the response time is 200-300ms).

Parameters set in Register 6 should not be changed when a hookswitch timeout is occuring, as this may give an unpredictable timeout period. If this occurs, however, the device will behave as normal after the timeout is complete.

REGISTER 7 - TIMED BREAK RECALL (FLASH) PERIOD

Code	Default	Function
0 - 15	1 (ie. 100ms)	Set TBR (Flash) Period. Duration = Code x 100ms.

Table 12· Register 7

If code 0 is loaded, the TBR (Flash) Period will be set to the default value and the ERROR bit will be set in the status register.

REGISTER 8 - INTER-DIGIT PAUSE DURATION

Code	Default	Function
0 - 15	8 (ie. 800ms)	Set IDP duration (LD dialling) Duration = Code x 100ms.

Table 13: Register 8

The IDP duration applies only to LD dialling If code 0 is loaded, the IDP duration will be set to the default value and the ERROR bit will be set in the status register

REGISTER 9 - SINGLE TONE OUTPUT

Code	Default	Function
0 - 7	Disable	Disable single tone output
8		Enable 697 Hz output
9		Enable 770 Hz output
10		Enable 852 Hz output
11		Enable 941 Hz output
12		Enable 1209 Hz output
13		Enable 1339 Hz output
14		Enable 1477 output
15		Enable 1663 Hz output

Table 14: Register 9

When selected the single tone output is generated from the DTMF output The output level is therefore dependent upon whether the particular tone is in the high or low frequency group (see AC characteristics). Once selected, the single tone output is continuous until it is either disabled or until another single tone is selected. Single tones cannot be selected in LD mode.

Single tone outputs are active whether the device is on or off-hook.

During single tone outputs the BUSY bit is not set In addition, the device outputs (MUTE,MASK and LINE) will remain inactive.

If the DIAL bit is set whilst a single tone is active, the device will behave as it it is dialling (i.e. BUSY bit set, MUTE active et cetera) although the single tone will take priority on the TONE pin. It is therefore important to disable single tones before a DTMF dialling sequence.

REGISTER 10 - STATUS REGISTER (READ ONLY)

Bit	Name	Function
0	BUSY	Indicates dialling in progress: 1 = Busy
1	ERROR	Indicates programming error: 1 = Error
2	HS	Indicates hookswitch status: 0 = available 1 = in use
3	BUF	Indicates digit buffer status: 0 = available 1 = in use
7	IRQF	Interrupt request set flag: 0 = clear 1 = set

Table 15: Register 10

BIT 0: BUSY

The BUSY bit is active (i.e set to '1') during dialling ot digits, TBR and Pauses in either LD or DTMF modes.

The BUSY bit is automatically reset to '0' when:

1. A dialling sequence is complete.
2. A dialling sequence is terminated by setting the DISCON bit (Reg 2) to 1.
3. A dialling sequence is terminated by an on-hook timeout

BIT 1: ERROR

In general, the ERROR bit is raised when an illegal operation is performed. Some operations, such as changing certain registers whilst dialling, are not fundamentally illegal but are nevertheless not recommended Such errors do *not* raise the ERROR flag

The ERROR bit is always reset by reading the Status Register.

The ERROR bit is set to 1 under the following conditions:

1. When an attempt is made to load illegal digits into the digit buffer (Reg0) while the device is set to LD mode (i.e. A,B,C,D,*or #)
2. When an attempt is made to dial an illegal digit in LD mode (i.e. A,B,C,D,*or #) loaded whilst the device is in DTMF mode . If an attempt is made to load a digit into the dial store while the BUF bit is set to 1.
4. If an attempt is made to load code 0 into registers 4, 7 or 8.
5. When a register addressing error is made (i.e. if a register number greater than 11 is addressed).

BIT 2: HS

The HS bit is set to 1 immediately the HSW input goes high. HS remains high until the HSW input goes low, when it will be reset to 0. The status ot the HSW input has no relevance to device operation when in Modem mode, but the HS bit remains operational If DISCON is invoked during a hookswitch timeout the device will assume the on-hook condition instantly, i.e. DISCON takes priority over the hookswitch timeout.

BIT 3: BUF

When the BUF bit is set to 0, this indicates that a digit (or a TBR or Pause) can be loaded into the dial store via Register 0, the digit buffer (or via Register 2)

When the BUF bit is set to 1 this indicates that the temporary digit buffer is not available for use and that digits should therefore not be loaded If a digit is loaded while BUF = 1, it will not be accepted and the ERROR bit and IRaF will be set.

The BUF bit is set to 1 under the following conditions

1. While the MA525 is accepting a digit from the temporary digit buffer to the dial store. A handshaking procedure, as shown in Fig. 6, can be used to load digits from the digit buffer to the dial store. Such handshaking will ensure correct loading of the digits whether or not the MA525 oscillator is running at the time of first loading. Providing that the oscillator is running (see Oscillator Circuit section) handshaking need not be used so long as the buffer timing constraints are observed.
2. When the dial store is full and therefore unable to receive any further digits. As soon as a dial store location becomes available the BUF bit will be reset to 0 and the digit previously held in the buffer will be transferred to the dial store

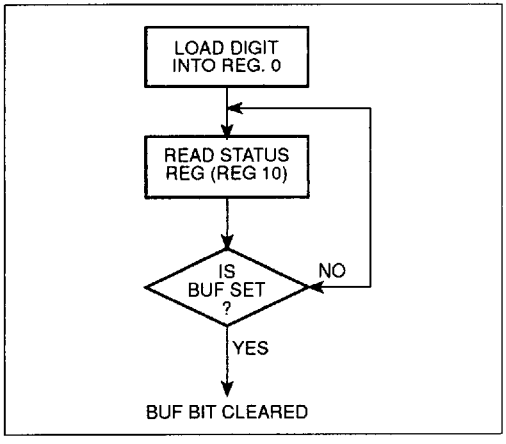


Figure 6: Digit loading handshaking procedure

BIT 7: IRQF

The IRQF bit simply reflects the status of the $\overline{IRQ}$ output. The IRQF bit is set to 1 ($\overline{IRQ}$ = 0) under the following conditions:

1. Whenever the ERROR bit is set to 1.
2. Whenever a dialling sequence is completed (but not if DISCON is asserted or the hookswitch is taken low before the sequence is complete).

The IRQF bit and $\overline{IRQ}$ are returned to their inactive states by reading the status register.

Note that if IRQF goes high and is subsequently cleared as a consequence of a good sequence, the Status Register will hold the data relating to the latter (correct) operation and not the former (incorrect) operation.

LAST NUMBER REDIAL FACILITY

The MA525 will dial the previous contents of the dial store if:

(i) No digits are loaded between HSW being timing out (or DISCON being set) and DIAL being set in Phone Mode.(See Fig. 7).

(ii) No digits are loaded between DISCON being set and DIAL being set in Modem Mode.(See Fig. 8).

Note:

(i) Digits cannot be appended to an LNR.

(ii) The presence of a Timed Break Recall (TBR) or Access Pause does not affect the LNR - they are simply treated as another digit

OSCILLATOR CIRCUIT

The oscillator circuit requires an external 560kHz ceramic resonator between OSC and Vss. No other components should be used. Please see your resonator supplier who will recommend a suitable resonator type. The OSC pin may also be driven by an external logic signal if required .

Under normal MA525 operation, the oscillator will be started during dialling or digit loading sequences and shutdown afterwards in order to conserve power and reduce possible crosstalk to speech or other sensitive circuits.

Thus the oscillator will be started by:

1. The presence of a digit in the digit buffer. (whilst offhook or in Modem mode).
2. DIAL bit being set (whilst off-hook or in Modem mode).
3. Whilst performing a hookswitch timeout (whilst in Phone mode only).
4. Beginning a Single Tone output.

The oscillator will be shut-down following:

1. A hookswitch timeout (in Phone mode only).
2. DISCON bit being set.
3. Completion of a dialling sequence.
4. BUF being cleared Note that if a 23rd digit is loaded, it will reside in the buffer until a space becomes available for it in the dial store. In the meantime, BUF will be set and the oscillator will run continuously. To ensure minimum crosstalk with any speech circuitry, it is advisable to avoid this situation.
5. Ending a Single Tone output.

Note that reading the Status Register will not restart the oscillator. Hence data held in this Register will not be updated after the oscillator has been shut-down.

Since the oscillator is stopped whilst the hookswitch is down in Phone mode it is not possible to load digits into the dial store. A single digit can be held in the buffer, however, until the device is next taken off-hook. Digits may, however, be loaded at any time whilst in Modem mode irrespective of hookswitch and DISCON status.

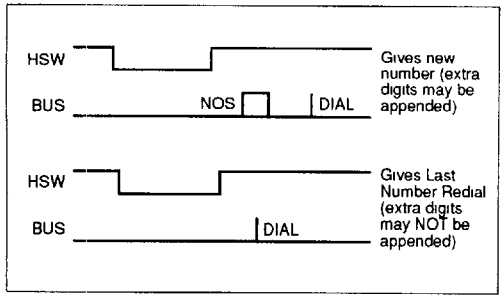


Figure 7: LNR protocol - Phone mode

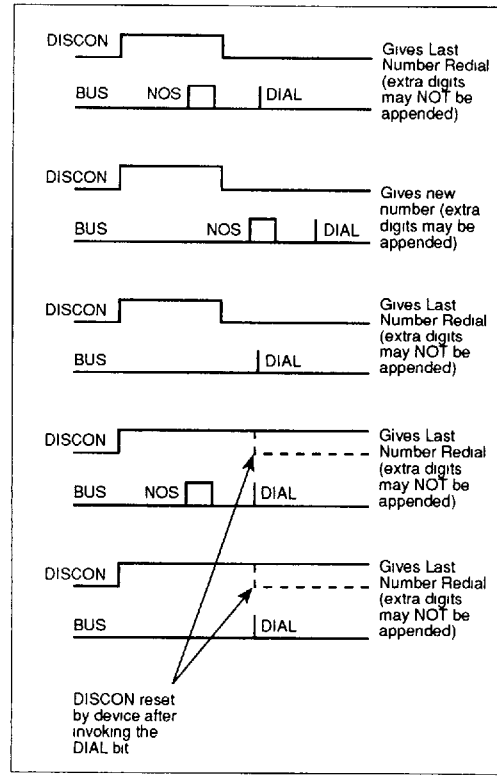


Figure 8: LNR protocol - Modem mode

Reg no.	Name	Bit 3 (MSB)	Bit 2	Bit 1	Bit 0 (LSB)
1	DIAL CONDITIONS	**MODE** 0 PULSE 1 DTMF	**DIAL SPEED** 0 NORM 1 DOUBLE	**B/M RATIO** 0 = 2:1 1 = 3:2	**USE** 0 PHONE 1 MODEM
2	CONTROL REGISTER	**TBR**	**ACCESS PAUSE**	**DISCON**	**DIAL**
3	OUTPUT CONFIGURATION	**MASK POLARITY** 0 NORM 1 INV	**MUTE POLARITY** 0 NORM 1 INV	**LINE POLARITY** 0 NORM 1 INV	**IE** 0 DISABLE 1 ENABLE
10	STATUS REGISTER	**BUF** 0 AVAIL 1 IN USE	**HS** 0 OFFHK 1 ONHK	**DIGIT ERROR**	**BUSY BIT**

Table 16 Summary of registers 1, 2, 3 and 10 functions

Reg. no.	Function	Coding
4	ACCESS PAUSE DURATION	CODE x 500ms
5	DTMF DURATION	CODE x 6.67ms
6	HOOKSWITCH RESPONSE TIME	CODE x 100ms
7	TBR (FLASH) DURATION	CODE x 100ms
8	INTER-DIGIT PAUSE DURATION	CODE x 100ms

Table 17: Summary of registers 4, 5, 6, 7 and 8 functions

Code	Register 9 - Single Tone Output
0-7	Disable single tone output
8	Enable 697 Hz output
9	Enable 770 Hz output
10	Enable 852 Hz output
11	Enable 941 Hz output
12	Enable 1209 Hz output
13	Enable 1336 Hz output
14	Enable 1477 Hz output
15	Enable 1663 Hz output

Table 18: Register 9 summary

PULSE DIALLING IN PHONE MODE

The MASK output is provided in order to disable the speech circuit during LD (Pulse) dialling. Consequently, the MASK output is normally at logic '0' in the off-hook condition, but changes to logic '1' during LD dialling. MASK also changes to logic '1' in order to signal a Timed Break Recall (Flash) to the line.

LD dialling is signalled on the LINE output: a break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. When not dialling, the LINE output sits at logic '0'.

Both MUTE and TONE outputs remain low during LD dialling. LINE, MUTE and MASK outputs may be inverted independently if desired.

If the HSW input goes low whilst dialling, the LINE and MASK outputs continue as normal until the hookswitch timeout occurs. If the hookswitch goes high again before the timeout, LINE and MASK will continue uninterrupted. The BUSY bit (Reg 10) will remain high until either the dialling sequence finishes internally or until a hookswitch timeout occurs (whichever comes first).

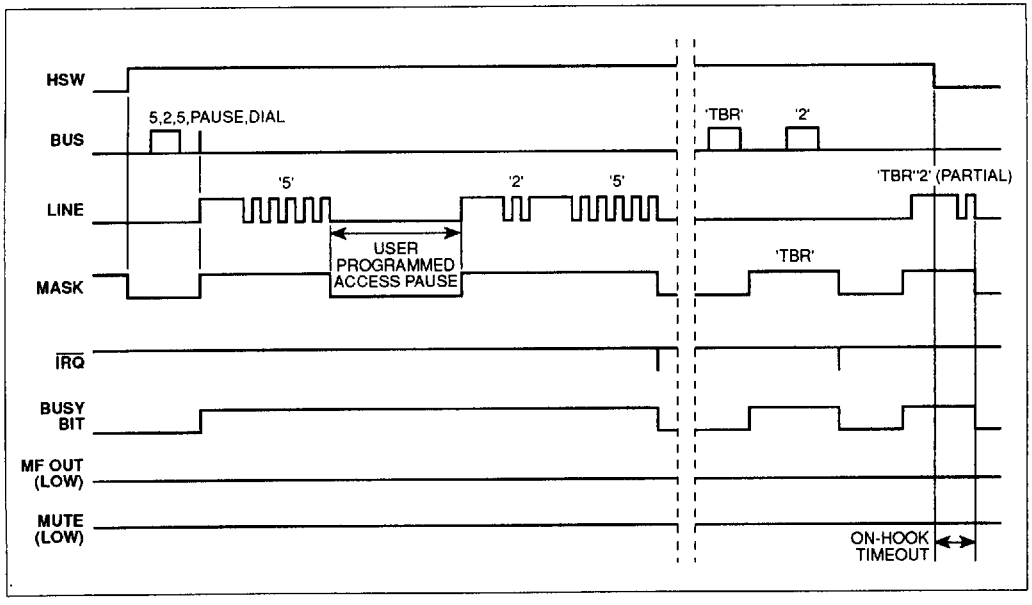
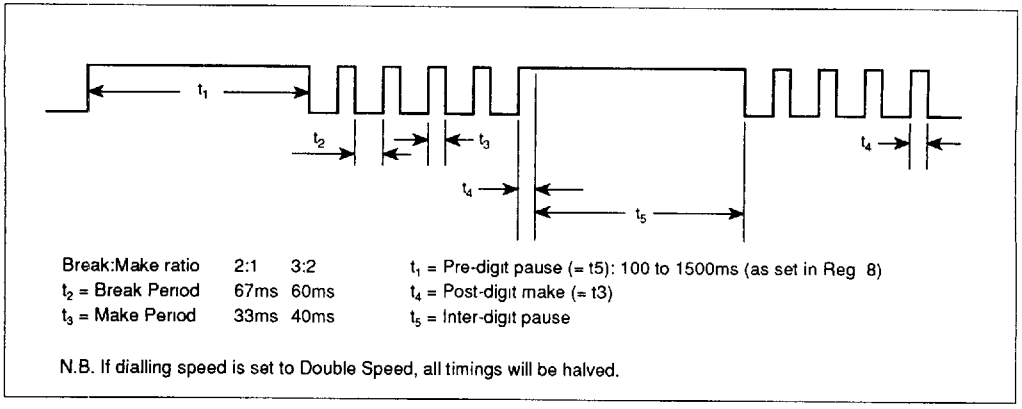


Figure 9: LD/phone mode timing diagram



Break:Make ratio	2:1	3:2	t_1 = Pre-digit pause (= t5): 100 to 1500ms (as set in Reg 8)
t_2 = Break Period	67ms	60ms	t_4 = Post-digit make (= t3)
t_3 = Make Period	33ms	40ms	t_5 = Inter-digit pause

N.B. If dialling speed is set to Double Speed, all timings will be halved.

Figure 10. Timing data

PULSE DIALLING, IN MODEM MODE

The MASK output is provided in order to disable the speech circuit during LD dialling. Consequently, the MASK output is normally at logic '0' in the off-hook condition, but changes to logic 1' during LD dialling. MASK also changes to logic '1' in order to signal a Timed Break Recall (Flash) to the line.

Both MUTE and TONE remain low during LD dialling. LINE, MUTE and MASK may be inverted independently if desired.

The status of the HSW input is irrelevant in Modem mode. However, HSW status can still be read from register 1 O.

The LINE output is used to control the on/off-hook status and for LD dialling. The line will be seized when dialling starts. A break is signalled by a logic '0', make periods and IDP times are signalled by a logic '1'. After dialling finishes the LINE output will remain high until the line is disconnected by setting the DISCON bit to '1'.

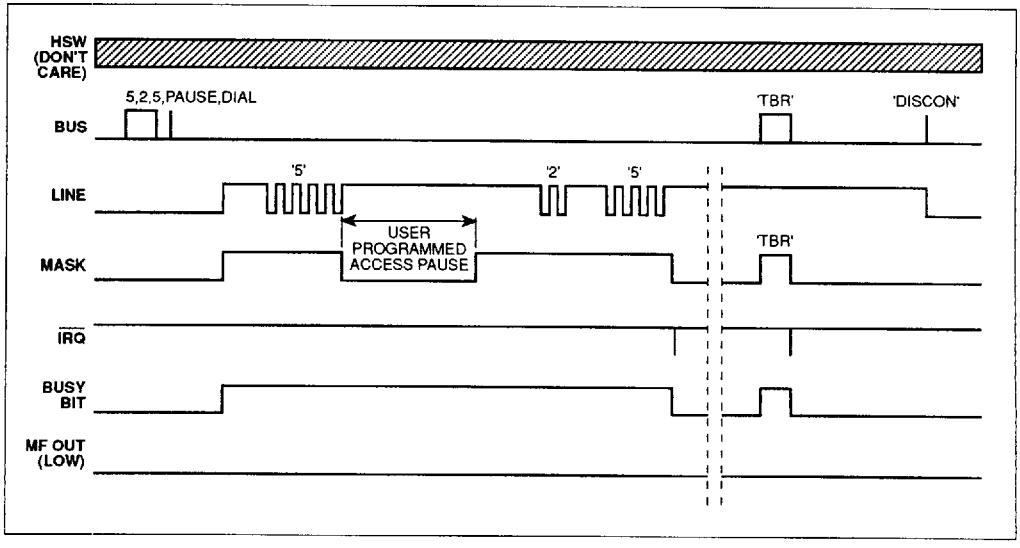


Figure 11: LD/modem mode timing diagram

DTMF DIALLING IN PHONE MODE

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission The LINE output remains low during tone transmission.

The MF OUT output rises to its DC level as soon as the MODE bit in register 1 is set and is kept there between tone bursts. This is to avoid transients at the beginning and end of tone bursts.

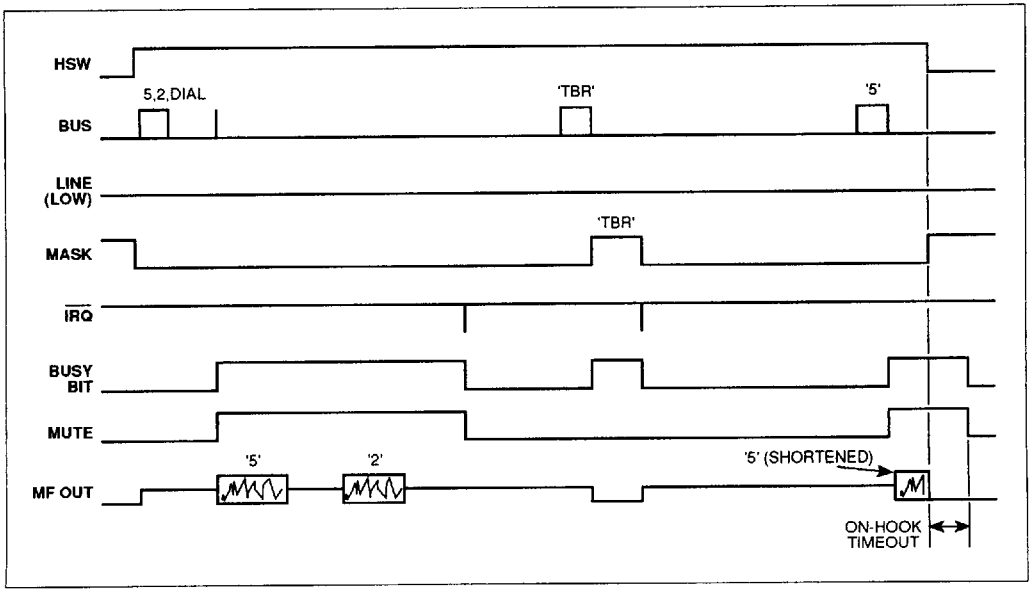


Figure 12: DTMF/phone mode timing diagram

	1209Hz	1336Hz	1447Hz	1633Hz
697Hz	1	2	3	A
770Hz	4	5	6	B
852Hz	7	8	9	C
941Hz	*	0	#	D

Table 19: Tone frequencies

Nominal frequency (Hz)	697	770	852	941	1209	1336	1477	1633
Deviation from nominal (%)	-0 07	-0.10	+0.19	-0.15	-0.17	-0.20	-0.22	-0.31

NOTE:
There will be an additional frequency error caused by any deviation of the resonator frequency from the nominal 560kHz.

Table 20· Tone frequency accuracy

PULSE DIALLING IN MODEM MODE

During DTMF dialling the MUTE output goes to logic '1' and remains there for the duration of the tone transmission. The LINE output is used to control the on/off hook status whilst MF OUT is used for tone transmission

The MF OUT output rises to its DC level as soon as the MODE bit is set and remains there during tone bursts. This is to avoid transients at the beginning and end of tone bursts.

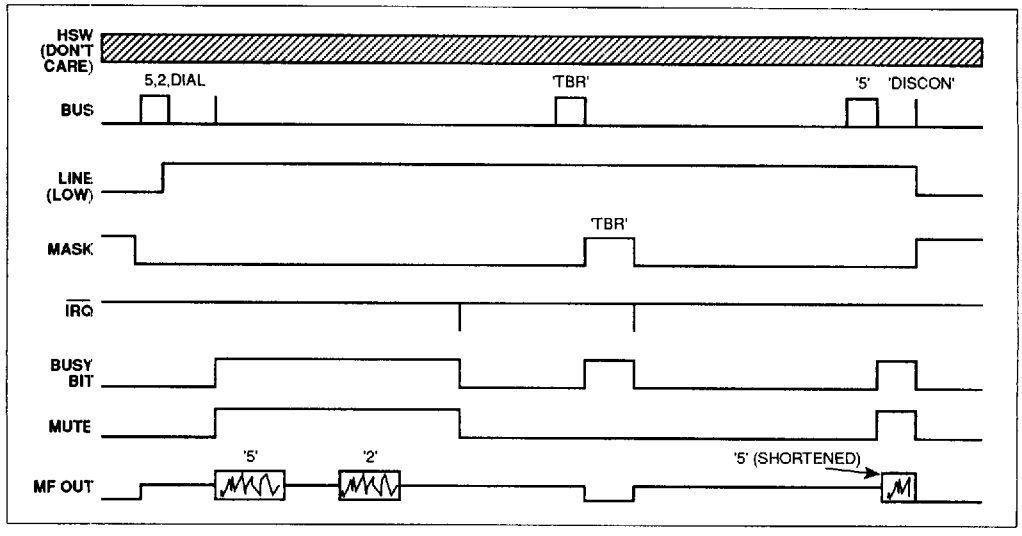


Figure 13: DTMF/Modem mode timing diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): T_{amb} = 25°C

DC CHARACTERISTICS AT V_{DD} = 2.5V

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply Current:	On-hook		< 0.2	5.0	µA	V_{DD} = 2.0V. See note 1.
	Off-hook		1 5		µA	MF OUT low
	MF tone sending			1.0	mA	
	LD impulsing			200	µA	
Output high voltage (MASK, MUTE and LINE outputs)		2.2		–	V	I = -1 mA
Output low voltage (MASK, MUTE and LINE outputs)				0 3	V	I = + 1 mA
MF OUT DC level during tone sending			$0.5V_{DD}$			
MF OUT output resistance			15	20	kΩ	
Microprocessor interface: input high		-	2.0	V_{DD}	V	
Input low		-	0	0.5	V	
Output high		2.3	-	-	V	I = -50µA
Output low		-	-	0.2	V	I = + 50µA
$\overline{IRQ}$ Output	Output low			0.2	V	I = + 50µA
	Output high leakage	-	-	1	µA	

NOTE:

1. Specially tested versions with guaranteed lower on-hook supply current are available

DC CHARACTERISTICS AT V_{DD} = 5V

Characteristic		Min.	Typ.	Max.	Units	Condition
Supply Current:	On-hook		1.5		µA	MF OUT low
	MF tone sending		0.5	2.0	mA	
	LD impulsing			0.5	mA	
Output high voltage (MASK, MUTE and LINE outputs)		4.55	4.8		V	I = -10 mA
Output low voltage (MASK, MUTE and LINE outputs)			0.2	0.45	V	I = + 10 mA
Microprocessor interface: input high		-	2.0	V_{DD}	V	
	Input low	-	0	0.8	V	
	Output high	4.6	-	-	V	I = -1mA
	Output low	-	-	0.4	V	I = + 1mA
$\overline{IRQ}$ Output	Output low	-	-	0.4	V	I = + 1mA
	Output high leakage	-	-	1	µA	

NOTE:
2. All other characteristics are as specified at V_{DD} = 2.5V given on page 1-89.

AC CHARACTERISTICS

Characteristic	Min.	Typ.	Max.	Units	Condition
Tone output at VDD = 2 5V: LOW group	285	320		mV rms	No load
High group		405	455	mV rms	No load
Tone output at VDD - 5V: LOW group	570	640		mV rms	No load
High group		810	910	mV rms	No load
High-to-Low group amplitude ratio (pre-emphasis)	1.5	2	2.5	dB	All V_{DD}, see note 3
Total harmonic distortion: 0-4 kHz		1 5		%	All V_{DD}
0-10 kHz		25		%	All V_{DD}
0-50 kHz		50		%	All V_{DD}
0-200 kHz	_	65	10	%	All V_{DD}
Oscillator start-up time		< 0.1	1	ms	

NOTE:
3. Typical value varies slightly dependent upon particular tone pair.

RECOMMENDED OPERATING TEMPERATURES

Condition		Min.	Typ.	Max.	Units	Notes
Supply Voltage:	On-hook	1.8		5.7	V	For memory retention
	Off-hook	2.4		5.7	V	
Hookswitch Input:	On-hook			$0.2V_{DD}$ V		
	Off-hook	$0.8V_{DD}$				
Oscillating frequency			560		kHz	
Digit load to dial store accept time (BUF high time)				36	µs	See note 4

NOTE:
4. Assumes oscillator is running. If oscillator is not running, add start-up time given in AC Characteristics above.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}-V_{SS}	-0.3 to 6.5V
Voltage on any pin (except HSW)	V_{SS} - 0 3V to V_{DD} + 0 3V
Voltage on HSW pin (See note 5)	V_{SS}- 0.3V min
Current at any pin (except HSW)	±1 mA
Storage temperature	-55°C to +125°C
Operating temperature range	-10°C to +55°C

NOTES

5. A diode is internally connected between this pin and V_{DD}. Provided current is externally limited to 300µA max no damage will occur.

6. Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the Electrical Characteristics, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.