

SAW Based Clock and Data Recovery Products

TRU 600A

Features

SAW Filter Based Timing Recovery Module

Typical Output Jitter Below 10 ps

Data Rate Output Options from 124.416 Mb/s to 622.08 Mb/s

SONET/SDH Compatible

100K ECL/PECL Compatible Outputs and Inputs

Superior Jitter Tolerance and Transfer Performance

Single Power Supply Operation

External Clock Enable upon LOS

Miniature Ceramic SMD Package (SO-28)

Description

The TRU600A regenerates clean clock and data signals from incoming NRZ data streams, such as those encountered in fiber-optic transmission and telecom applications. The device utilizes SAW filter CDR technology for superior jitter performance.

The clock is extracted from the input NRZ data by first passing it through a frequency doubler to generate sufficient spectral energy at the data rate. The SAW filter (a precision narrow-band filter) then suppresses jitter by rejecting unwanted frequency spectra. The extracted clock is then precisely aligned with the data and the signals are reshaped.

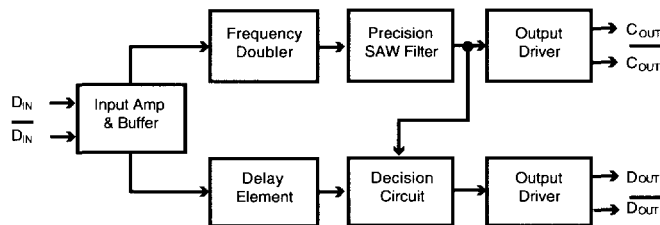
The output is thus free of undesirable jitter and distortion. Unlike phase-locked loop designs, the jitter transfer function is uniquely stable because it is determined by the SAW filter's response, which can be precisely controlled and reproduced.

Performance Characteristics (TA = -40 °C to 85 °C)					
Specifications	Sym	Min	Typ	Max	Unit
Nominal Clock Frequency	f_N	124.416	-	622.08	MHz
Supply Current	I_{EE}	50	65	75	mA
Supply Voltage	V_{CC}	4.5	5	5.5	V
Data Input Low	V_{IL}	-1.81	-	-1.48	V
Data Input High	V_{IH}	-1.17	-	-0.88	V
Data/Clock Output Low ¹	V_{OL}	-1.95	-	-1.63	V
Data/Clock Output High ¹	V_{OH}	-1.03	-	-0.88	V
Input Clock Deviation ²	D_C	-200	-	200	ppm
Clock/Data Alignment ³	T_{DCA}	-100	-	100	ps
Data/Clock Rise/Fall Time ⁴	$T_{R/F}$	275	375	575	ps
Clock Duty Cycle	DC	45	-	55	%
Acquisition Time ⁵	T_A	-	-	2	μ s
Clock Random Jitter ⁶	J_C	-	10	-	ps rms
Storage Temperature ⁷	T_S	-55	-	125	°C
Soldering Temp. /Time ⁷	T_{LS}	-	-	240/10	°C/s
Absolute Max Supply Volt	$V_{CC}-V_{EE}$	0	-	8	V
ESD Rating (HBM,CDM)	-	-	-	1	kV

Mechanical and Environmental Qualification

Parameter	Test Method
Shock and Vibration	MIL-STD-883C, 2002.3, Test B, C
Solderability	MIL-STD-883C, 2003.5
Gross and Fine Leak	MIL-STD-883C, 1014.7, 100%
Resistance to Solvents	MIL-STD-883C, M2016

Simplified Block Diagram



- 1 Measured with respect to V_{CC} with a 50 Ω load to $V_{CC}-2V$. See Fig 6 and 7. ECL levels are specified for D.C. performance, 50 mV should be added for dynamic performance.
- 2 Allowable input clock variation with respect to nominal clock Frequency(f_N), -40°C to 85°C.
- 3 Alignment of clock and data output.
- 4 20% to 80%.
- 5 Time required to achieve valid data and clock outputs with a 50% input transition density.
- 6 Measured with 2²³-1 pseudorandom word (PRW) data input.
- 7 Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

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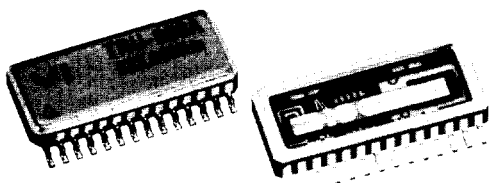
Pinout Information

Pin	Function
2	Test Data In (TDI)
4	Data Out (D_{OUT})
6	Data Out (D_{OUT})
8	Test Clock In (TCI)
10	Clock Out (C_{OUT})
12	Clock Out (C_{OUT})
1,3,5,7,9,11, 13,15,17,18, 20,22,24,26, 27,28	Case Ground (GND)
14	External Clock Enable (ECE)
16	Positive Supply Voltage (V_{CC})
19	Negative Supply Voltage (V_{EE})
21	Positive Supply Voltage (V_{CC})
23	Data Input (D_{IN})
25	Data Input (D_{IN})

*Standard

Frequency (MHz)	Part Number
124.416	107316424
155.520	107208670
155.520 (Tape and Reel)	106859002
278.528	107316440
311.040	107097933
622.080	106859028
622.080 (Tape and Reel)	107208662

* Other frequencies available upon request



Outline Drawing

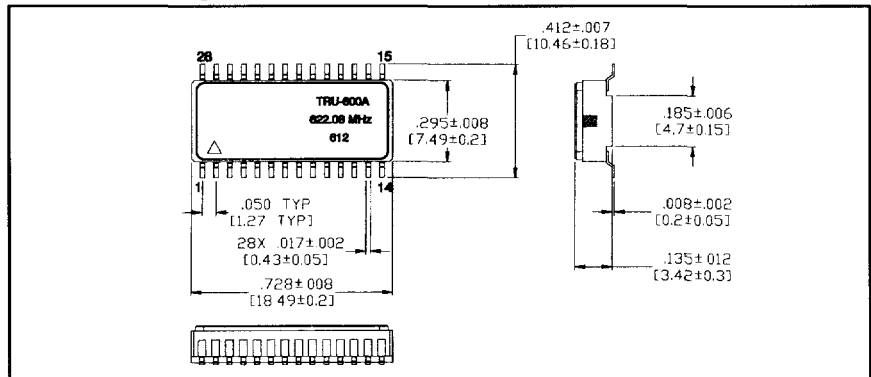


Figure 3 Jitter Transfer and 4 Jitter Tolerance

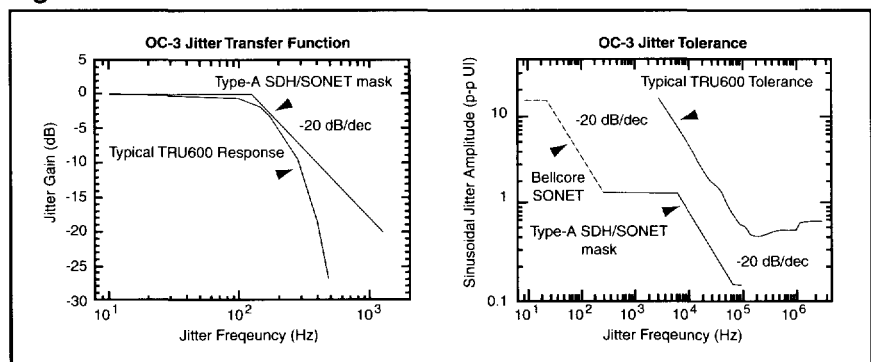


Figure 5 Clock/Data Alignment

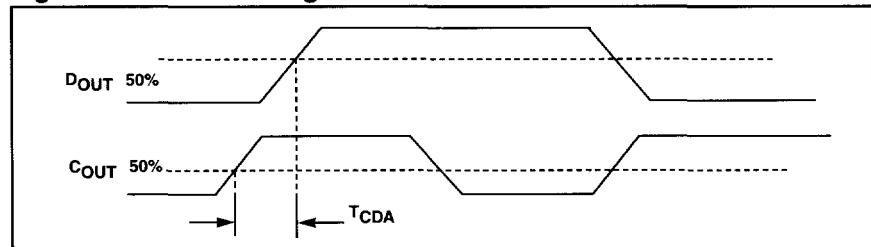
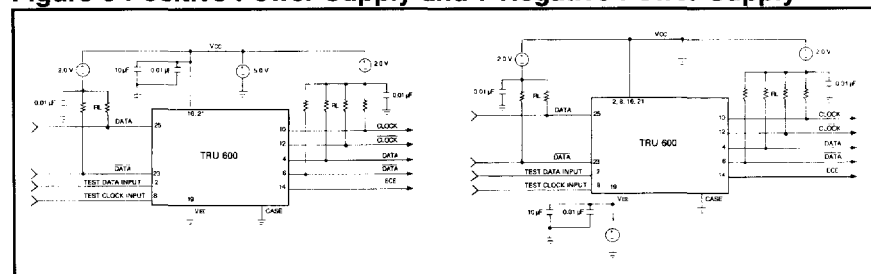


Figure 6 Positive Power Supply and 7 Negative Power Supply



Notes: Pins 16 and 21 provide the power V_{CC} connections. Bypass capacitors should be located close to these pins in the positive supply configuration. When used on a positive supply, all inputs and outputs are ECL referenced to V_{CC} . The data inputs are internally tied to V_{BB} ($V_{CC}-1.3$ V) through 400 ohm resistors. For single ended or ac coupling, external biasing of the inputs is not required. All outputs are open-emitter circuits and may be terminated with any standard ECL configuration. Unused clock and data outputs should be terminated in the same manner as used outputs. Case connections can be made at pins 1, 3, 5, 9, 11, 13, 15, 17, 18, 20, 22, 24, 26, 27, and 28.