

## Description

The CXK77P36L80GB is a high speed CMOS synchronous static RAM with common I/O pins, organized as 262,144 words by 36 bits. This synchronous SRAM integrates input registers, high speed RAM, output latches, and a one-deep write buffer onto a single monolithic IC. Register - Latch (R-L) read operations and Late Write (LW) write operations are supported, providing a high-performance user interface.

All address and control input signals except  $\overline{G}$  (Output Enable) and ZZ (Sleep Mode) are registered on the rising edge of K (Input Clock).

During read operations, output data is driven valid from the falling edge of K, one half clock cycle after the address is registered.

During write operations, input data is registered on the rising edge of K, one full clock cycle after the address is registered.

The output drivers are series terminated, and the output impedance is programmable through an external impedance matching resistor RQ. By connecting RQ between ZQ and V<sub>SS</sub>, the output impedance of all DQ pins can be precisely controlled.

Sleep (power down) mode control is provided through the asynchronous ZZ input. 250 MHz operation is obtained from a single 3.3V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

## Features

- | <u>4 Speed Bins</u> | <u>Cycle Time / Access Time</u> |
|---------------------|---------------------------------|
| -4 (-4A) (-4B)      | 4.0ns / 3.9ns (3.8ns) (3.7ns)   |
| -42 (-42A) (-42B)   | 4.2ns / 4.2ns (4.1ns) (4.0ns)   |
| -43 (-43A) (-43B)   | 4.3ns / 4.5ns (4.4ns) (4.3ns)   |
| -44                 | 4.4ns / 4.7ns                   |
- Single 3.3V power supply (V<sub>DD</sub>): 3.3V ± 5%
  - Dedicated output supply voltage (V<sub>DDQ</sub>): 1.9V typical
  - Extended HSTL-compatible I/O interface with dedicated input reference voltage (V<sub>REF</sub>): 0.85V typical
  - Register - Latch (R-L) read operations
  - Late Write (LW) write operations
  - Full read/write coherency
  - Byte Write capability
  - One cycle deselect
  - Differential input clocks (K/ $\overline{K}$ )
  - Asynchronous output enable ( $\overline{G}$ )
  - Programmable impedance output drivers
  - Sleep (power down) mode via dedicated mode pin (ZZ)
  - JTAG boundary scan (subset of IEEE standard 1149.1)
  - 119 pin (7x17), 1.27mm pitch, 14mm x 22mm Ball Grid Array (BGA) package

## Pin Assignment (Top View)

|   | 1                | 2                 | 3                 | 4               | 5                 | 6                   | 7                |
|---|------------------|-------------------|-------------------|-----------------|-------------------|---------------------|------------------|
| A | V <sub>DDQ</sub> | SA                | SA                | NC              | SA                | SA                  | V <sub>DDQ</sub> |
| B | NC               | NC <sup>(2)</sup> | SA                | NC              | SA                | SA                  | NC               |
| C | NC               | SA                | SA                | V <sub>DD</sub> | SA                | SA                  | NC               |
| D | DQc              | DQc               | V <sub>SS</sub>   | ZQ              | V <sub>SS</sub>   | DQb                 | DQb              |
| E | DQc              | DQc               | V <sub>SS</sub>   | $\overline{SS}$ | V <sub>SS</sub>   | DQb                 | DQb              |
| F | V <sub>DDQ</sub> | DQc               | V <sub>SS</sub>   | $\overline{G}$  | V <sub>SS</sub>   | DQb                 | V <sub>DDQ</sub> |
| G | DQc              | DQc               | $\overline{SBWc}$ | NC              | $\overline{SBWb}$ | DQb                 | DQb              |
| H | DQc              | DQc               | V <sub>SS</sub>   | NC              | V <sub>SS</sub>   | DQb                 | DQb              |
| J | V <sub>DDQ</sub> | V <sub>DD</sub>   | V <sub>REF</sub>  | V <sub>DD</sub> | V <sub>REF</sub>  | V <sub>DD</sub>     | V <sub>DDQ</sub> |
| K | DQd              | DQd               | V <sub>SS</sub>   | K               | V <sub>SS</sub>   | DQa                 | DQa              |
| L | DQd              | DQd               | $\overline{SBWd}$ | $\overline{K}$  | $\overline{SBWa}$ | DQa                 | DQa              |
| M | V <sub>DDQ</sub> | DQd               | V <sub>SS</sub>   | $\overline{SW}$ | V <sub>SS</sub>   | DQa                 | V <sub>DDQ</sub> |
| N | DQd              | DQd               | V <sub>SS</sub>   | SA              | V <sub>SS</sub>   | DQa                 | DQa              |
| P | DQd              | DQd               | V <sub>SS</sub>   | SA              | V <sub>SS</sub>   | DQa                 | DQa              |
| R | NC               | SA                | M1 <sup>(4)</sup> | V <sub>DD</sub> | M2 <sup>(5)</sup> | SA                  | NC               |
| T | NC               | NC <sup>(1)</sup> | SA                | SA              | SA                | NC <sup>(1)</sup>   | ZZ               |
| U | V <sub>DDQ</sub> | TMS               | TDI               | TCK             | TDO               | RSVD <sup>(3)</sup> | V <sub>DDQ</sub> |

## Notes:

1. Pad Locations 2T and 6T are true no-connects. However, they are defined as SA address inputs in x18 LW SRAMs.
2. Pad Location 2B is a true no-connect. However, it is defined as an SA address input in 16Mb LW SRAMs.
3. Pad Location 6U must be left unconnected. It is used by Sony for internal test purposes.
4. Pad Location 3R is defined as an M1 mode pin in LW SRAMs. However, it must be tied "high" in this device.
5. Pad Location 5R is defined as an M2 mode pin in LW SRAMs. However, it must be tied "low" in this device.

## Pin Description

| Symbol   | Type   | Description  |
|--|--------|--|
| SA   | Input  | Synchronous Address Inputs - Registered on the rising edge of K.   |
| DQa, DQb<br>DQc, DQd   | I/O    | Synchronous Data Inputs / Outputs - Registered on the rising edge of K during write operations.<br>Driven from the falling edge of K during read operations.<br>DQa - indicates Data Byte a<br>DQb - indicates Data Byte b<br>DQc - indicates Data Byte c<br>DQd - indicates Data Byte d   |
| K, $\bar{K}$   | Input  | Differential Input Clocks  |
| $\bar{SS}$   | Input  | Synchronous Select Input - Registered on the rising edge of K.<br>$\bar{SS} = 0$ specifies a write operation when $\bar{SW} = 0$<br>specifies a read operation when $\bar{SW} = 1$<br>$\bar{SS} = 1$ specifies a deselect operation  |
| $\bar{SW}$   | Input  | Synchronous Global Write Enable Input - Registered on the rising edge of K.<br>$\bar{SW} = 0$ specifies a write operation when $\bar{SS} = 0$<br>$\bar{SW} = 1$ specifies a read operation when $\bar{SS} = 0$   |
| $\bar{SBWa}$ , $\bar{SBWb}$ ,<br>$\bar{SBWc}$ , $\bar{SBWd}$ | Input  | Synchronous Byte Write Enable Inputs - Registered on the rising edge of K.<br>$\bar{SBWa} = 0$ specifies write Data Byte a when $\bar{SS} = 0$ and $\bar{SW} = 0$<br>$\bar{SBWb} = 0$ specifies write Data Byte b when $\bar{SS} = 0$ and $\bar{SW} = 0$<br>$\bar{SBWc} = 0$ specifies write Data Byte c when $\bar{SS} = 0$ and $\bar{SW} = 0$<br>$\bar{SBWd} = 0$ specifies write Data Byte d when $\bar{SS} = 0$ and $\bar{SW} = 0$ |
| $\bar{G}$  | Input  | Asynchronous Output Enable Input - De-asserted (high) forces the data output drivers to Hi-Z.  |
| ZZ   | Input  | Asynchronous Sleep Mode Input - Asserted (high) forces the SRAM into low-power mode.   |
| M1, M2   | Input  | Read Operation Protocol Select - These mode pins must be tied "high" and "low" respectively to select Register - Latch read operations.  |
| ZQ   | Input  | Output Impedance Control Resistor Input  |
| V <sub>DD</sub>  |        | 3.3V Core Power Supply - Core supply voltage.  |
| V <sub>DDQ</sub>   |        | Output Power Supply - Output buffer supply voltage.  |
| V <sub>REF</sub>   |        | Input Reference Voltage - Input buffer threshold voltage.  |
| V <sub>SS</sub>  |        | Ground   |
| TCK  | Input  | JTAG Clock   |
| TMS  | Input  | JTAG Mode Select   |
| TDI  | Input  | JTAG Data In   |
| TDO  | Output | JTAG Data Out  |
| RSVD   |        | Reserved - This pin is used for Sony test purposes only. It must be left unconnected.  |
| NC   |        | No Connect - These pins are true no-connects, i.e. there is no internal chip connection to these pins. They can be left unconnected or tied directly to V <sub>DD</sub> , V <sub>DDQ</sub> , or V <sub>SS</sub> .  |

### •Clock Truth Table

| K   | ZZ | $\overline{SS}$<br>( $t_n$ ) | $\overline{SW}$<br>( $t_n$ ) | $\overline{SBWx}$<br>( $t_n$ ) | $\overline{G}$ | Operation                              | DQ<br>( $t_n$ ) | DQ<br>( $t_{n+1}$ ) |
|-----|----|------------------------------|------------------------------|--------------------------------|----------------|--|-----------------|---------------------|
| X   | H  | X                            | X                            | X                              | X              | Sleep (Power Down) Mode                | Hi - Z          | Hi - Z              |
| L→H | L  | H                            | X                            | X                              | X              | Deselect                               | Hi - Z          | X                   |
| L→H | L  | L                            | H                            | X                              | H              | Read                                   | Hi - Z          | Hi - Z              |
| L→H | L  | L                            | H                            | X                              | L              | Read                                   | Q( $t_n$ )      | X                   |
| L→H | L  | L                            | L                            | L                              | X              | Write All Bytes                        | Hi - Z          | D( $t_n$ )          |
| L→H | L  | L                            | L                            | X                              | X              | Write Bytes With $\overline{SBWx} = L$ | Hi - Z          | D( $t_n$ )          |
| L→H | L  | L                            | L                            | H                              | X              | Abort Write                            | Hi - Z          | X                   |

### •Sleep (Power Down) Mode

Sleep (power down) mode is provided through the asynchronous input signal ZZ. When ZZ is asserted (high), the output drivers will go to a Hi-Z state, and the SRAM will begin to draw standby current. Contents of the memory array will be preserved. An enable time ( $t_{ZZE}$ ) must be met before the SRAM is guaranteed to be in sleep mode, and a recovery time ( $t_{ZZR}$ ) must be met before the SRAM can resume normal operation.

### •Programmable Impedance Output Drivers

These devices have programmable impedance output drivers. The output impedance is controlled by an external resistor RQ connected between the SRAM's ZQ pin and  $V_{SS}$ , and is equal to one-fifth the value of this resistor, nominally. See the DC Electrical Characteristics section for further information.

#### Output Driver Impedance Power-Up Requirements

Output driver impedance will reach the programmed value within 8192 cycles after power-up. Consequently, it is recommended that Read operations not be initiated until after the initial 8192 cycles have elapsed.

#### Output Driver Impedance Updates

Output driver impedance is updated during Write and Deselect operations when the output driver is disabled.

### •Power-Up Sequence

For reliability purposes, Sony recommends that power supplies power up in the following sequence:  $V_{SS}$ ,  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$ , and Inputs.  $V_{DDQ}$  should never exceed  $V_{DD}$ . If this power supply sequence cannot be met, a large bypass diode may be required between  $V_{DD}$  and  $V_{DDQ}$ . Please contact Sony Memory Application Department for further information.

### •Absolute Maximum Ratings<sup>(1)</sup>

| Item  | Symbol    | Rating                             | Units |
|---|-----------|------------------------------------|-------|
| Supply Voltage                                | $V_{DD}$  | -0.5 to +3.8                       | V     |
| Output Supply Voltage                         | $V_{DDQ}$ | -0.5 to +2.3                       | V     |
| Input Voltage (Address, Control, Data, Clock) | $V_{IN}$  | -0.5 to $V_{DDQ} + 0.5$            | V     |
| Input Voltage (M1, M2)                        | $V_{MIN}$ | -0.5 to $V_{DD} + 0.5$ (3.8V max.) | V     |
| Input Voltage (TCK, TMS, TDI)                 | $V_{TIN}$ | -0.5 to +3.8V                      | V     |
| Operating Temperature                         | $T_A$     | 0 to 85                            | °C    |
| Junction Temperature                          | $T_J$     | 0 to 110                           | °C    |
| Storage Temperature                           | $T_{STG}$ | -55 to 150                         | °C    |

<sup>(1)</sup> Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### •BGA Package Thermal Characteristics

| Item                         | Symbol        | Rating | Units |
|------------------------------|---------------|--------|-------|
| Junction to Case Temperature | $\Theta_{JC}$ | 3.6    | °C/W  |

### •I/O Capacitance

( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

| Item               | Symbol  | Test conditions | Min            | Max | Units |    |
|--------------------|---------|-----------------|----------------|-----|-------|----|
| Input Capacitance  | Address | $C_{ADDR}$      | $V_{IN} = 0V$  | --- | 3.5   | pF |
|                    | Control | $C_{CTRL}$      | $V_{IN} = 0V$  | --- | 3.5   | pF |
|                    | Clock   | $C_{CLK}$       | $V_{IN} = 0V$  | --- | 3.5   | pF |
| Output Capacitance | Data    | $C_{DATA}$      | $V_{OUT} = 0V$ | --- | 4.5   | pF |

Note: These parameters are sampled and are not 100% tested.

## •DC Recommended Operating Conditions

 $(V_{SS} = 0V, T_A = 0 \text{ to } 85^\circ\text{C})$ 

| Item  | Symbol    | Min             | Typ  | Max             | Units | Notes |
|---|-----------|-----------------|------|-----------------|-------|-------|
| Supply Voltage                              | $V_{DD}$  | 3.13            | 3.3  | 3.47            | V     |       |
| Output Supply Voltage                       | $V_{DDQ}$ | 1.8             | 1.9  | 2.0             | V     |       |
| Input Reference Voltage                     | $V_{REF}$ | 0.7             | 0.85 | 1.0             | V     | 1     |
| Input High Voltage (Address, Control, Data) | $V_{IH}$  | $V_{REF} + 0.1$ | ---  | $V_{DDQ} + 0.3$ | V     | 2     |
| Input Low Voltage (Address, Control, Data)  | $V_{IL}$  | -0.3            | ---  | $V_{REF} - 0.1$ | V     | 3     |
| Input High Voltage (M1, M2)                 | $V_{MIH}$ | 1.3             | ---  | $V_{DD} + 0.3$  | V     |       |
| Input Low Voltage (M1, M2)                  | $V_{MIL}$ | -0.3            | ---  | 0.4             | V     |       |
| Clock Input Signal Voltage                  | $V_{KIN}$ | -0.3            | ---  | $V_{DDQ} + 0.3$ | V     |       |
| Clock Input Differential Voltage            | $V_{DIF}$ | 0.2             | ---  | $V_{DDQ} + 0.6$ | V     |       |
| Clock Input Common Mode Voltage             | $V_{CM}$  | 0.7             | ---  | 1.3             | V     |       |

1. The peak-to-peak AC component superimposed on  $V_{REF}$  may not exceed 5% of the DC component.
2.  $V_{IH}$  (max) AC =  $V_{DDQ} + 1.0V$  for pulse widths less than one-quarter of the cycle time ( $t_{CYC}/4$ ).
3.  $V_{IL}$  (min) AC =  $-1.0V$  for pulse widths less than one-quarter of the cycle time ( $t_{CYC}/4$ ).

## •DC Electrical Characteristics

 $(V_{DD} = 3.3V \pm 5\%, V_{SS} = 0V, T_A = 0 \text{ to } 85^\circ\text{C})$ 

| Item  | Symbol    | Test Conditions  | Min                | Typ    | Max                | Units    | Notes |
|---|-----------|--|--------------------|--------|--------------------|----------|-------|
| Input Leakage Current (Address, Control, Clock) | $I_{LI}$  | $V_{IN} = V_{SS} \text{ to } V_{DDQ}$                              | -5                 | ---    | 5                  | uA       |       |
| Input Leakage Current (M1, M2)                  | $I_{MLI}$ | $V_{MIN} = V_{SS} \text{ to } V_{DD}$                              | -10                | ---    | 10                 | uA       |       |
| Input Leakage Current (Data)                    | $I_{DLI}$ | $V_{DIN} = V_{SS} \text{ to } V_{DDQ}$<br>$\overline{G} = V_{IH}$  | -10                | ---    | 10                 | uA       |       |
| Average Power Supply Operating Current          | $I_{DD}$  | $I_{OUT} = 0 \text{ mA}$<br>$\overline{SS} = V_{IL}, ZZ = V_{IL}$  | ---                | ---    | 600                | mA       | 1     |
| Power Supply Standby Current                    | $I_{SB}$  | $I_{OUT} = 0 \text{ mA}$<br>$ZZ = V_{IH}$                          | ---                | ---    | 100                | mA       |       |
| Output High Voltage                             | $V_{OH}$  | $I_{OH} = -6.0 \text{ mA}$<br>$RQ = 250\Omega$                     | $V_{DDQ}-0.4$      | ---    | ---                | V        |       |
| Output Low Voltage                              | $V_{OL}$  | $I_{OL} = 6.0 \text{ mA}$<br>$RQ = 250\Omega$                      | ---                | ---    | 0.4                | V        |       |
| Output Driver Impedance                         | $R_{OUT}$ | $V_{OH}, V_{OL} = V_{DDQ}/2$<br>$RQ < 125\Omega$                   | ---                | ---    | 28<br>(25*1.12)    | $\Omega$ | 2     |
|   |           | $V_{OH}, V_{OL} = V_{DDQ}/2$<br>$125\Omega \leq RQ \leq 300\Omega$ | $(RQ/5)^*$<br>0.82 | $RQ/5$ | $(RQ/5)^*$<br>1.12 | $\Omega$ |       |
|   |           | $V_{OH}, V_{OL} = V_{DDQ}/2$<br>$RQ > 300\Omega$                   | 49<br>(60*0.82)    | ---    | ---                | $\Omega$ | 3     |

1. This parameter applies to all speed bins (-4, -42, -43, and -44).
2. For maximum output drive (i.e. minimum impedance), the ZQ pin can be tied directly to  $V_{SS}$ .
3. For minimum output drive (i.e. maximum impedance), the ZQ pin can be left unconnected or tied to  $V_{DDQ}$ .

## •AC Electrical Characteristics

| Parameter  | Symbol      | -4  |                   | -42 |                   | -43 |                   | -44 |     | Units | Notes |
|--|-------------|-----|-------------------|-----|-------------------|-----|-------------------|-----|-----|-------|-------|
|  |             | Min | Max               | Min | Max               | Min | Max               | Min | Max |       |       |
| K Cycle Time   | $t_{KHKH}$  | 4.0 | ---               | 4.2 | ---               | 4.3 | ---               | 4.4 | --- | ns    |       |
| K Clock High Pulse Width                                       | $t_{KHKL}$  | 1.5 | ---               | 1.5 | ---               | 1.5 | ---               | 1.5 | --- | ns    |       |
| K Clock Low Pulse Width  | $t_{KLKH}$  | 1.5 | ---               | 1.5 | ---               | 1.5 | ---               | 1.5 | --- | ns    |       |
| Address Setup Time   | $t_{AVKH}$  | 0.3 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 1     |
| Address Hold Time  | $t_{KHAX}$  | 0.5 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 2     |
| Write Enables Setup Time                                       | $t_{WVKH}$  | 0.3 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 1     |
| Write Enables Hold Time  | $t_{KHWX}$  | 0.5 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 2     |
| Synchronous Select Setup Time                                  | $t_{SVKH}$  | 0.3 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 1     |
| Synchronous Select Hold Time                                   | $t_{KHSX}$  | 0.5 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 2     |
| Data Input Setup Time  | $t_{DVKH}$  | 0.3 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 1     |
| Data Input Hold Time   | $t_{KHDX}$  | 0.5 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 2     |
| K Clock High to Output Valid<br>("A" Sub-Bin)<br>("B" Sub-Bin) | $t_{KHQV}$  | --- | 3.9<br>3.8<br>3.7 | --- | 4.2<br>4.1<br>4.0 | --- | 4.5<br>4.4<br>4.3 | --- | 4.7 | ns    |       |
| K Clock Low to Output Valid                                    | $t_{KLQV}$  | --- | 1.8               | --- | 2.0               | --- | 2.1               | --- | 2.2 | ns    |       |
| K Clock Low to Output Hold                                     | $t_{KLQX}$  | 0.5 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 3     |
| K Clock Low to Output Low-Z                                    | $t_{KLQX1}$ | 0.5 | ---               | 0.5 | ---               | 0.5 | ---               | 0.5 | --- | ns    | 3,4   |
| K Clock High to Output High-Z                                  | $t_{KHQZ}$  | 1.2 | 2.2               | 1.2 | 2.3               | 1.2 | 2.4               | 1.2 | 2.5 | ns    | 3,4   |
| Output Enable Low to Output Valid                              | $t_{GLQV}$  | --- | 2.2               | --- | 2.3               | --- | 2.4               | --- | 2.5 | ns    |       |
| Output Enable Low to Output Low-Z                              | $t_{GLQX}$  | 0.3 | ---               | 0.3 | ---               | 0.3 | ---               | 0.3 | --- | ns    | 3,4   |
| Output Enable High to Output High-Z                            | $t_{GHQZ}$  | --- | 2.2               | --- | 2.3               | --- | 2.4               | --- | 2.5 | ns    | 3,4   |
| Sleep Mode Enable Time   | $t_{ZZE}$   | --- | 15                | --- | 15                | --- | 15                | --- | 15  | ns    | 3     |
| Sleep Mode Recovery Time                                       | $t_{ZZR}$   | 20  | ---               | 20  | ---               | 20  | ---               | 20  | --- | ns    | 3     |

All parameters are specified over the range  $T_A = 0$  to  $85^\circ\text{C}$ .

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal, unless otherwise noted.

1. These parameters are measured from  $V_{REF} \pm 200\text{mV}$  to the clock mid-point ("4" bin only).
2. These parameters are measured from  $V_{REF} \pm 200\text{mV}$  to the clock mid-point.
3. These parameters are sampled and are not 100% tested.
4. These parameters are measured at  $\pm 50\text{mV}$  from steady state voltage.

**•AC Electrical Characteristics (Guaranteed By Design)**

| Parameter                     | Symbol     | -4               |     | Units | Notes |
|-------------------------------|------------|------------------|-----|-------|-------|
|                               |            | Min              | Max |       |       |
| K Clock High to Output High-Z | $t_{KHQZ}$ | $t_{KHQV} - 2.4$ | 2.0 | ns    | 1,2,3 |

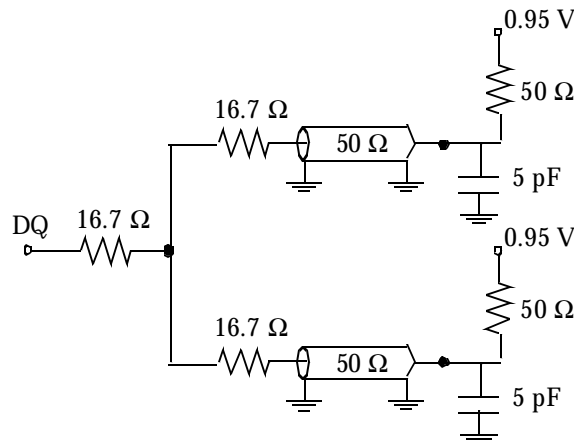
1. This parameter is applicable when  $t_{KHQV} \leq 3.8\text{ns}$ .
2. This parameter is measured at the gate of the output driver of the SRAM.
3. Please refer to the previous page (p. 8) of this document for information concerning to what specification this parameter is tested.

•AC Test Conditions

( $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDQ} = 1.9V \pm 0.1V$ ,  $T_A = 0$  to  $85^\circ C$ )

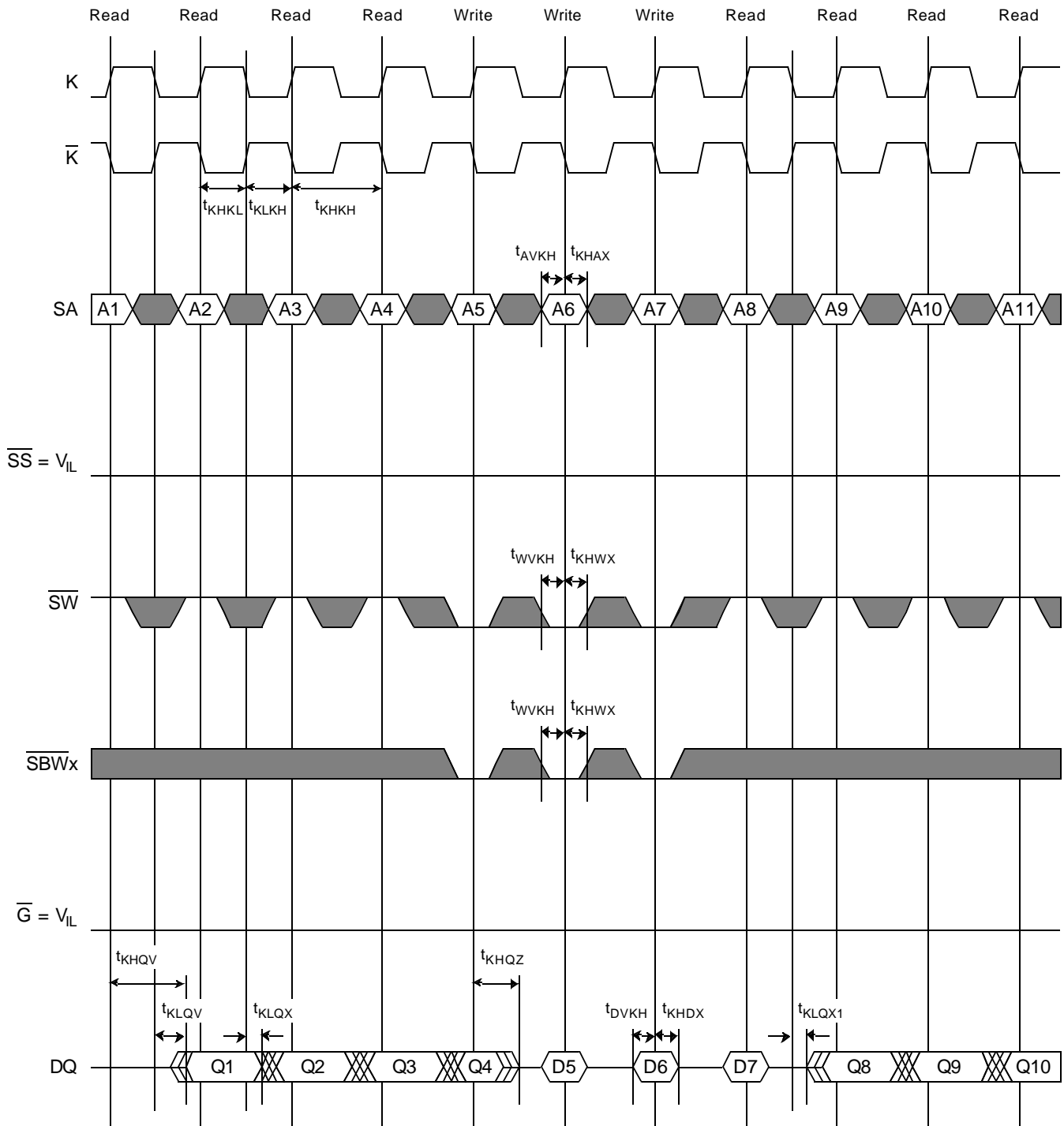
| Item                               | Symbol     | Conditions         | Units | Notes                      |
|------------------------------------|------------|--------------------|-------|----------------------------|
| Input Reference Voltage            | $V_{REF}$  | 0.85               | V     |                            |
| Address / Control Input High Level | $V_{CAIH}$ | 1.45               | V     |                            |
| Address / Control Input Low Level  | $V_{CAIL}$ | 0.35               | V     |                            |
| Data Input High Level              | $V_{DIH}$  | 1.25               | V     |                            |
| Data Input Low Level               | $V_{DIL}$  | 0.55               | V     |                            |
| Input Rise & Fall Time             |            | 2.0                | V/ns  |                            |
| Input Reference Level              |            | 0.85               | V     |                            |
| Clock Input High Voltage           | $V_{KIH}$  | 1.45               | V     | $V_{DIF} = 0.7V$           |
| Clock Input Low Voltage            | $V_{KIL}$  | 0.75               | V     | $V_{DIF} = 0.7V$           |
| Clock Input Common Mode Voltage    | $V_{CM}$   | 1.10               | V     |                            |
| Clock Input Rise & Fall Time       |            | 2.0                | V/ns  |                            |
| Clock Input Reference Level        |            | K/ $\bar{K}$ cross | V     |                            |
| Output Reference Level             |            | 0.95               | V     |                            |
| Output Load Conditions             |            |                    |       | Fig.1<br>$R_Q = 250\Omega$ |

Figure 1: AC Test Output Load



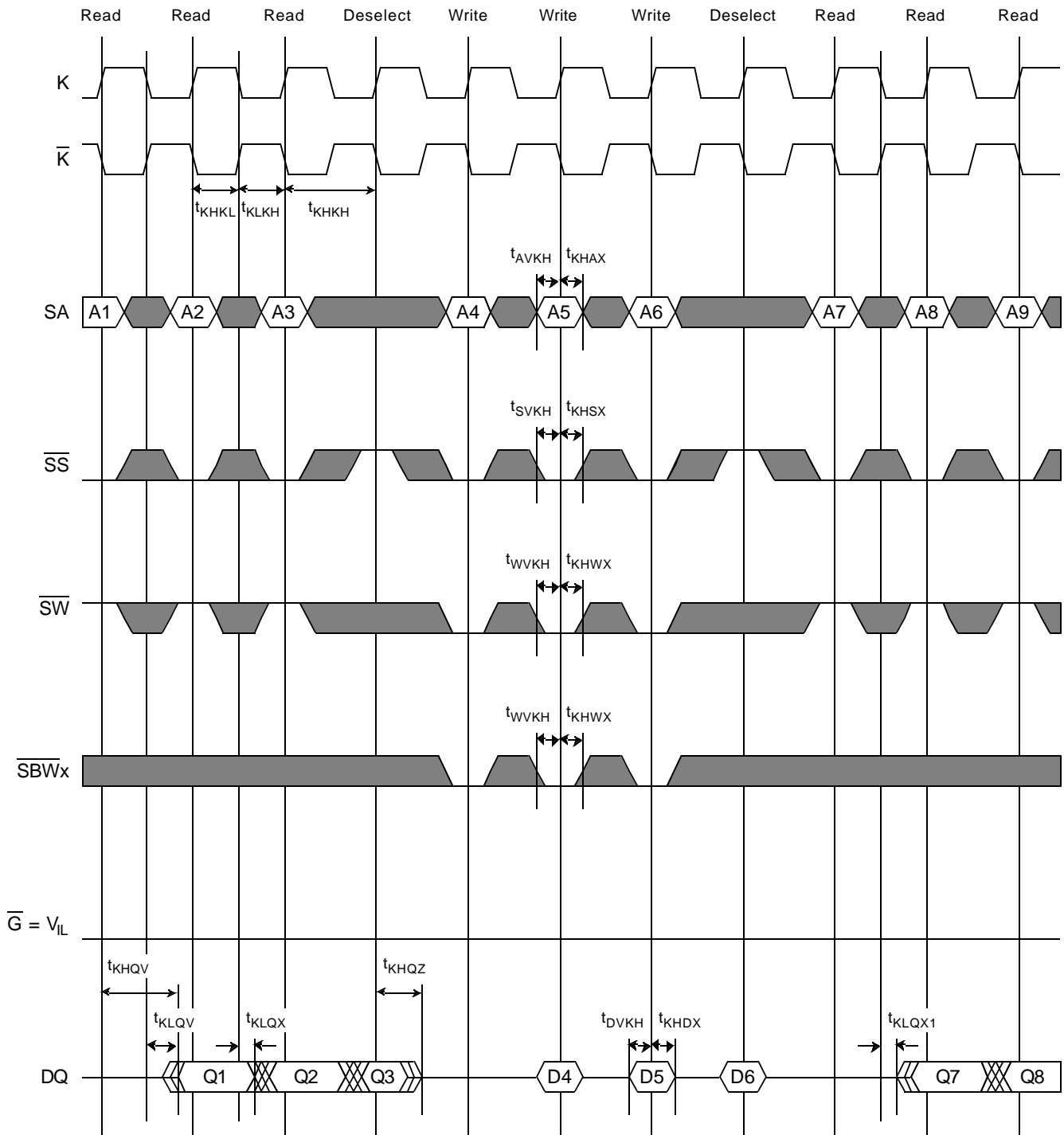
**Timing Diagram of Read-Write-Read Operations  
Synchronously Controlled via SW (G = Low and SS = Low)**

Figure 2



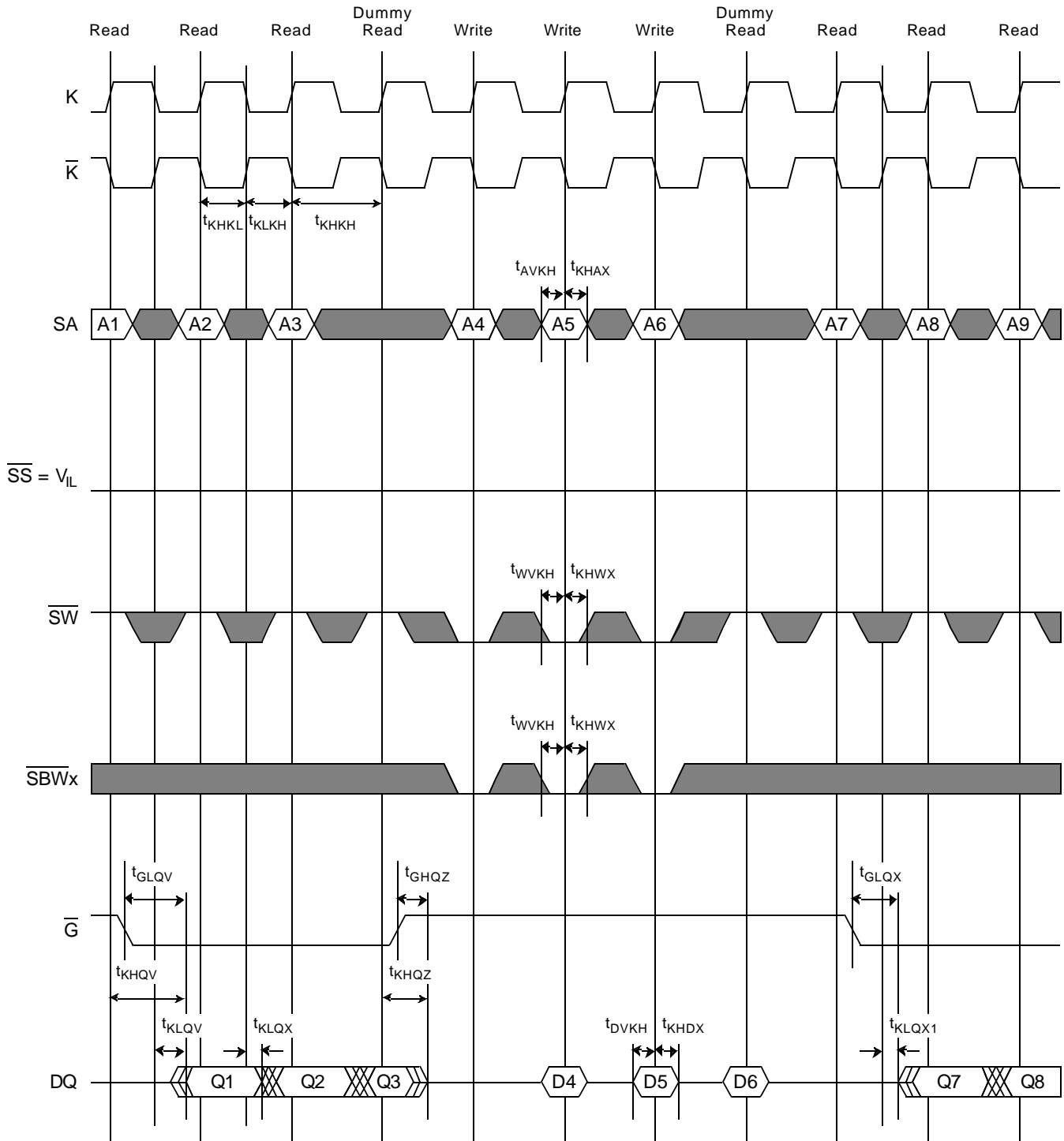
**Timing Diagram of Read-Write-Read Operations**  
**Synchronously Controlled via SS and Deselect Operations ( $\bar{G} = \text{Low}$ )**

Figure 3



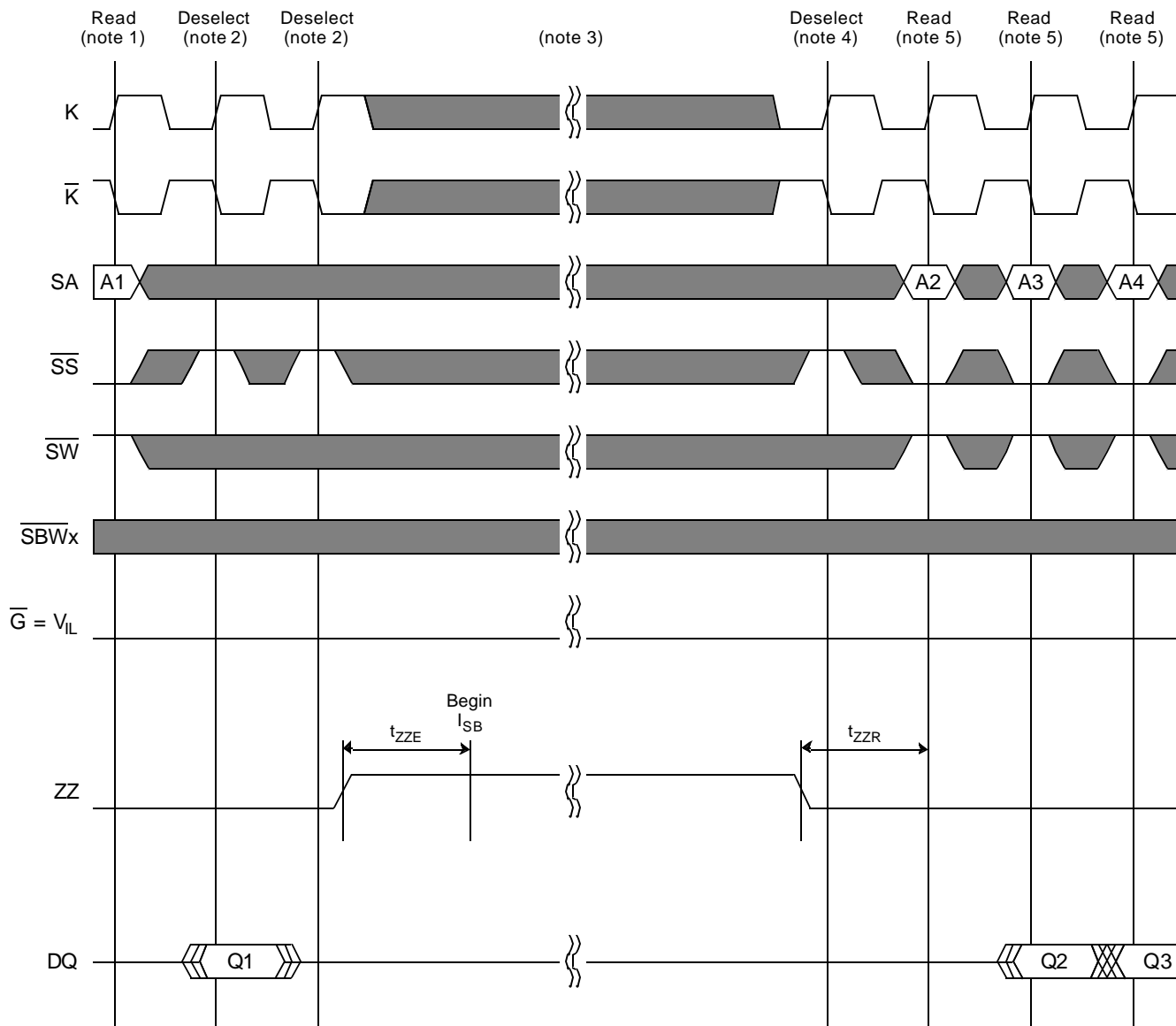
**Timing Diagram of Read-Write-Read Operations  
Asynchronously Controlled via G and Dummy Read Operations ( $\overline{SS} = V_L$ )**

Figure 4



**Timing Diagram of Sleep (Power-Down) Mode Operation  
Asynchronously Controlled via ZZ**

Figure 5



Note 1: This can be ANY valid operation. The depiction of a Read operation here is provided only as an example.

Note 2: Before ZZ is asserted, at least two (2) Deselect operations must be initiated after the last Read or Write operation is initiated, in order to ensure the successful completion of the last Read or Write operation.

Note 3: While ZZ is asserted, all of the SRAM's address, control, data, and clock inputs are ignored.

Note 4: After ZZ is deasserted, Deselect operations must be initiated until the specified recovery time ( $t_{ZZR}$ ) has been met. Read and Write operations may NOT be initiated during this time.

Note 5: This can be ANY valid operation. The depiction of a Read operation here is provided only as an example.

### •Test Mode Description

This device provides a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components, and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, this device contains a TAP Controller and four TAP Registers. The TAP Registers consist of one Instruction Register and three Data Registers (ID, Bypass, and Boundary Scan Registers).

The TAP consists of the following four signals:

|      |                  |  |
|------|------------------|--|
| TCK: | Test Clock       | Induces (clocks) TAP Controller state transitions.                                 |
| TMS: | Test Mode Select | Inputs commands to the TAP Controller. Sampled on the rising edge of TCK.          |
| TDI: | Test Data In     | Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK.      |
| TDO: | Test Data Out    | Outputs data serially from the TAP Registers. Driven from the falling edge of TCK. |

### Disabling the TAP

When JTAG is not used, TCK should be tied "low" to prevent clocking the SRAM. TMS and TDI should either be tied "high" through a pull-up resistor or left unconnected. TDO should be left unconnected.

Note: Operation of the TAP does not interfere with normal SRAM operation except when the SAMPLE-Z instruction is selected (see page 20 for further information). Consequently, TCK, TMS, and TDI can be controlled any number of ways without adversely affecting the functionality of the device.

### JTAG DC Recommended Operating Conditions

( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0$  to  $85^\circ C$ )

| Parameter                       | Symbol    | Test Conditions          | Min  | Max | Units   |
|---------------------------------|-----------|--------------------------|------|-----|---------|
| JTAG Input High Voltage         | $V_{TIH}$ | ---                      | 1.4  | 3.6 | V       |
| JTAG Input Low Voltage          | $V_{TIL}$ | ---                      | -0.3 | 0.8 | V       |
| JTAG Output High Voltage (CMOS) | $V_{TOH}$ | $I_{TOH} = -100\mu A$    | 2.6  | --- | V       |
| JTAG Output Low Voltage (CMOS)  | $V_{TOL}$ | $I_{TOL} = 100\mu A$     | ---  | 0.1 | V       |
| JTAG Output High Voltage (TTL)  | $V_{TOH}$ | $I_{TOH} = -2.0mA$       | 2.3  | --- | V       |
| JTAG Output Low Voltage (TTL)   | $V_{TOL}$ | $I_{TOL} = 2.0mA$        | ---  | 0.4 | V       |
| JTAG Input Leakage Current      | $I_{TLI}$ | $V_{TIN} = 0V$ to $3.6V$ | -10  | 10  | $\mu A$ |

### JTAG AC Test Conditions

( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = 0$  to  $85^\circ C$ )

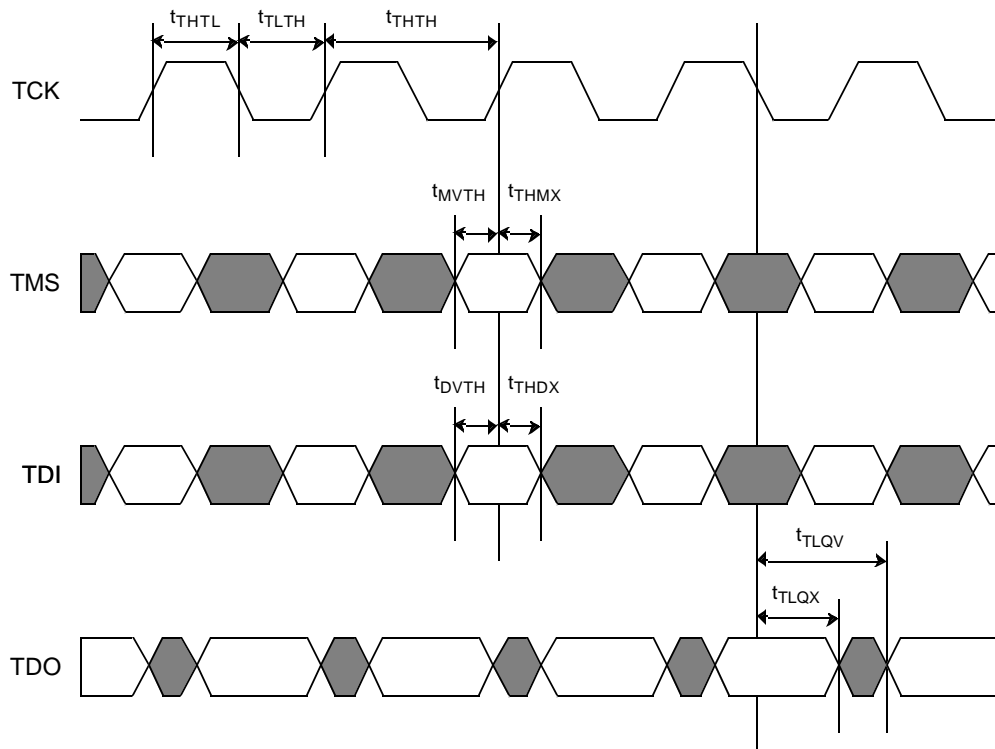
| Parameter                   | Symbol    | Conditions | Units | Notes               |
|-----------------------------|-----------|------------|-------|---------------------|
| JTAG Input High Level       | $V_{TIH}$ | 3.0        | V     |                     |
| JTAG Input Low Level        | $V_{TIL}$ | 0.0        | V     |                     |
| JTAG Input Rise & Fall Time |           | 1.0        | V/ns  |                     |
| JTAG Input Reference Level  |           | 1.5        | V     |                     |
| JTAG Output Reference Level |           | 1.5        | V     |                     |
| JTAG Output Load Condition  |           |            |       | See Fig.1 (page 10) |

**JTAG AC Electrical Characteristics**

| Parameter            | Symbol     | Min | Max | Unit |
|----------------------|------------|-----|-----|------|
| TCK Cycle Time       | $t_{THTH}$ | 100 |     | ns   |
| TCK High Pulse Width | $t_{THTL}$ | 40  |     | ns   |
| TCK Low Pulse Width  | $t_{TLTH}$ | 40  |     | ns   |
| TMS Setup Time       | $t_{MVTH}$ | 10  |     | ns   |
| TMS Hold Time        | $t_{THMX}$ | 10  |     | ns   |
| TDI Setup Time       | $t_{DVTH}$ | 10  |     | ns   |
| TDI Hold Time        | $t_{THDX}$ | 10  |     | ns   |
| TCK Low to TDO Valid | $t_{TLQV}$ |     | 20  | ns   |
| TCK Low to TDO Hold  | $t_{TLQX}$ | 0   |     | ns   |

**JTAG Timing Diagram**

Figure 6



## **TAP Registers**

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: “Instruction Registers”, of which there is one - the Instruction Register, and “Data Registers”, of which there are three - the ID Register, the Bypass Register, and the Boundary Scan Register. Individual TAP registers are “selected” (inserted between TDI and TDO) when the appropriate sequence of commands is given to the TAP Controller.

### **Instruction Register (3 bits)**

The Instruction Register stores the instructions that are executed by the TAP Controller when the TAP Controller is in the “Run-Test / Idle” state, or in any of the various “Data Register” states. It is loaded with the IDCODE instruction at power-up, or when the TAP Controller is in the “Test-Logic Reset” state or the “Capture-IR” state. It is inserted between TDI and TDO when the TAP Controller is in the “Shift-IR” state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed by the TAP Controller until the TAP Controller has reached the “Update-IR” state.

The Instruction Register is 3 bits wide, and is encoded as follows:

| Code (2:0) | Instruction | Description   |
|------------|-------------|---|
| 000        | BYPASS      | Inserts the Bypass Register between TDI and TDO.  |
| 001        | IDCODE      | Inserts the ID Register between TDI and TDO.  |
| 010        | SAMPLE-Z    | Captures the SRAM’s I/O ring contents in the Boundary Scan Register. Inserts the Boundary Scan Register between TDI and TDO. Disables the SRAM’s data output drivers. |
| 011        | BYPASS      | Inserts the Bypass Register between TDI and TDO.  |
| 100        | SAMPLE      | Captures the SRAM’s I/O ring contents in the Boundary Scan Register. Inserts the Boundary Scan Register between TDI and TDO.  |
| 101        | PRIVATE     | Do not use. Reserved for manufacturer use only.   |
| 110        | BYPASS      | Inserts the Bypass Register between TDI and TDO.  |
| 111        | BYPASS      | Inserts the Bypass Register between TDI and TDO.  |

Bit 0 is the LSB of the Instruction Register, and Bit 2 is the MSB. When the Instruction Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

### **ID Register (32 bits)**

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

The ID Register is 32 bits wide, and is encoded as follows:

| Revision Number (31:28) | Part Number (27:12) | Sony ID (11:1) | Start Bit (0) |
|-------------------------|---------------------|----------------|---------------|
| xxxx                    | 0000 0000 0100 1000 | 0000 1110 001  | 1             |

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

**Bypass Register (1 bit)**

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic “0” when the BYPASS instruction has been loaded in the the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

**Boundary Scan Register (70 bits)**

The Boundary Scan Register is equal in length to the number of active signal connections to the SRAM (excluding the TAP pins) plus a number of place holder locations reserved for density and/or functional upgrades. The Boundary Scan Register is loaded with the contents of the SRAM’s I/O ring when the SAMPLE or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the “Capture-DR” state. It is inserted between TDI and TDO when the SAMPLE or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the “Shift-DR” state.

The Boundary Scan Register contains the following bits:

|  |    |
|--|----|
| DQ   | 36 |
| SA   | 18 |
| K, $\overline{K}$                                      | 2  |
| $\overline{SS}$ , $\overline{SW}$ , $\overline{SBW}_x$ | 6  |
| $\overline{G}$ , ZZ                                    | 2  |
| M1, M2   | 2  |
| ZQ   | 1  |
| Place Holder   | 3  |

For deterministic results, all signals composing the SRAM’s I/O ring must meet setup and hold times with respect to TCK (same as TDI and TMS) when sampled.

$K/\overline{K}$  are connected to a differential input receiver that generates a single-ended input clock signal to the device. Therefore, in order to capture specific values for these signals in the Boundary Scan Register, these signals must be at opposite logic levels when sampled.

Place Holders are required for some NC pins to allow for future density and/or functional upgrades. They are connected to  $V_{SS}$  internally, regardless of pin connection externally.

The Boundary Scan Order Assignment table that follows depicts the order in which the bits from the table above are arranged in the Boundary Scan Register. In the notation, Bit 1 is the LSB bit of the register. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

**Boundary Scan Order Assignments  
(By Exit Sequence)**

| Bit | Signal      | Pad | Bit | Signal            | Pad |
|-----|-------------|-----|-----|-------------------|-----|
| 1   | M2          | 5R  | 36  | SA                | 3B  |
| 2   | SA          | 4P  | 37  | NC <sup>(1)</sup> | 2B  |
| 3   | SA          | 4T  | 38  | SA                | 3A  |
| 4   | SA          | 6R  | 39  | SA                | 3C  |
| 5   | SA          | 5T  | 40  | SA                | 2C  |
| 6   | ZZ          | 7T  | 41  | SA                | 2A  |
| 7   | DQa         | 6P  | 42  | DQc               | 2D  |
| 8   | DQa         | 7P  | 43  | DQc               | 1D  |
| 9   | DQa         | 6N  | 44  | DQc               | 2E  |
| 10  | DQa         | 7N  | 45  | DQc               | 1E  |
| 11  | DQa         | 6M  | 46  | DQc               | 2F  |
| 12  | DQa         | 6L  | 47  | DQc               | 2G  |
| 13  | DQa         | 7L  | 48  | DQc               | 1G  |
| 14  | DQa         | 6K  | 49  | DQc               | 2H  |
| 15  | DQa         | 7K  | 50  | DQc               | 1H  |
| 16  | <u>SBWa</u> | 5L  | 51  | <u>SBWc</u>       | 3G  |
| 17  | <u>K</u>    | 4L  | 52  | <u>ZQ</u>         | 4D  |
| 18  | <u>K</u>    | 4K  | 53  | <u>SS</u>         | 4E  |
| 19  | <u>G</u>    | 4F  | 54  | NC <sup>(1)</sup> | 4G  |
| 20  | <u>SBWb</u> | 5G  | 55  | NC <sup>(1)</sup> | 4H  |
| 21  | DQb         | 7H  | 56  | <u>SW</u>         | 4M  |
| 22  | DQb         | 6H  | 57  | <u>SBWd</u>       | 3L  |
| 22  | DQb         | 7G  | 58  | DQd               | 1K  |
| 24  | DQb         | 6G  | 59  | DQd               | 2K  |
| 25  | DQb         | 6F  | 60  | DQd               | 1L  |
| 26  | DQb         | 7E  | 61  | DQd               | 2L  |
| 27  | DQb         | 6E  | 62  | DQd               | 2M  |
| 28  | DQb         | 7D  | 63  | DQd               | 1N  |
| 29  | DQb         | 6D  | 64  | DQd               | 2N  |
| 30  | SA          | 6A  | 65  | DQd               | 1P  |
| 31  | SA          | 6C  | 66  | DQd               | 2P  |
| 32  | SA          | 5C  | 67  | SA                | 3T  |
| 33  | SA          | 5A  | 68  | SA                | 2R  |
| 34  | SA          | 6B  | 69  | SA                | 4N  |
| 35  | SA          | 5B  | 70  | M1                | 3R  |

Note 1: NC pins at pad locations 2B, 4G, and 4H are connected to V<sub>SS</sub> internally, regardless of pin connection externally.

## **TAP Instructions**

### **IDCODE**

IDCODE is the default instruction loaded into the Instruction Register at power-up, and when the TAP Controller is in the “Test-Logic Reset” state.

When the IDCODE instruction is selected, a predetermined device- and manufacturer-specific identification code is loaded into the ID Register when the TAP Controller is in the “Capture-DR” state, and the ID Register is inserted between TDI and TDO when the TAP Controller is in the “Shift-DR” state.

Normal SRAM operation is not disrupted when the IDCODE instruction is selected.

### **BYPASS**

When the BYPASS instruction is selected, a logic “0” is loaded into the Bypass Register when the TAP Controller is in the “Capture-DR” state, and the Bypass Register is inserted between TDI and TDO when the TAP Controller is in the “Shift-DR” state.

Normal SRAM operation is not disrupted when the BYPASS instruction is selected.

### **SAMPLE**

When the SAMPLE instruction is selected, the individual logic states of all signals composing the SRAM’s I/O ring (see the Boundary Scan Register description for the complete list of signals) are loaded into the Boundary Scan Register when the TAP Controller is in the “Capture-DR” state, and the Boundary Scan Register is inserted between TDI and TDO when the TAP Controller is in the “Shift-DR” state.

Normal SRAM operation is not disrupted when the SAMPLE instruction is selected.

### **SAMPLE-Z**

When the SAMPLE-Z instruction is selected, the individual logic states of all signals composing the SRAM’s I/O ring (see the Boundary Scan Register description for the complete list of signals) are loaded into the Boundary Scan Register when the TAP Controller is in the “Capture-DR” state, and the Boundary Scan Register is inserted between TDI and TDO when the TAP Controller is in the “Shift-DR” state.

Additionally, when the SAMPLE-Z instruction is selected, the SRAM’s data output drivers are *disabled* (that is, the DQ I/O buffers are forced to an input state).

Consequently, normal SRAM operation is disrupted when the SAMPLE-Z instruction is selected. Read operations initiated while the SAMPLE-Z instruction is selected will fail.

**TAP Controller**

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction. State transitions are controlled by TMS and occur on the rising edge of TCK.

The TAP Controller enters the “Test-Logic Reset” state in one of two ways:

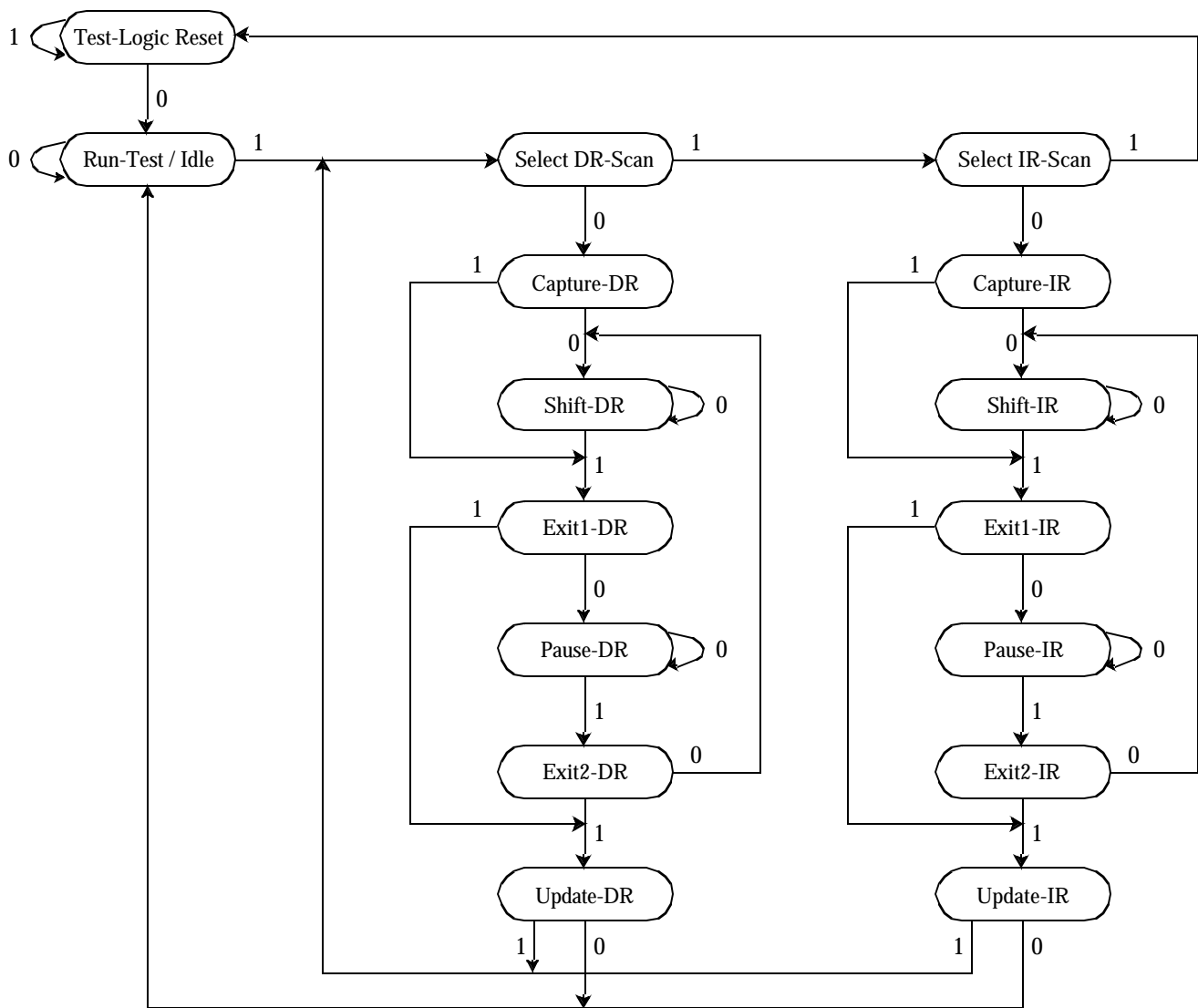
1. At power up.
2. When a logic “1” is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the “Shift-IR” state or the “Shift-DR” state.

The TDO output driver is active only when the TAP Controller is in either the “Shift-IR” state or the “Shift-DR” state.

**TAP Controller State Diagram**

Figure 7



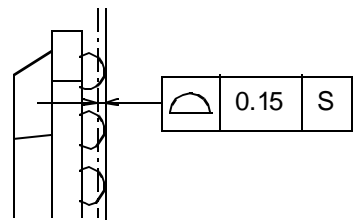
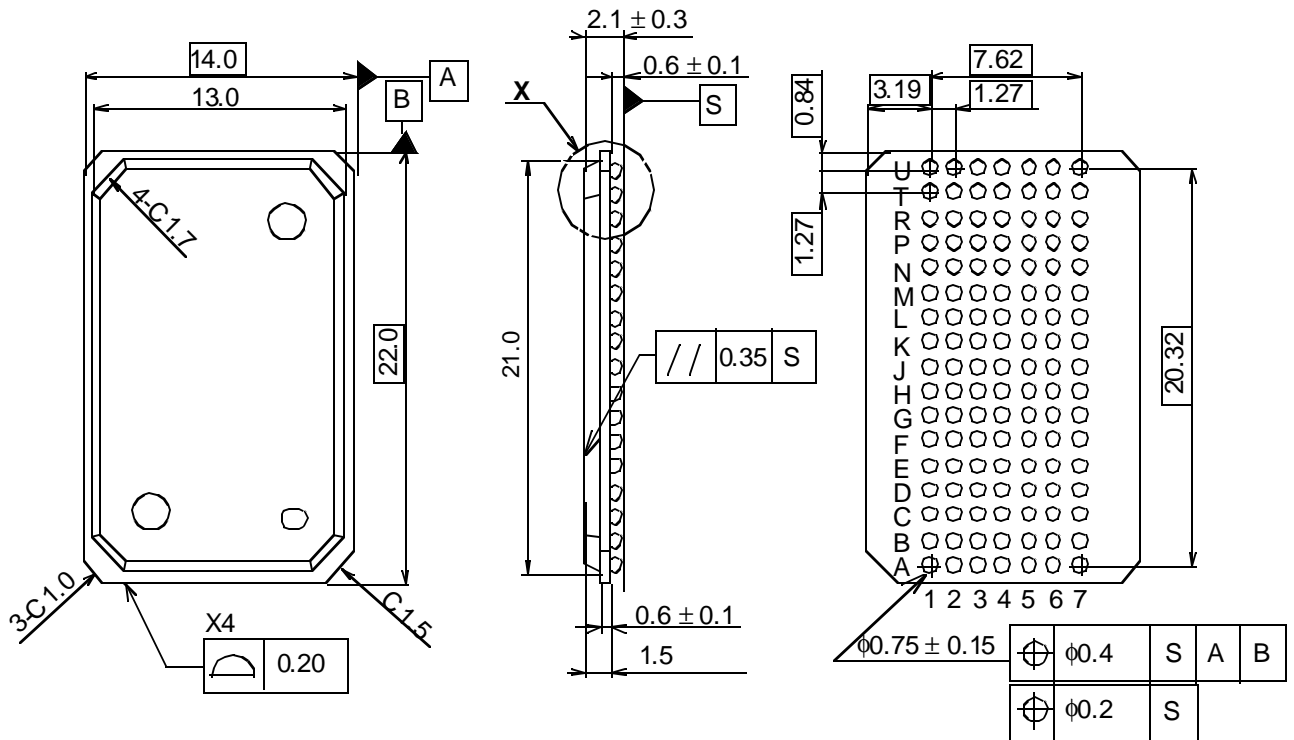
### •Ordering Information

| Part Number  | V <sub>DD</sub> | I/O Type | Size      | Speed<br>(Cycle / Access Time)                  |
|--|-----------------|----------|-----------|---|
| CXK77P36L80GB-4<br>CXK77P36L80GB-4A<br>CXK77P36L80GB-4B    | 3.3V            | HSTL     | 256K x 36 | 4.0ns / 3.9ns<br>4.0ns / 3.8ns<br>4.0ns / 3.7ns |
| CXK77P36L80GB-42<br>CXK77P36L80GB-42A<br>CXK77P36L80GB-42B | 3.3V            | HSTL     | 256K x 36 | 4.2ns / 4.2ns<br>4.2ns / 4.1ns<br>4.2ns / 4.0ns |
| CXK77P36L80GB-43<br>CXK77P36L80GB-43A<br>CXK77P36L80GB-43B | 3.3V            | HTSL     | 256K x 36 | 4.3ns / 4.5ns<br>4.3ns / 4.4ns<br>4.3ns / 4.3ns |
| CXK77P36L80GB-44   | 3.3V            | HSTL     | 256K x 36 | 4.4ns / 4.7ns                                   |

Note: These devices may be manufactured at two different fab locations - Wafertech and TSMC. Please see the BGA Package Marking diagram on page 25 for information concerning how to distinguish between devices manufactured at the two facilities.

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(7x17) 119 Pin BGA Package Dimensions



DETAIL A

PRELIMINARY

PACKAGE STRUCTURE

|            |               |
|------------|---------------|
| SONY CODE  | BGA-119P-021  |
| EIAJ CODE  | BGA119-P-1422 |
| JEDEC CODE | —             |

|                  |                      |
|------------------|----------------------|
| PACKAGE MATERIAL | EPOXY RESIN          |
| BORAD TREATMENT  | COPPER-CLAD LAMINATE |
| LEAD MATERIAL    | SOLDER               |
| PACKAGE MASS     | 1.1g                 |

(7x17) 119 Pin BGA Package Marking



**Description**

- 1) C Field: Part Number Code (up to 17 characters).
- 2) B Field: Lot Code (up to 7 characters).
- 3) F Field: Wafer Fab Plant Code (1 character).  
 e.g. F = "W" indicates Wafertech Fab.  
 e.g. F = "" (blank) indicates TSMC Fab (no character is used for TSMC).
- 4) F' Field: Revised Control Code (1 character).

**Example 1: Wafertech Fab**



**Example 2: TSMC Fab**



## •Revision History

| Rev. #  | Rev. date | Description of Modification   |
|---------|-----------|---|
| rev 0.0 | 01/07/00  | Initial Version   |
| rev 1.0 | 07/18/00  | <ol style="list-style-type: none"> <li>Added BGA Package Thermal Characteristics (p. 5).<br/>Junction to Case Temperature (<math>\Theta_{JC}</math>) 3.6 °C/W</li> <li>Modified DC Recommended Operating Conditions (p. 6).<br/> <math>V_{DDQ}</math> (min) 1.4V to 1.8V<br/> <math>V_{REF}</math>, <math>V_X</math> (max) 1.1V to 1.0V<br/> <math>V_{REF}</math>, <math>V_{CM}</math>, <math>V_X</math> (min) 0.6V to 0.7V</li> <li>Modified DC Electrical Characteristics (p. 7).<br/> <math>I_{LI}</math> (min/max) ±1uA to ±5uA<br/> <math>I_{DD}</math> (max) for -4 / -42 / -43 / -44 600mA / 580mA / 570mA / 560mA<br/> Added Note 3 regarding <math>R_{OUT}</math> that states "This parameter is guaranteed by design through extensive corner lot characterization".</li> <li>Modified AC Electrical Characteristics (p. 8).<br/> Added note 1 regarding Address, Write Enables, Synchronous Select, and Data Input Setup Times in the "-4" bin that states "these parameters are measured from <math>V_{REF} \pm 200mV</math> to the clock mid-point ("-4" bin only)".</li> <li>Removed 1.5V HSTL AC Test Condition.</li> <li>Added note to Disabling the TAP section that states that TAP operation does not interfere with normal SRAM operation except during the SAMPLE-Z instruction (p. 15).</li> <li>Modified JTAG DC Recommended Operating Conditions (p. 15).<br/> <math>V_{TOH}</math> (min) at <math>I_{TOH} = -100uA</math> 2.7V<br/> <math>V_{TOL}</math> (max) at <math>I_{TOL} = 100uA</math> 0.1V<br/> <math>V_{TOH}</math> (min) at <math>I_{TOH} = -2mA</math> 2.4V<br/> <math>V_{TOL}</math> (max) at <math>I_{TOL} = 2mA</math> 0.4V</li> <li>Updated JTAG AC Test Conditions (p. 15).</li> <li>Added BGA Package Dimensions (p. 23).</li> </ol> |
| rev 1.1 | 11/03/00  | <ol style="list-style-type: none"> <li>Modified DC Recommended Operating Conditions (p. 6).<br/> Removed Single-Ended clock support.<br/> Removed Clock Input Cross Point Voltage (<math>V_X</math>) specification.<br/> <math>V_{MIH}</math> (min) <math>V_{REF} + 0.3V</math> to 1.3V<br/> <math>V_{MIL}</math> (max) <math>V_{REF} - 0.3V</math> to 0.4V<br/> <math>V_{CM}</math> (max) 1.1V to 1.3V</li> <li>Modified DC Electrical Characteristics (p. 7).<br/> Combined <math>I_{DD}</math> specifications for each speed bin into one specification for all speed bins.<br/> Removed <math>I_{DD3}</math> specification.</li> <li>Modified AC Electrical Characteristics (p. 8).<br/> Added note 2 regarding Address, Write Enables, Synchronous Select, and Data Input Hold Times that states "these parameters are measured from <math>V_{REF} \pm 200mV</math> to the clock mid-point".</li> <li>Modified JTAG DC Recommended Operating Conditions (p. 15).<br/> <math>V_{TOH}</math> (min) at <math>I_{TOH} = -100uA</math> 2.7V to 2.6V<br/> <math>V_{TOH}</math> (min) at <math>I_{TOH} = -8mA</math> 2.4V to 2.3V</li> <li>Added BGA Package Marking (p. 24).</li> </ol>  |
| rev 1.2 | 10/02/02  | <ol style="list-style-type: none"> <li>Modified DC Electrical Characteristics (p. 7).<br/> <math>R_{OUT}</math> (min) RQ/5 - 10% to RQ/5 - 18%<br/> <math>R_{OUT}</math> (max) RQ/5 + 10% to RQ/5 + 12%</li> <li>Modified AC Electrical Characteristics (p. 8).<br/> Removed Output Enable Setup and Hold Time specifications.</li> </ol>   |