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ECL Products	

100181

4–Bit Binary/BCD ALU

FEATURES

- **Typical propagation delay: 2.10ns**
- **Typical supply current ($-I_{EE}$): 205mA**

DESCRIPTION

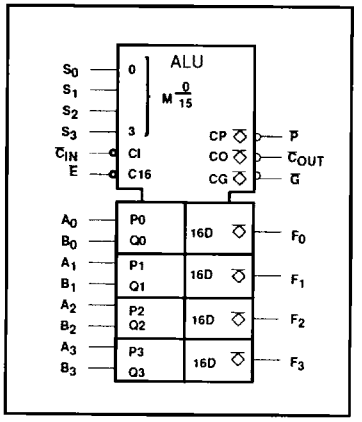
The 100181 is a 4–bit, binary/BCD arithmetic logic unit which performs eight arithmetic operations and eight logic operations on two four–bit words. Arithmetic and logic operations are selected by four select inputs (S_0–S_3). The circuit performs BCD as well as binary arithmetic. The A_n and B_n inputs accept the function arguments. The F_n outputs yield the function result. The circuit contains four output latches, which are transparent when the enable input (E) is low. The Carry Input ($\overline{C}_{IN}$), Carry Output ($\overline{C}_{OUT}$), Carry Lookahead Propagate ($\overline{P}$), and Carry Lookahead Generate ($\overline{G}$) lines allow for parallel operation with two or more devices.

Unused inputs must be tied to a low voltage, V_{IL} or V_{EE}.

PIN DESCRIPTION

PINS	DESCRIPTION
$A_0 - A_3$	Operand A Inputs
$B_0 - B_3$	Operand B Inputs
$\overline{C}_{IN}$	Carry Input (Active–Low)
$S_0 - S_3$	Function Select Inputs
$\overline{E}$	Latch Enable input (Active Low)
$\overline{G}$	Carry Lookahead Generate Output (Active–Low)
$\overline{P}$	Carry Lookahead Propagate Output (Active–Low)
$\overline{C}_{OUT}$	Carry Output (Active–Low)
$F_0 - F_3$	Function Outputs

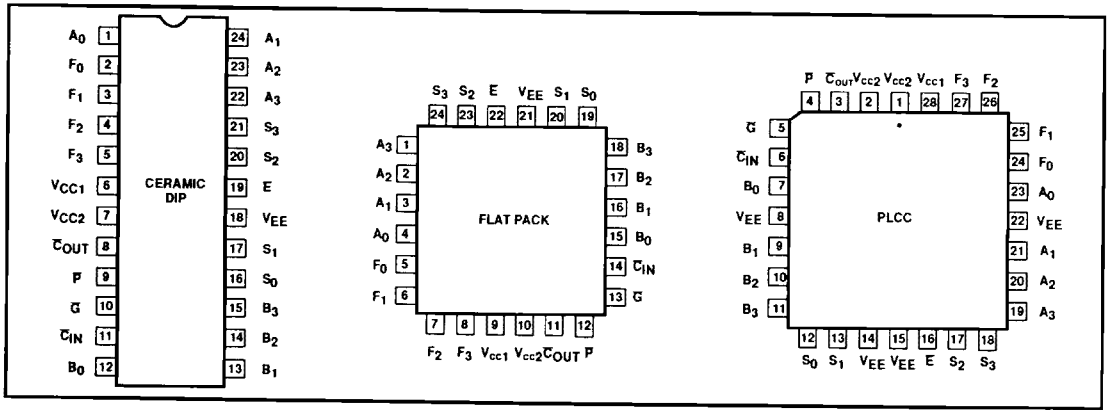
IEC/IEEE SYMBOL



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin Ceramic DIP (400 mils wide)	100181F
24–Pin Ceramic Flat Pack	100181Y
28–Pin PLCC	100181A

PIN CONFIGURATIONS



BINARY ARITHMETIC

When a binary addition operation is performed, F = A plus B plus C_{IN}, where A, B, and F are expressed in binary code.

For binary subtraction, F = A minus B plus C_{IN} = A plus B^1 plus C_{IN} where A and B are binary words and the superscript 1 designates one's complement. The circuit automatically takes the one's complement of word B by inverting bits B_0 through B_3. If the result is positive, then $\overline{C}_{OUT}$ will be low and the difference less one will be expressed in binary at F. If the result is negative or zero, $\overline{C}_{OUT}$ will be high and the difference will be expressed in one's complement at F. If a result in two's complement is desired, force $\overline{C}_{IN}$ low , since $F^2 = F^1 + 1$ (A superscript 2 denotes two's complement). The preceding description for binary subtraction holds true for the F = B minus A plus C_{IN} operation as well. Just switch the A and B variables.

BCD ARITHMETIC

When a BCD addition operation is performed, F = A plus B plus C_{IN}, where A, B, and F are expressed in BCD code.

The circuit automatically adds a +6 code correction to word B. Define a temporary variable F' = A plus B plus C_{IN} plus 6. If F' < 16, then a –6 code correction is performed: F = F' – 6 = A plus B plus C_{IN}. If F' ≥ 16, no further code correction is necessary, and F = F' = A plus B plus C_{IN} plus 6.

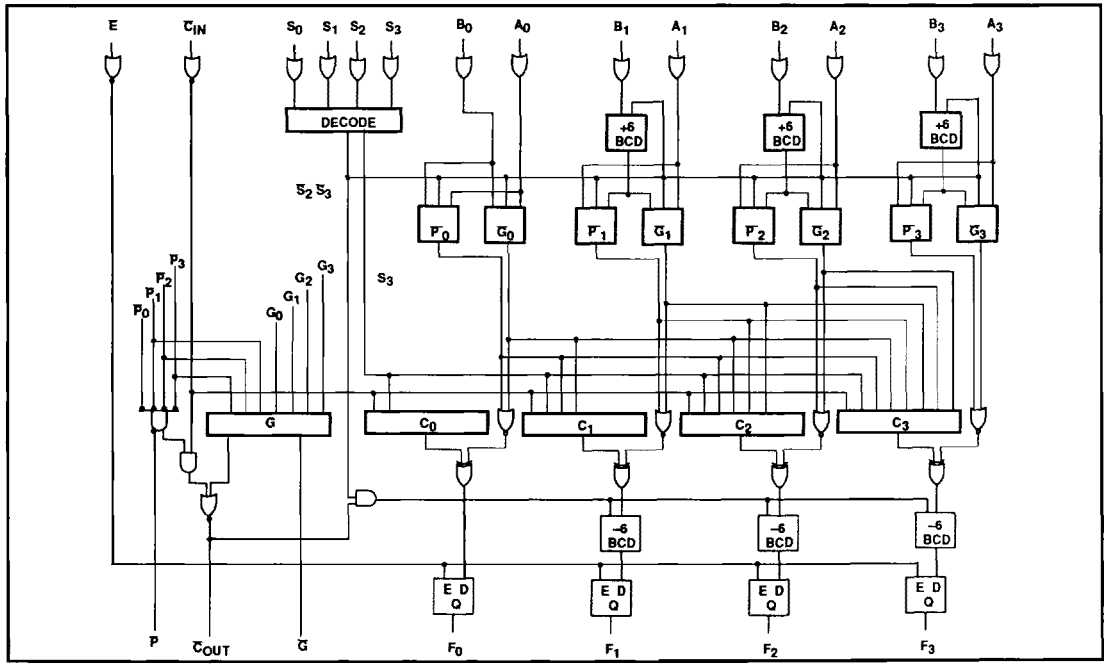
For BCD subtraction, F = A minus B plus $\overline{C}_{IN}$ = A plus B^9 plus C_{IN} where A and B are BCD words and the superscript 9 designates nine's complement. The circuit automatically takes the nine's complement of word B and then adds a +6 code correction. Define a temporary variable F' = A plus B^9 plus C_{IN} plus 6. If F' < 16, then a –6 code correction is performed: F = F' – 6 = A plus B^9 plus C_{IN}. if F' ≥ 16, no further code correction is necessary and F = F' = A plus B' plus C_{IN} plus 6. If the result is positive, then $\overline{C}_{OUT}$ will be low and the difference less one will be expressed in binary at F. If the result is negative or zero, $\overline{C}_{OUT}$ will be high and the difference will be expressed in nine's complement at F. If a result in 10's complement is desired, force $\overline{C}_{IN}$ low , since $F^{10} = F^9 + 1$ (A superscript 10 denotes 10's complement).

The preceding description for BCD subtraction holds true for the F = B minus A plus C_{IN} operation as well. Just switch the A and the B variables.

THE CARRY

Arithmetic on words larger than 4–bits can be performed by operating two or more 100181's together in parallel fashion. There are two possible arrangements: In the ripple–carry configuration, $\overline{C}_{OUT}$ of one stage is connected to $\overline{C}_{IN}$ of the next stage. The carry–lookahead configuration uses $\overline{P}$ and $\overline{G}$ in association with the 100179 (the Carry Lookahead Generator) or other external logic. With the addition of the 100179 chip, the carry–lookahead method offers faster adder throughput than the ripple–carry method. $\overline{P}$ goes low when a binary addition operation produces fifteen (nine for BCD), or when a minus operation produces zero. $\overline{G}$ goes low when the binary sum of A and B is greater than 15 (nine for BCD), or the difference of A and B is greater than zero.

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS				FUNCTION	OUTPUTS	
S_3	S_2	S_1	S_0		G_n	P_n
L	L	L	L	F = A plus B plus C_{IN} (BCD addition)	$A_n X_n$	$A_n + X_n$
L	L	L	H	F = A minus B plus C_{IN} (BCD subtraction)	$A_n Y_n$	$A_n + Y_n$
L	L	H	L	F = B minus A plus C_{IN} (BCD subtraction)	$A^9_n X_n$	$A^9_n + X_n$
L	L	H	H	F = 0 minus B plus C_{IN} (BCD subtraction)	0	Y_n
L	H	L	L	F = A plus B plus C_{IN} (Binary addition)	$A_n B_n$	$A_n + B_n$
L	H	L	H	F = A minus B plus C_{IN} (Binary subtraction)	$A_n \overline{B}_n$	$A_n + \overline{B}_n$
L	H	H	L	F = B minus A plus C_{IN} (Binary subtraction)	$\overline{A}_n B_n$	$\overline{A}_n + B_n$
L	H	H	H	F = 0 minus B plus C_{IN} (Binary subtraction)	0	$\overline{B}_n$
H	L	L	L	$F_n = A_n B_n + \overline{A}_n \overline{B}_n$ (Equivalence)	$A_n B_n$	$A_n + B_n$
H	L	L	H	$F_n = A_n \overline{B}_n + \overline{A}_n B_n$ (Exclusive OR)	$A_n \overline{B}_n$	$A_n + \overline{B}_n$
H	L	H	L	$F_n = A_n + B_n$ (OR)	A_n	$\overline{B}_n$
H	L	H	H	$F_n = A_n$	A_n	1
H	H	L	L	$F_n = \overline{B}_n$ (NOT)	0	B_n
H	H	L	H	$F_n = B_n$	0	$\overline{B}_n$
H	H	H	L	$F_n = A_n B_n$ (AND)	0	$\overline{A}_n + \overline{B}_n$
H	H	H	H	$F_n = 0$	0	1

NOTES:
H = High voltage level
L = Low voltage level
Overscore designates one's complement. Superscript "9" designates nine's complement.
All operations are described by $F_n = \overline{G_n + \overline{P}_n} \oplus C_n$ where n = 0 to 3, $\overline{P} = \overline{P}_0 + \overline{P}_1 + \overline{P}_2 + \overline{P}_3$ and $\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$
Internal equation for carry lookahead:
$C_0 = C_{IN} + S_3$
$C_1 = G_0 + P_0C_{IN} + S_3$
$C_2 = G_1 + P_1G_0 + P_1P_0C_{IN} + S_3$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_{IN} + S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_{IN} = C_{OUT}$

+6 correction for BCD operations (B + 6):
$X_0 = B_0$
$X_1 = \overline{B}_1$
$X_2 = B_1B_2 + \overline{B}_1\overline{B}_2$
$X_3 = \overline{B}_1\overline{B}_2B_3 + B_2\overline{B}_3 + B_1\overline{B}_3$

+6 correction for BCD operations (B^9 + 6)
$Y_0 = B_0^9$
$Y_1 = \overline{B_1^9}$
$Y_2 = B_1^9B_2^9 + \overline{B_1^9}\,\overline{B_2^9}$
$Y_3 = \overline{B_1^9}\,\overline{B_2^9}B_3^9 + B_2^9\overline{B_3^9} + B_1^9\overline{B_3^9}$

ABSOLUTE MAXIMUM RATINGS $V_{CC1} = V_{CC2}$ = ground, T_A = 0°C to +85°C unless otherwise specified.

SYMBOL	PARAMETER	LIMITS	UNIT
V_{EE}	Supply voltage range	–7.0 to +0.5	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})	V_{EE} to +0.5	V
I_O	Output source current (continuous)	–55	mA
T_S	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage		–4.8	–4.5	–4.2	V
V_{EE}	Supply voltage when operating with the 10K or the 10KH ECL family		–5.7			V
V_{IH}	High level input voltage	V_{EE} = –4.2V	–1150		–880	mV
		V_{EE} = –4.5V	–1165			
		V_{EE} = –4.8V	–1165			
V_{IL}	Low level input voltage	V_{EE} = –4.2V	–1810		–1475	mV
		V_{EE} = –4.5V			–1475	mV
		V_{EE} = –4.8V			–1490	mV
T_A	Operating ambient temperature range		0	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltages (–4.2V, –4.5V, –4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V, T_A = 0°C to +85°C unless otherwise specified[1,3,4]

SYMBOL	PARAMETER		TEST CONDITIONS[2]			LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		Outputs loaded with 50Ω to –2.0V ±0.010V	Inputs at V_{IHMAX} or V_{ILMIN}	V_{EE} = –4.2V	–1020		–870	mV
					V_{EE} = –4.5V	–1025	–955	–880	mV
					V_{EE} = –4.8V	–1035		–880	mV
V_{OHT}	High level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1030			mV
					V_{EE} = –4.5V	–1035			mV
					V_{EE} = –4.8V	–1045			mV
V_{OLT}	Low level output threshold voltage			Apply V_{IHMIN} or V_{ILMAX} to one input at a time. Other inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V			–1595	mV
					V_{EE} = –4.5V			–1610	mV
					V_{EE} = –4.8V			–1610	mV
V_{OL}	Low level output voltage			Inputs at V_{IHMAX} or V_{ILMIN}.	V_{EE} = –4.2V	–1810		–1605	mV
					V_{EE} = –4.5V	–1810	–1705	–1620	mV
					V_{EE} = –4.8V	–1830		–1620	mV
I_{IH}	High level input current	S_n, $\overline{E}$	One input under test at V_{IHMAX}. Other inputs at V_{ILMIN}.					300	µA
		others						190	µA
I_{IL}	Low level input current		One input under test at V_{ILMIN}. Other inputs at V_{IHMAX}.			0.5			µA
$-I_{EE}$	V_{EE} supply current		All inputs at V_{IHMAX}			130	205	300	mA

NOTES:

1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
4. The device can function down to V_{EE} = –5.7V, allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended V_{EE} range. For more information, see Chapters 5 and 10, Section 4.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –4.8V to –4.2V

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			T_A = 0°C		T_A = +25°C		T_A = +85°C		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	2.00 2.00	6.90 6.90	2.10 2.10	6.80 6.80	2.30 2.30	7.40 7.40	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$, $\overline{G}$		1.40 1.40	4.70 4.70	1.40 1.40	4.40 4.40	1.40 1.40	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{C}_{OUT}$		2.00 2.00	6.50 6.50	2.00 2.00	6.50 6.50	2.10 2.10	6.80 6.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		1.60 1.60	5.10 5.10	1.60 1.60	5.20 5.20	1.60 1.60	5.50 5.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.30 1.30	3.00 3.00	1.40 1.40	3.00 3.00	1.40 1.40	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n		1.40 1.40	8.80 8.80	1.50 1.50	8.60 8.60	1.50 1.50	9.00 9.00	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$, $\overline{G}$		1.70 1.70	7.40 7.40	2.00 2.00	5.90 5.90	2.00 2.00	6.50 6.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{C}_{OUT}$		2.70 2.70	10.1 10.1	2.80 2.80	8.50 8.50	2.90 2.90	8.70 8.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to F_n		1.00 1.00	3.40 3.40	0.90 0.90	3.60 3.60	1.10 1.10	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{C}_{OUT}$, $\overline{P}$, $\overline{G}$		0.45 0.45	2.70 2.70	0.45 0.45	2.60 2.60	0.45 0.45	2.70 2.70	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}$	Waveform 2	6.00		6.00		6.00		ns
t_h	Hold time, $\overline{E}$ to A_n, B_n		0.10		0.10		0.10		ns
t_s	Setup time, S_n to $\overline{E}$		7.00		7.00		7.00		ns
t_h	Hold time, $\overline{E}$ to S_n		0.60		0.60		0.60		ns
t_s	Setup time, $\overline{C}_{IN}$ to $\overline{E}$		4.00		4.00		4.00		ns
t_h	Hold time, $\overline{E}$ to $\overline{C}_{IN}$		0.60		0.60		0.60		ns
$t_{w(L)}$	Pulse width Low, $\overline{E}$	Waveform 1	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Ceramic DIP $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	2.00 2.00	6.90 6.90	2.10 2.10	6.80 6.80	2.30 2.30	7.40 7.40	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$, $\overline{G}$		1.40 1.40	4.70 4.70	1.40 1.40	4.40 4.40	1.40 1.40	4.70 4.70	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{C}_{OUT}$		2.00 2.00	6.50 6.50	2.00 2.00	6.50 6.50	2.10 2.10	6.80 6.80	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		1.60 1.60	5.10 5.10	1.60 1.60	5.20 5.20	1.60 1.60	5.50 5.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.30 1.30	3.00 3.00	1.40 1.40	3.00 3.00	1.40 1.40	3.10 3.10	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n		1.40 1.40	8.80 8.80	1.50 1.50	8.60 8.60	1.50 1.50	9.00 9.00	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$, $\overline{G}$		1.70 1.70	7.40 7.40	2.00 2.00	5.90 5.90	2.00 2.00	6.50 6.50	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{C}_{OUT}$		2.70 2.70	10.1 10.1	2.80 2.80	8.50 8.50	2.90 2.90	8.70 8.70	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to F_n		1.00 1.00	3.40 3.40	0.90 0.90	3.60 3.60	1.10 1.10	3.80 3.80	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{C}_{OUT}$, $\overline{P}$, $\overline{G}$		0.45 0.45	2.70 2.70	0.45 0.45	2.60 2.60	0.45 0.45	2.70 2.70	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}$	Waveform 2	6.00		6.00		6.00		ns
t_h	Hold time, $\overline{E}$ to A_n, B_n		0.10		0.10		0.10		ns
t_s	Setup time, S_n to $\overline{E}$		7.00		7.00		7.00		ns
t_h	Hold time, $\overline{E}$ to S_n		0.60		0.60		0.60		ns
t_s	Setup time, $\overline{C}_{IN}$ to $\overline{E}$		4.00		4.00		4.00		ns
t_h	Hold time, $\overline{E}$ to $\overline{C}_{IN}$		0.60		0.60		0.60		ns
$t_{w(L)}$	Pulse width Low, E	Waveform 1	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -4.8V$ to $-4.2V$

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	2.00 2.00	6.70 6.70	2.10 2.10	6.60 6.60	2.30 2.30	7.20 7.20	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$, $\overline{G}$		1.40 1.40	4.50 4.50	1.40 1.40	4.20 4.20	1.40 1.40	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{C}_{OUT}$		2.00 2.00	6.30 6.30	2.00 2.00	6.30 6.30	2.10 2.10	6.60 6.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		1.60 1.60	4.90 4.90	1.60 1.60	5.00 5.00	1.60 1.60	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.30 1.30	2.80 2.80	1.40 1.40	2.80 2.80	1.40 1.40	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n		1.40 1.40	8.60 8.60	1.50 1.50	8.40 8.40	1.50 1.50	8.80 8.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$, $\overline{G}$		1.70 1.70	7.20 7.20	2.00 2.00	5.70 5.70	2.00 2.00	6.30 6.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{C}_{OUT}$		2.70 2.70	9.90 9.90	2.80 2.80	8.30 8.30	2.90 2.90	8.50 8.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to F_n		1.00 1.00	3.20 3.20	0.90 0.90	3.40 3.40	1.10 1.10	3.60 3.60	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{C}_{OUT}$, $\overline{P}$, $\overline{G}$		0.45 0.45	2.60 2.60	0.45 0.45	2.50 2.50	0.45 0.45	2.60 2.60	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}$	Waveform 2	6.00		6.00		6.00		ns
t_h	Hold time, $\overline{E}$ to A_n, B_n		0.00		0.00		0.00		ns
t_s	Setup time, S_n to $\overline{E}$		7.00		7.00		7.00		ns
t_h	Hold time, $\overline{E}$ to S_n		0.50		0.50		0.50		ns
t_s	Setup time, $\overline{C}_{IN}$ to $\overline{E}$		4.00		4.00		4.00		ns
t_h	Hold time, $\overline{E}$ to $\overline{C}_{IN}$		0.50		0.50		0.50		ns
$t_w(L)$	Pulse width Low, E	Waveform 1	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

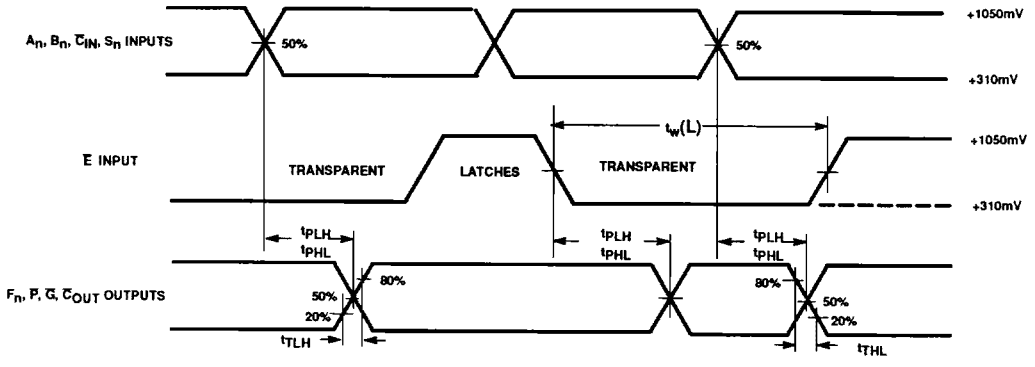
AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC $V_{CC1} = V_{CC2} = \text{ground}$, $V_{EE} = -5.2V \pm 5\%$

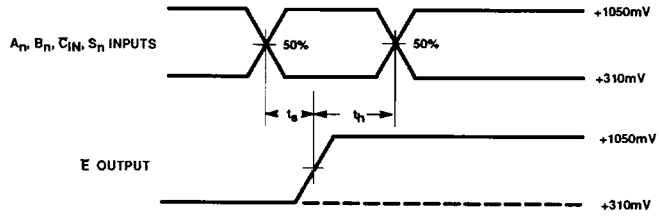
SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0°C$		$T_A = +25°C$		$T_A = +85°C$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to F_n	Waveform 1	2.00 2.00	6.70 6.70	2.10 2.10	6.60 6.60	2.30 2.30	7.20 7.20	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{P}$, $\overline{G}$		1.40 1.40	4.50 4.50	1.40 1.40	4.20 4.20	1.40 1.40	4.50 4.50	ns ns
t_{PLH} t_{PHL}	Propagation delay A_n, B_n to $\overline{C}_{OUT}$		2.00 2.00	6.30 6.30	2.00 2.00	6.30 6.30	2.10 2.10	6.60 6.60	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to F_n		1.60 1.60	4.90 4.90	1.60 1.60	5.00 5.00	1.60 1.60	5.30 5.30	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{C}_{IN}$ to $\overline{C}_{OUT}$		1.30 1.30	2.80 2.80	1.40 1.40	2.80 2.80	1.40 1.40	2.90 2.90	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to F_n		1.40 1.40	8.60 8.60	1.50 1.50	8.40 8.40	1.50 1.50	8.80 8.80	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$, $\overline{G}$		1.70 1.70	7.20 7.20	2.00 2.00	5.70 5.70	2.00 2.00	6.30 6.30	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{C}_{OUT}$		2.70 2.70	9.90 9.90	2.80 2.80	8.30 8.30	2.90 2.90	8.50 8.50	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}$ to F_n		1.00 1.00	3.20 3.20	0.90 0.90	3.40 3.40	1.10 1.10	3.60 3.60	ns ns
t_{TLH} t_{THL}	Transition time F_n, $\overline{C}_{OUT}$, $\overline{P}$, $\overline{G}$		0.45 0.45	2.60 2.60	0.45 0.45	2.50 2.50	0.45 0.45	2.60 2.60	ns ns
t_s	Setup time, A_n, B_n to $\overline{E}$	Waveform 2	6.00		6.00		6.00		ns
t_h	Hold time, $\overline{E}$ to A_n, B_n		0.00		0.00		0.00		ns
t_s	Setup time, S_n to $\overline{E}$		7.00		7.00		7.00		ns
t_h	Hold time, $\overline{E}$ to S_n		0.50		0.50		0.50		ns
t_s	Setup time, $\overline{C}_{IN}$ to $\overline{E}$		4.00		4.00		4.00		ns
t_h	Hold time, $\overline{E}$ to $\overline{C}_{IN}$		0.50		0.50		0.50		ns
$t_w(L)$	Pulse width Low, $\overline{E}$	Waveform 1	2.00		2.00		2.00		ns

NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times



Waveform 2. Setup and Hold Times

NOTE:
All power and signal voltages shifted up 2.0V for AC bench test purposes.