4M x 32 SDRAM / 2M x 8 SDRAM

EXTERNAL MEMORY SOLUTION FOR AGERE'S TAPC640 ATM PORT CONTROLLER

FEATURES

- Clock speeds:
  - SDRAM: 100 MHz
- 100% tested to timing requirements of TAPC640's memory interface
- Packaging:
  - 153 pin BGA, 14mm x 22mm
- 3.3V Operating supply voltage
- Direct control interface to both the BRAM and PRAM ports on the TAPC640
- 62% space savings vs. monolithic solution
- Reduced system inductance and capacitance

DESCRIPTION

The WED9LAPC2B16P8BC is a 3.3V, 4M x 32 Synchronous DRAM and a 2M x 8 Synchronous DRAM array packaged in a 14mm x 22mm 153 lead BGA.

The WED9LAPC2B16P8BC provides the memory required for the BRAM (Buffer Memory) and PRAM (Pointer Memory) memory ports for Agere's TAPC640 ATM port controller. When used in conjunction with the WED9LAPC2C16V4BC, which provides memory for the CRAM (Control Memory) and VCRAM (Virtual Control Memory) memory ports, the entire memory requirement of the LUCTAPC640 can be met using these 2 BGA devices.

The WED9LAPC2B16P8BC is 100% tested to the timing requirements of the TAPC640's memory interface timing for both Commercial and Industrial temperature ranges.

FIG. 1 PIN CONFIGURATION

PINOUT BRAM AND PRAM MCM -- TOP VIEW

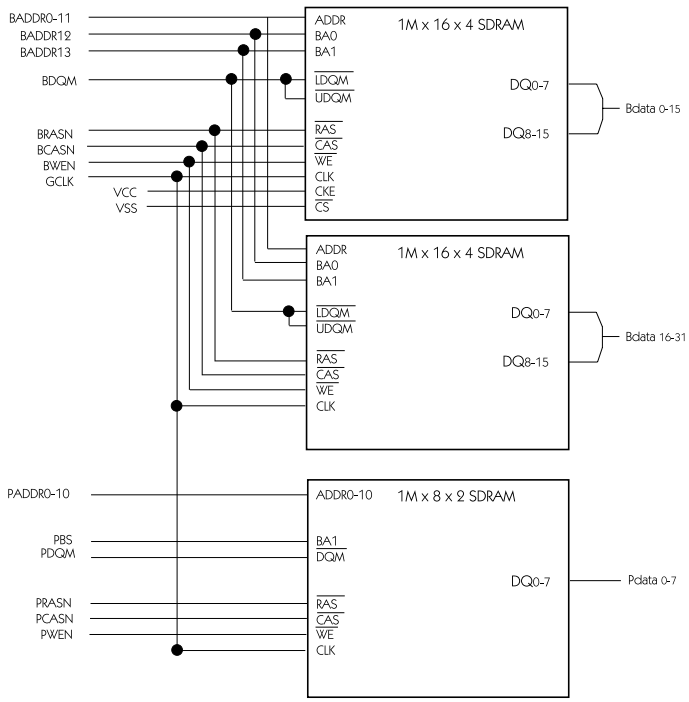
	1	2	3	4	5	6	7	8	9
A	VCC	BDATA_A	BDATA_A	VSS	GCLK	VSS	BWEN	BCASN	BRASN
B	BDATA_A	BDATA_A	BDATA_A	VSS	VSS	NC	VCC	VCC	BDQM
C	BDATA_A	BDATA_A	BDATA_A	VCC	NC	NC	VSS	BADDR9	BADDR11
D	VSS	BDATA_A	BDATA_A	VCC	VCC	VSS	VSS	BADDR7	BADDR8
E	BDATA_A	BDATA_A	BDATA_A	VCC	VCC	VSS	VSS	BADDR5	BADDR6
F	BDATA_A	BDATA_A	BDATA_A	VSS	VCC	VSS	VSS	BADDR3	BADDR4
G	VCC	BDATA_B	BDATA_B	VSS	VCC	VSS	VCC	VCC	VCC
H	BDATA_B	BDATA_B	BDATA_B	VSS	VCC	NC	VSS	BADDR1	BADDR2
J	BDATA_B	BDATA_B	BDATA_B	VCC	NC	NC	VSS	BADDR10	BADDR0
K	VSS	BDATA_B	BDATA_B	VCC	NC	NC	VSS	BADDR12	BADDR13
L	BDATA_B	BDATA_B	BDATA_B	VCC	NC	NC	VCC	VCC	VCC
M	BDATA_B	BDATA_B	BDATA_B	VSS	NC	NC	VSS	PADDR8	PADDR9
N	VCC	VCC	VSS	VSS	NC	NC	VSS	PADDR6	PADD7
P	PDATA	PDATA	VSS	VSS	NC	NC	VSS	PADDR4	PADDR5
R	PDATA	VCC	VSS	VSS	NC	NC	VSS	PADDR2	PADDR3
T	PDATA	VCC	PDATA	VCC	VCC	VCC	PDQM	PADDR0	PADDR1
U	PDATA	PDATA	PDATA	VCC	PCASN	PRASN	PWEN	PBS	PADDR10

FIG. 1 PIN CONFIGURATION (CONTINUED)

PIN DESCRIPTION

SYMBOL	PIN NAME	DESCRIPTION
BADDR	BRAM ADDRESS	ADDRESS PINS FOR THE SDRAM MEMORY THAT SERVES AS THE BUFFER MEMORY (BRAM)
BDATA	BRAM DATA	DATA I/O PINS FOR THE SDRAM BUFFER MEMORY (BRAM)
BADDR12, BADDR13	BRAM BANK SELECT	BANK ADDRESS PIN FOR THE SDRAM BUFFER MEMORY (BRAM)
BDQM	BRAM DQM	DQM (DATA MASK) PIN FOR THE SDRAM BUFFER MEMORY (BRAM)
BRAS	BRAM ROW ADDRESS STROBE	RAS PIN FOR THE SDRAM BUFFER MEMORY (BRAM)
BCAS	BRAM COLUMN ADDRESS STROBE	CAS PIN FOR THE SDRAM BUFFER MEMORY (BRAM)
BWE	BRAM WRITE ENABLE	WRITE ENABLE PIN FOR THE SDRAM BUFFER MEMORY (BRAM)
PADDR	PRAM ADDRESS	ADDRESS PINS FOR THE SDRAM MEMORY THAT SERVES AS THE POINTER MEMORY (PRAM)
PDATA	PRAM DATA	DATA I/O PINS FOR THE SDRAM POINTER MEMORY (PRAM)
PBS	PRAM BANK SELECT	BANK ADDRESS PIN FOR THE SDRAM POINTER MEMORY (PRAM)
PDQM	PRAM DQM	DQM (DATA MASK) PIN FOR THE SDRAM POINTER MEMORY (PRAM)
PRAS	PRAM ROW ADDRESS STROBE	RAS PIN FOR THE SDRAM POINTER MEMORY (PRAM)
PCASN	PRAM COLUMN ADDRESS STROBE	CAS PIN FOR THE SDRAM POINTER MEMORY (PRAM)
PWE	PRAM WRITE ENABLE	WRITE ENABLE PIN FOR THE SDRAM POINTER MEMORY (PRAM)
GCLK	GLOBAL CLOCK	COMMON CLOCK PIN FOR BOTH THE BRAM AND PRAM MEMORY ARRAYS
VCC	POWER SUPPLY	POWER SUPPLY PINS
VSS	GROUND	GROUND PINS

FIG. 2 BLOCK DIAGRAM 4M X 32 SDRAM / 2M X 8 SDRAM



ABSOLUTE MAXIMUM RATINGS

VOLTAGE ON VCC RELATIVE TO VSS	-0.5V TO +4.6V
VIN (DQX)	-0.5V TO VCC +0.5V
STORAGE TEMPERATURE (BGA)	-55°C TO +125°C
JUNCTION TEMPERATURE	+125°C
SHORT CIRCUIT OUTPUT CURRENT	50 mA

**Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

RECOMMENDED DC OPERATING CONDITIONS

(0°C - TA - 70°C; VCC = 3.3V ±5% UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE (1)	VCC	3.135	3.465	V
INPUT HIGH VOLTAGE (1,2)	VIH	2.0	VCC +0.3	V
INPUT LOW VOLTAGE (1,2)	VIL	-0.3	0.8	V
INPUT LEAKAGE CURRENT 0 ≤ VIN ≤ VCC	ILI	-10	10	µA
OUTPUT LEAKAGE (OUTPUT DISABLED) 0 ≤ VIN ≤ VCC	ILO	-10	10	µA
OUTPUT HIGH (IOH = -2mA) (1)	VOH	2.4	—	V
OUTPUT LOW (IOL = 2mA) (1)	VOL	—	0.4	V

NOTES:

1. *All voltages referenced to VSS (GND).*
2. *Overshoot: VIH ≤ +6.0V for t ≤ tKC/2*
   Undershoot: VIL ≥ -2.0V for t ≤ tKC/2

DC ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
OPERATING CURRENT	BRAM AND PRAM ACTIVE	ICC1	170	210	mA	
OPERATING CURRENT	BRAM ACTIVE/PRAM INACTIVE	ICC2	140	160	mA	
OPERATING CURRENT	BRAM INACTIVE/PRAM ACTIVE	ICC3	90	110	mA	
OPERATING CURRENT	BRAM INACTIVE/PRAM INACTIVE	ICC4	40	60	mA	

BGA CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS
ADDRESS INPUT CAPACITANCE (1)	TA = 25°C; f = 1MHz	CI	5	8	pF
INPUT/OUTPUT CAPACITANCE (DQ) (1)	TA = 25°C; f = 1MHz	CO	8	10	pF
CONTROL INPUT CAPACITANCE (1)	TA = 25°C; f = 1MHz	CA	5	8	pF
CLOCK INPUT CAPACITANCE (1)	TA = 25°C; f = 1MHz	CCK	4	6	pF

NOTE:

1. *This parameter is sampled.*

SDRAM AC CHARACTERISTICS

PARAMETER		SYMBOL	MIN	MAX	UNITS
CLOCK CYCLE TIME (1)	CL = 3	tCC	8	1000	ns
	CL = 2	tCC	10	1000	ns
CLOCK TO VALID OUTPUT DELAY (1,2)		tSAC		6	ns
OUTPUT DATA HOLD TIME (2)		tOH	2.5		ns
CLOCK HIGH PULSE WIDTH (3)		tCH	3		ns
CLOCK LOW PULSE WIDTH (3)		tCL	3		ns
INPUT SETUP TIME (3)		tSS	2		ns
INPUT HOLD TIME (3)		tSH	1		ns
CLK TO OUTPUT LOW-Z (2)		tSLZ	1		ns
CLK TO OUTPUT HIGH-Z		tSHZ		6	ns
ROW ACTIVE TO ROW ACTIVE DELAY (4)		tRRD	16		ns
$\overline{RAS}$ TO $\overline{CAS}$ DELAY (4)		tRCD	20		ns
ROW PRECHARGE TIME (4)		tRP	20		ns
ROW ACTIVE TIME (4)		tRAS	48	10,000	ns
ROW CYCLE TIME - OPERATION (4)		tRC	70		ns
ROW CYCLE TIME - AUTO REFRESH (4,8)		tRFC	70		ns
LAST DATA IN TO NEW COLUMN ADDRESS DELAY (5)		tCDL	1		CLK
LAST DATA IN TO ROW PRECHARGE (5)		tRDL	2		CLK
LAST DATA IN TO BURST STOP (5)		tBDL	1		CLK
COLUMN ADDRESS TO COLUMN ADDRESS DELAY (6)		tCCD	1		CLK
NUMBER OF VALID OUTPUT DATA (7)				2	EA
				1	EA

NOTES:

1. *Parameters depend on programmed CAS latency.*
2. *If clock rise time is longer than 1ns (tRISE/2 -0.5)ns should be added to the parameter.*
3. *Assumed input rise and fall time = 1ns. If trise of tFALL are longer than 1ns. [(tRISE = tFALL)/2] - 1ns should be added to the parameter.*
4. *The minimum number of clock cycles required is detemined by dividing the minimum time required by the clock cycle time and then rounding up to the next higher integer.*
5. *Minimum delay is required to complete write.*
6. *All devices allow every cycle column address changes.*
7. *In case of row precharge interrupt, auto precharge and read burst stop.*
8. *A new command may be given tRFC after self-refresh exit.*

CLOCK FREQUENCY AND LATENCY PARAMETERS

(UNIT = NUMBER OF CLOCK)

CYCLE TIME	CAS LATENCY	tRC	tRAS	tRP	tRRD	tRCD	tCCD	tCDL	tRDL
		70ns	48ns	20ns	16ns	20ns	10ns	10ns	10ns
8.0ns	3	9	6	3	2	3	1	1	2
10.0ns	2	7	5	2	2	2	1	1	2

REFRESH CYCLE PARAMETERS

PARAMETER	SYMBOL	MIN	MAX	UNITS
REFRESH PERIOD (1,2)	tREF	—	64	ms

NOTES:

1. *4096 cycles.*
2. *Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.*

SDRAM COMMAND TRUTH TABLE

FUNCTION		BRAS OR PRAS	BCAS OR PCAS	BWE OR PWE	BDQM OR PDQM	BADDR12, BADDR13 OR PBS	BADDR OR PADDR	NOTES
MODE REGISTER SET		L	L	L	X	OP CODE		
AUTO REFRESH (CBR)		L	L	H	X	X	X	
PRECHARGE	SINGLE BANK	L	H	L	X	BA	L	2
	PRECHARGE ALL BANKS	L	H	L	X	X	H	
BANK ACTIVATE		L	H	H	X	BA	ROW ADDRESS	2
WRITE		H	L	L	X	BA	L	2
WRITE WITH AUTO PRECHARGE		H	L	L	X	BA	H	2
READ		H	L	L	X	BA	L	2
READ WITH AUTO PRECHARGE		H	L	H	X	BA	H	2
BURST TERMINATION		H	H	L	X	X	X	3
NO OPERATION		H	H	H	X	X	X	
DATA WRITE/OUTPUT DISABLE		X	X	X	L	X	X	4
DATA MASK/OUTPUT DISABLE		X	X	X	H	X	X	4

NOTES:
1. All of the SDRAM operations are defined by states of BWE or PWE, BRAS or PRAS, BCAS or PCAS, and BDQM or PDQM at the positive rising edge of the clock.
2. Bank Select (BADDR12, BADDR13, or PBS), if BADDR12, BADDR13, or PBS = 0 then bank A is selected, if BADDR12, BADDR13, or PBS = 1 then bank B is selected.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS latency.
4. The BDQM or PDQM has two functions for the data DQ Read and Write operations. During a Read cycle, when BDQM or PDQM goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. BDQM or PDQM also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).

SDRAM CURRENT STATE TRUTH TABLE

Current State	Command						Action	Notes
	BRAS or PRAS	BCAS or PCAS	BWE or PWE	BADDR12, BADDR13, or PBS	BADDR or PADDR	Description		
Idle	L	L	L	OP Code		Mode Register Set	Set the Mode Register	1
	L	L	H	X	X	Auto or Self Refresh	Start Auto	1
	L	H	L	X	X	Precharge	No Operation	
	L	H	H	BA	Row Address	Bank Activate	Activate the specified bank and row	
	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	2
	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	1
	H	H	L	X	X	Burst Termination	No Operation	1
	H	H	H	X	X	No Operation	No Operation	
Row Active	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	Precharge	3
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	1
	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	4,5
	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	4,5
	H	H	L	X	X	Burst Termination	No Operation	
	H	H	H	X	X	No Operation	No Operation	
Read	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	Terminate Burst; Start the Write cycle	5,6
	H	L	H	BA	Column	Read	Terminate Burst; Start a new Read cycle	5,6
	H	H	L	X	X	Burst Termination	Terminate the Burst	
	H	H	H	X	X	No Operation	Continue the Burst	
Write	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	Terminate Burst; Start a new Write cycle	5,6
	H	L	H	BA	Column	Read	Terminate Burst; Start the Read cycle	5,6
	H	H	L	X	X	Burst Termination	Terminate the Burst	
	H	H	H	X	X	No Operation	Continue the Burst	
Read with Auto Precharge	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	ILLEGAL	
	H	L	H	BA	Column	Read	ILLEGAL	
	H	H	L	X	X	Burst Termination	ILLEGAL	
	H	H	H	X	X	No Operation	Continue the Burst	

SDRAM CURRENT STATE TRUTH TABLE (CONT.)

Current State	Command					Description	Action	Notes
	BRAS or PRAS	BCAS or PCAS	BWE or PWE	BADDR12, BADDR13, or PBS	BADDR or PADDR			
Write with Auto Precharge	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	ILLEGAL	
	H	L	H	BA	Column	Read	ILLI	
	H	H	L	X	X	Burst Termination	ILLEGAL	
	H	H	H	X	X	No Operation	Continue the Burst	
Precharging	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	No Operation; Bank(s) idle after trp	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	2
	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	20
	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after trp	
	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after trp	
Row Activating	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	ILLEGAL	2
	H	L	H	BA	Column	Read	ILLEGAL	2
	H	H	L	X	X	Burst Termination	No Operation; Row active after trcd	
	H	H	H	X	X	No Operation	No Operation; Row active after trcd	
Write Recovering	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	6
	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	6
	H	H	L	X	X	Burst Termination	No Operation; Row active after tdpl	
	H	H	H	X	X	No Operation	No Operation; Row active after tdpl	
Write Recovering with Auto Precharge	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	2
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	H	L	L	BA	Column	Write	ILLEGAL	2,6
	H	L	H	BA	Column	Read	ILLEGAL	2,6
	H	H	L	X	X	Burst Termination	No Operation; Precharge after tdpl	
	H	H	H	X	X	No Operation	No Operation; Precharge after tdpl	

SDRAM CURRENT STATE TRUTH TABLE (CONT.)

Current State	Command						Action	Notes
	BRAS or PRAS	BCAS or PCAS	BWE or PWE	BADDR12, BADDR13, or PBS	BADDR or PADDR	Description		
Refreshing	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	H	L	L	BA	Column	Write	ILLEGAL	
	H	L	H	BA	Column	Read	ILLEGAL	
	H	H	L	X	X	Burst Termination	No Operation; Idle after t_{RC}	
	H	H	H	X	X	No Operation	No Operation; Idle after t_{RC}	
Mode Register Accessing	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	H	L	X	X	Precharge	ILLEGAL	
	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	H	L	L	BA	Column	Write	ILLEGAL	
	H	L	H	BA	Column	Read	ILLEGAL	
	H	H	L	X	X	Burst Termination	ILLEGAL	
	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	

NOTES:

1. *Both Banks must be idle otherwise it is an illegal action.*
2. *The Current State refers only refers to one of the banks, if BADDR12, BADDR13, or PBS selects this bank then the action is illegal. If BADDR12, BADDR13, or PBS selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.*
3. *The minimum and maximum Active time (t_{RAS}) must be satisfied.*
4. *The BRAS or PRAS to BCAS or PCAS Delay (t_{RCD}) must occur before the command is given.*
5. *Address VCADDR9/AP is used to determine if the Auto Precharge function is activated.*
6. *The command must satisfy any bus contention, bus turn around, and/or write recovery requirements. The command is illegal if the minimum bank-to-bank delay time (t_{RRD}) is not satisfied.*

FIG. 3 SDRAM POWER UP SEQUENCE

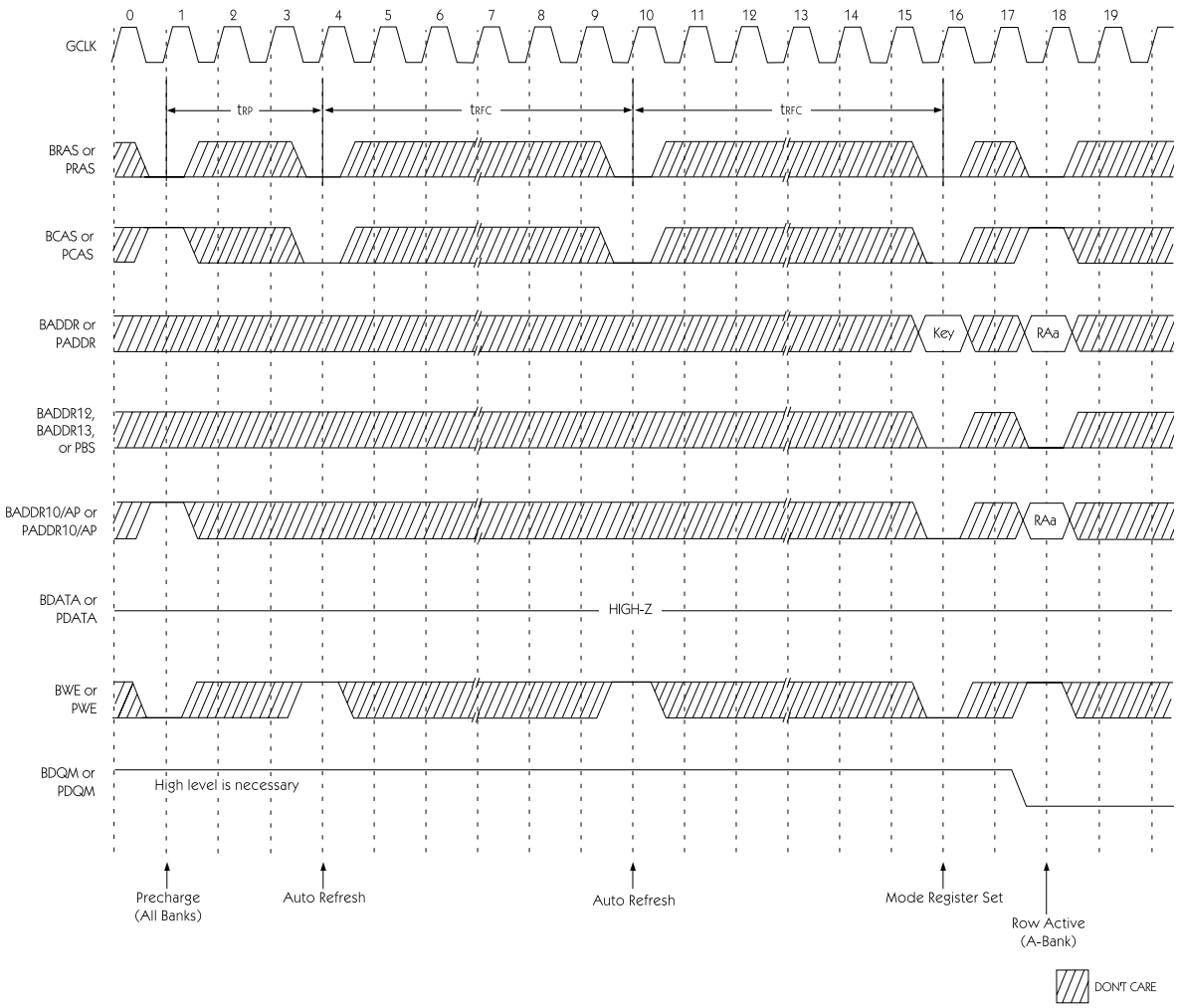


FIG. 4 SDRAM SINGLE BIT READ-WRITE-READ CYCLE (SAME PAGE) @ CAS LATENCY = 3, BURST LENGTH = 1

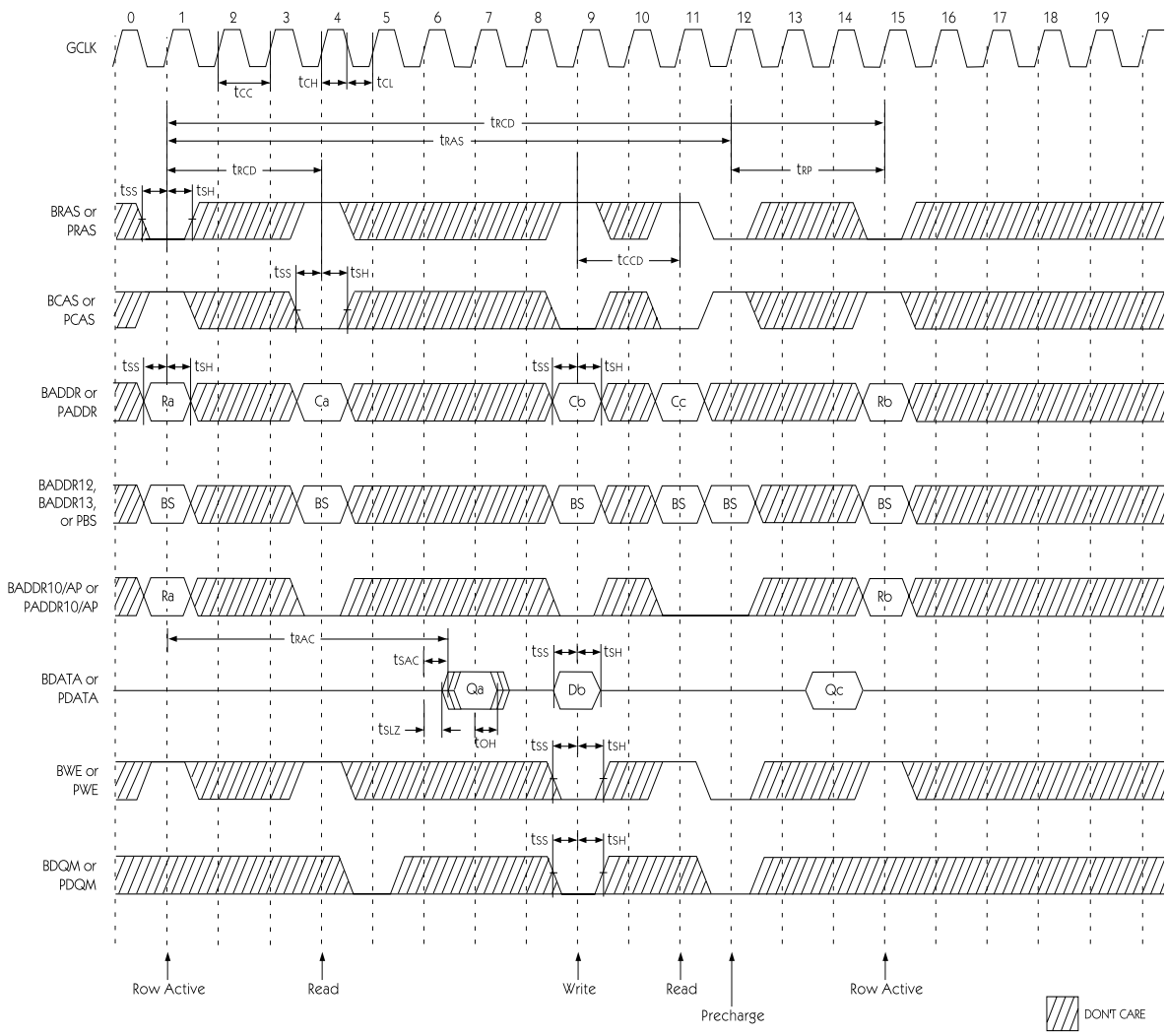
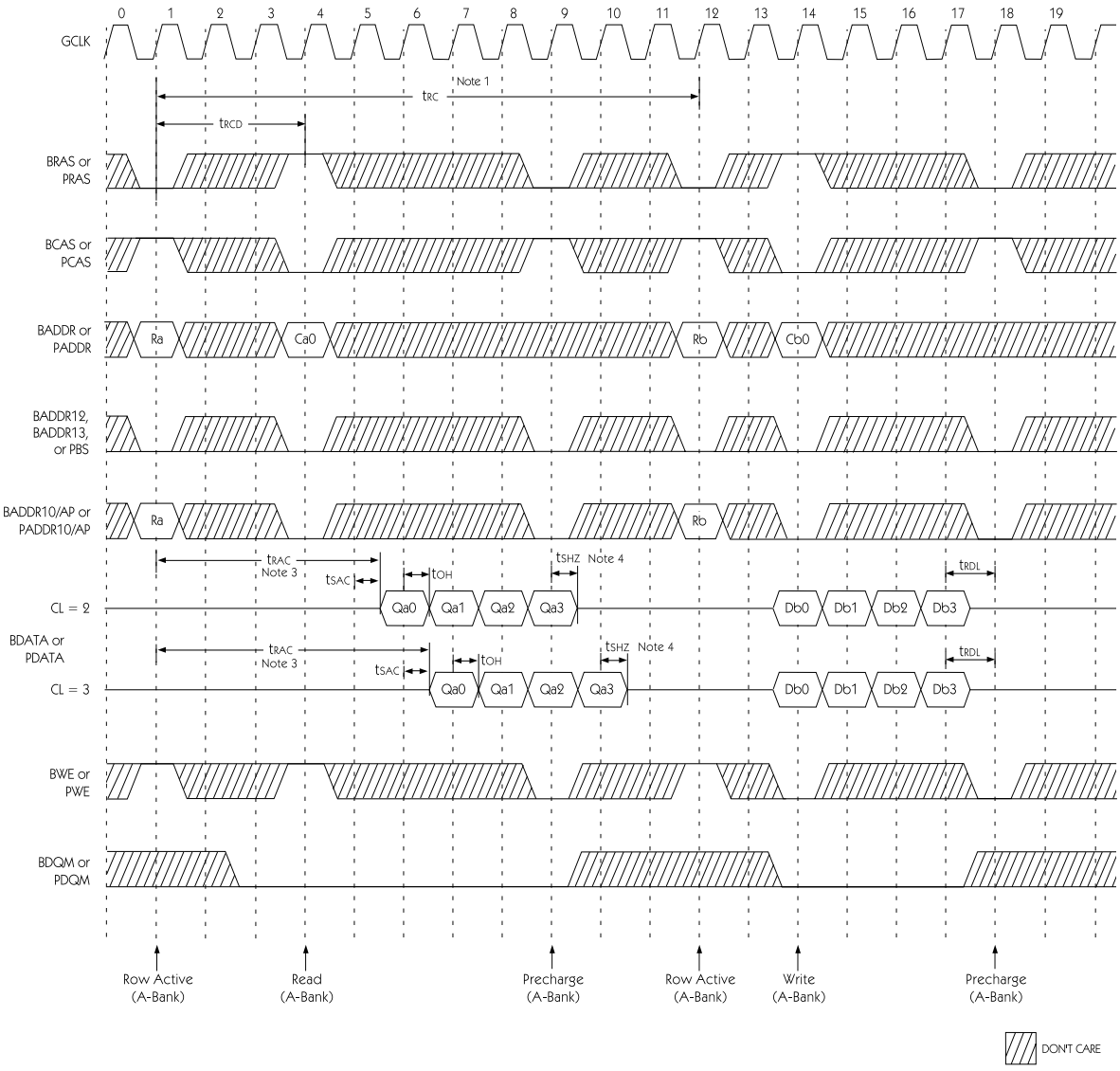


FIG. 5 SDRAM READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4



NOTES:

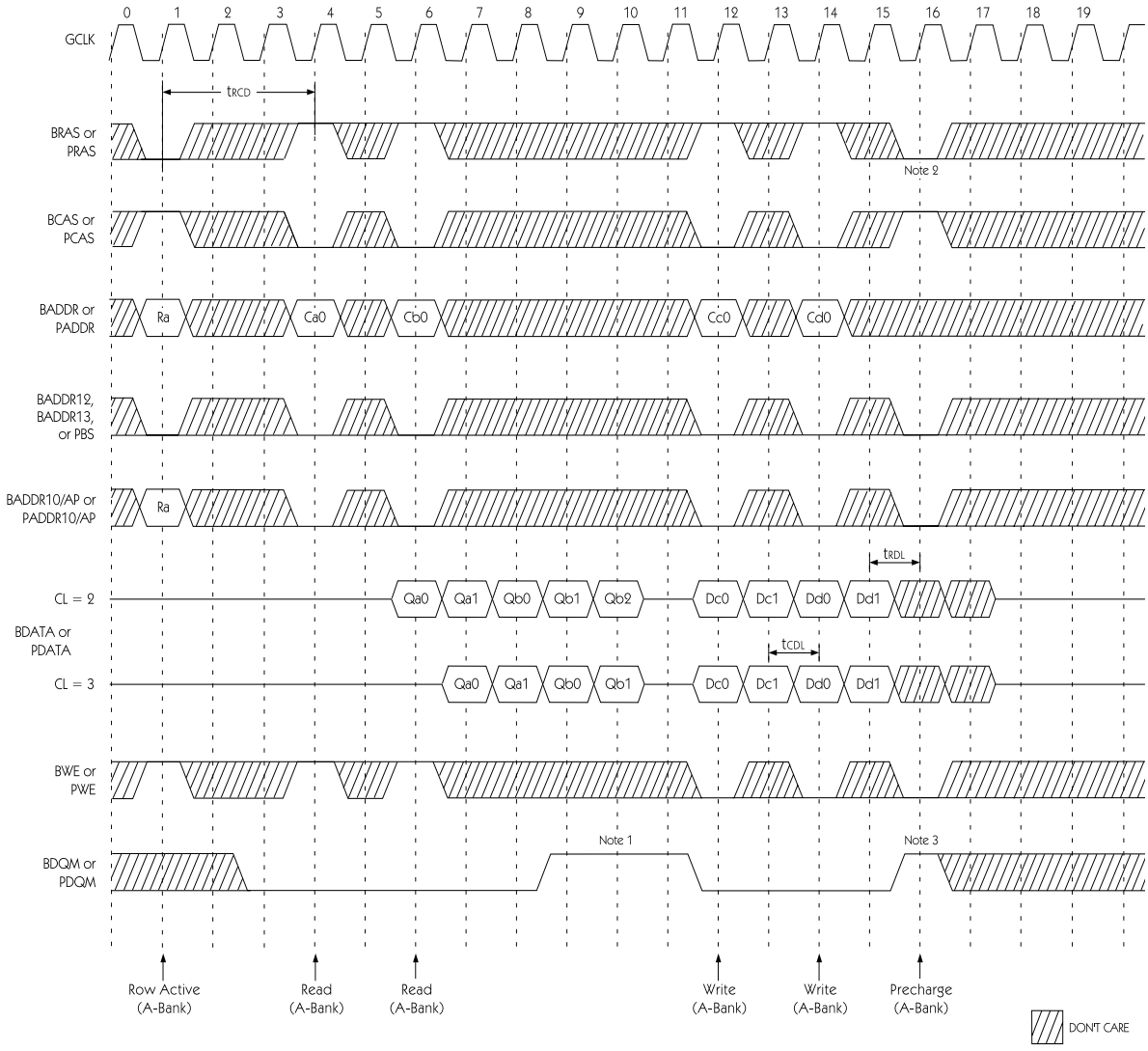
1. Minimum row cycle times are required to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle. (CAS Latency - 1) number of valid output data is available after Row precharge. Last valid output will be Hi-Z (t_{SHZ}) after the clock.

3. Access time from Row active command. t_{CC}(t_{RCD} + CAS Latency - 1) + t_{SAC}.*

4. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

FIG. 6 SDRAM PAGE READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4



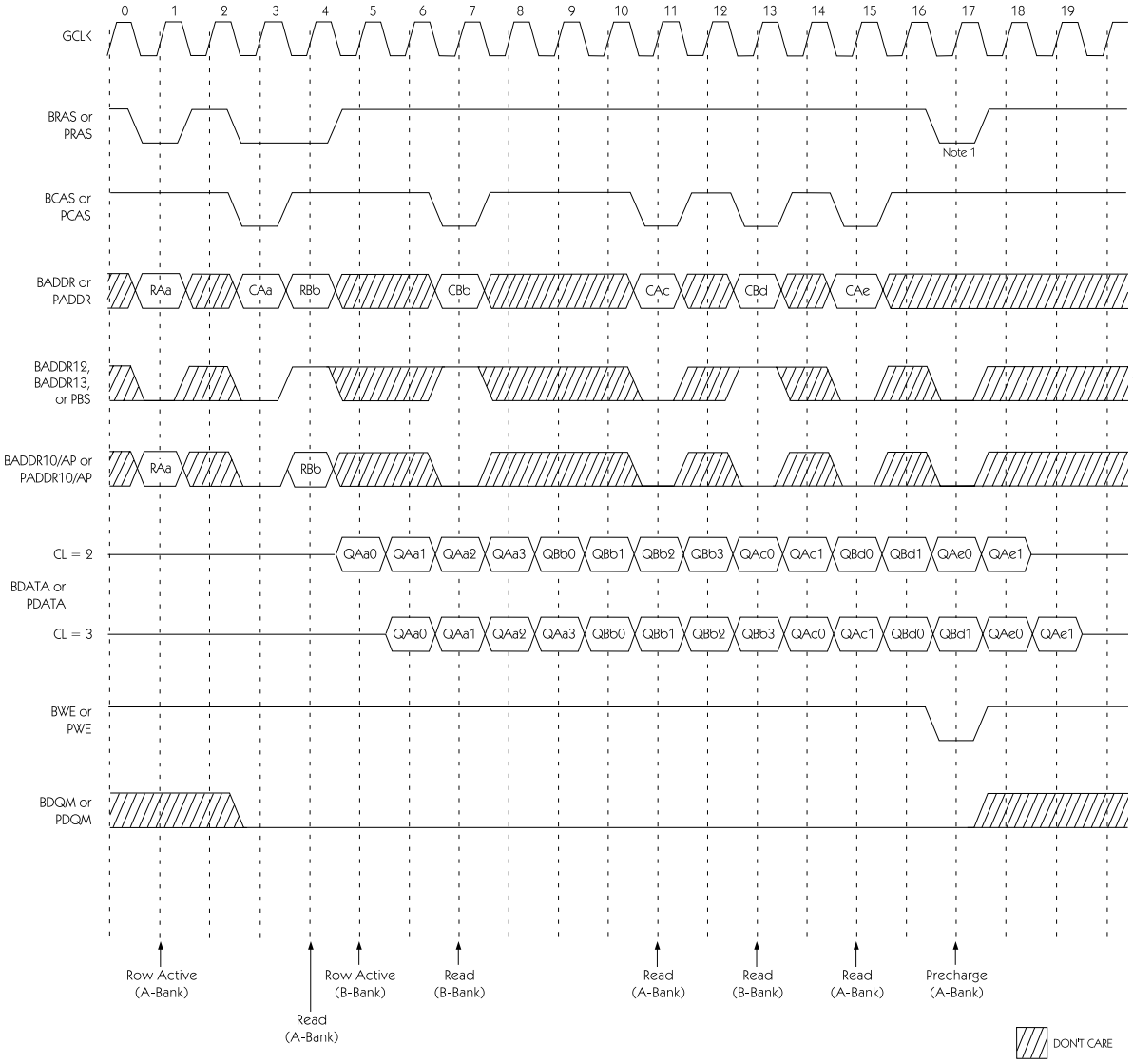
NOTES:

1. To write data before burst read ends. BDQM or PDQM should be asserted three cycle prior to write command to avoid bus contention.

2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge will be written.

3. BDQM or PDQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

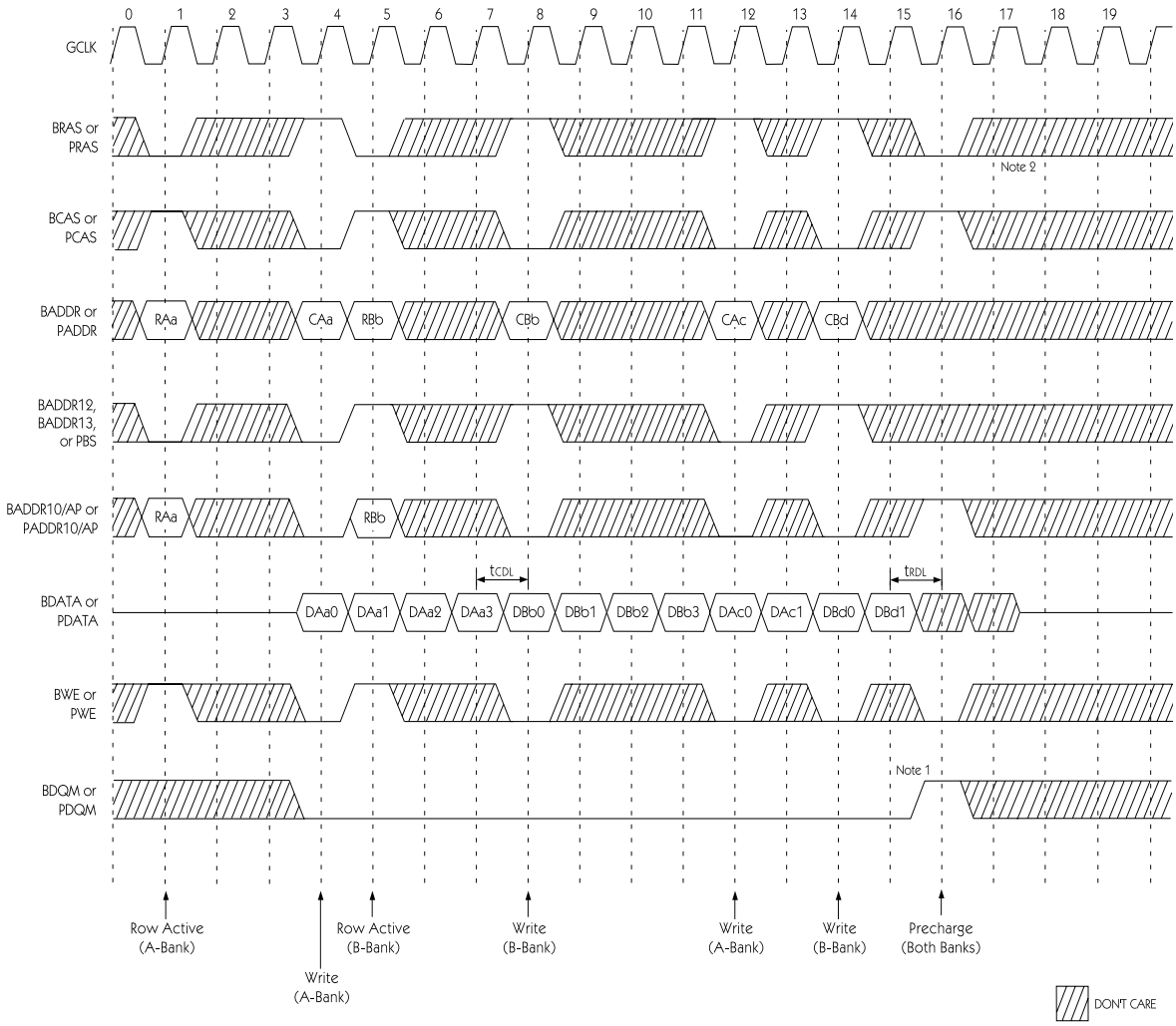
FIG. 7 SDRAM PAGE READ CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



NOTE:

1. To interrupt a burst read by Row precharge, both the read and the precharge banks must be the same.

FIG. 8 SDRAM PAGE WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4

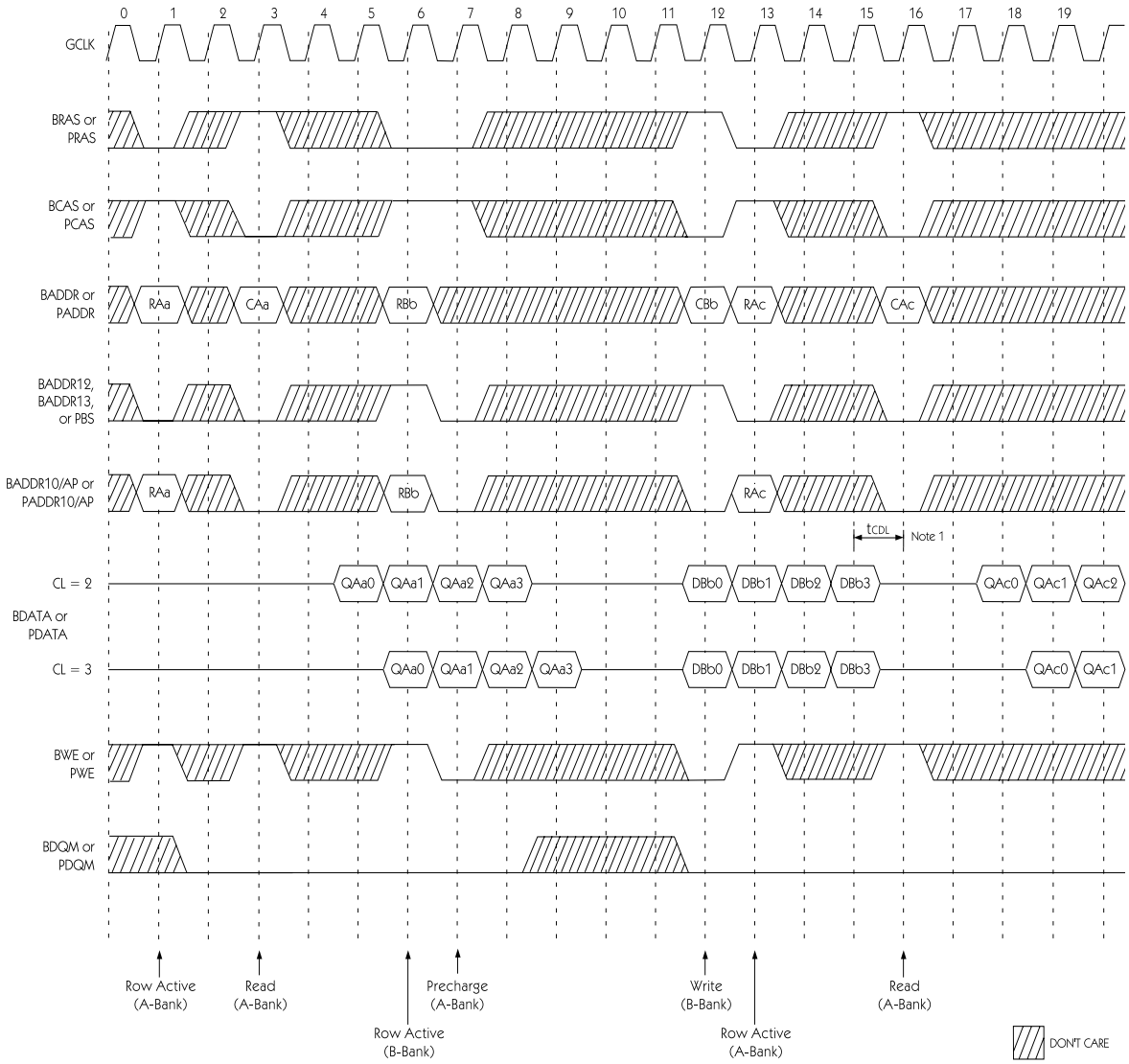


NOTES:

1. To interrupt burst write by Row precharge, BDQM or PDQM should be asserted to mask invalid input data.

2. To interrupt a burst read by Row precharge, both the read and the precharge banks must be the same.

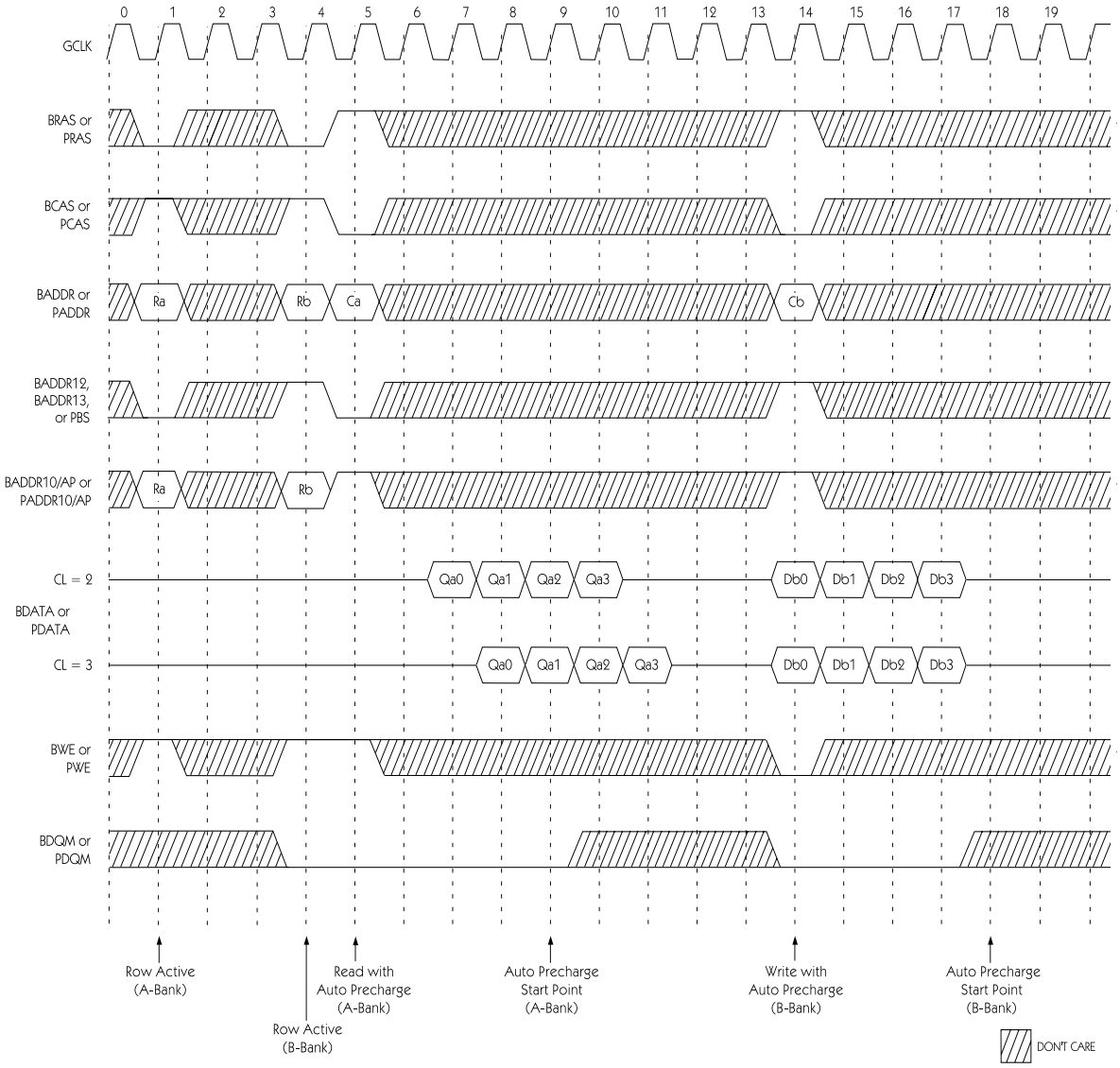
FIG. 9 SDRAM READ & WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



NOTE:

1. t_{CDL} should be met to complete write.

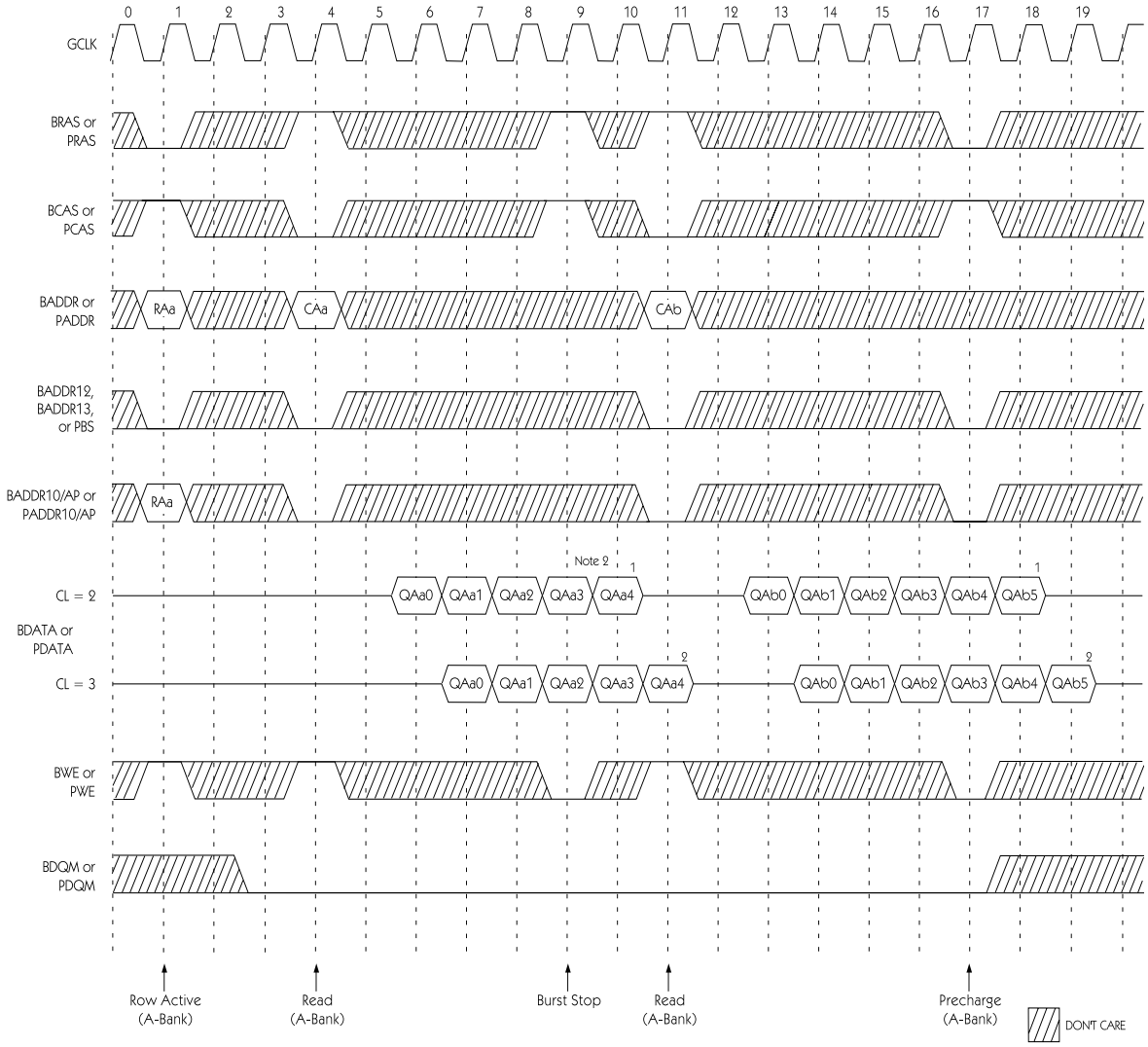
FIG. 10 SDRAM READ & WRITE CYCLE WITH AUTO PRECHARGE @ BURST LENGTH = 4



NOTE:

1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start. (In the case of Burst Length = 1 & 2 and BRSW mode)

FIG. 11 SDRAM READ INTERRUPTED BY PRECHARGE COMMAND & READ BURST STOP @ BURST LENGTH = FULL PAGE



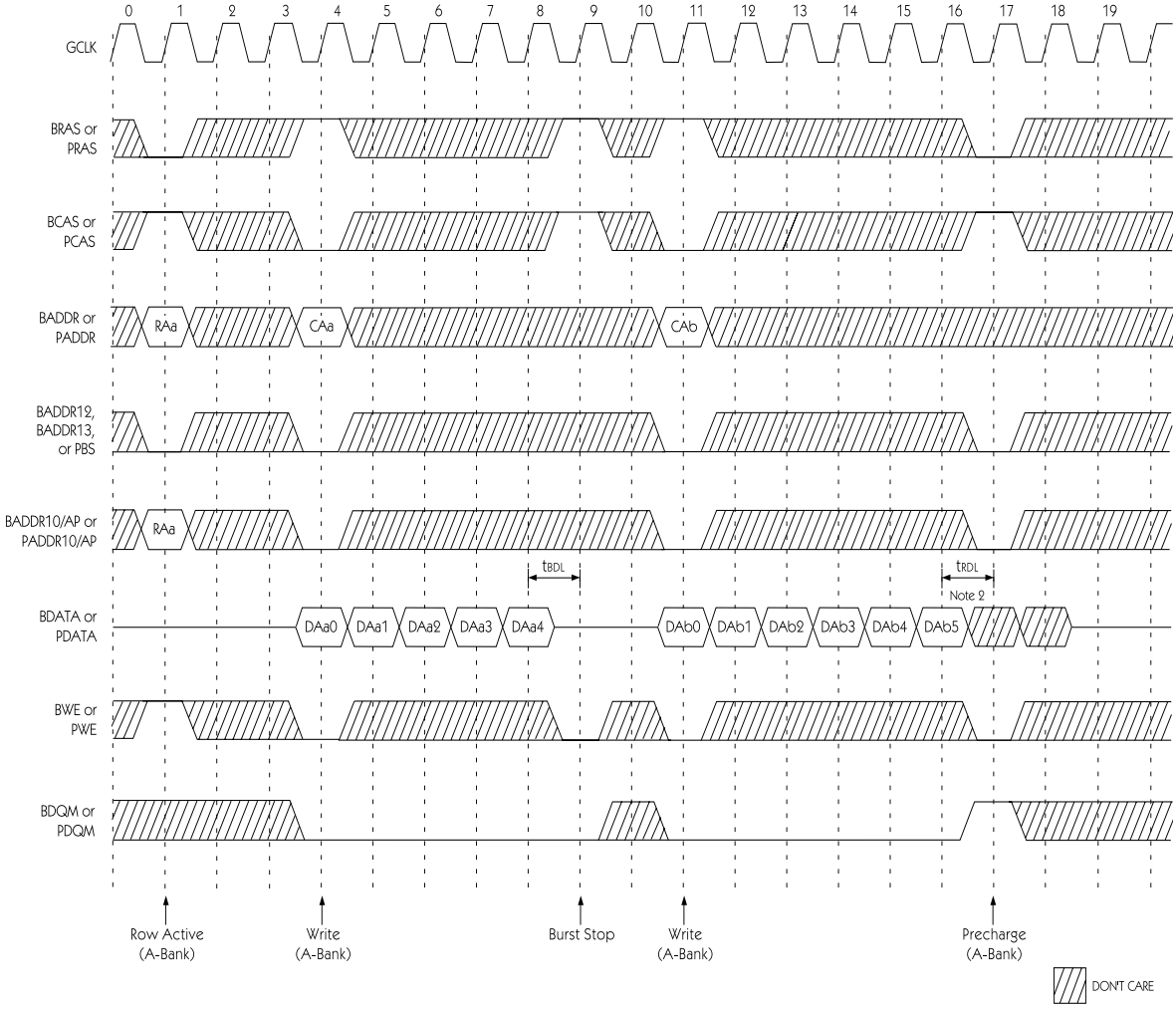
NOTES:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.

2. About the valid BDATAs or PDATAs after burst stop, it is the same as the case of BRAS or PRAS interrupt. Both cases are illustrated in the above timing diagram. See the label 1, 2 on each of them. But at burst write, burst stop and BRAS or PRAS interrupt should be compared carefully. Refer to the timing diagram of "Full page write burst stop cycle."

3. Burst stop is valid at every burst length.

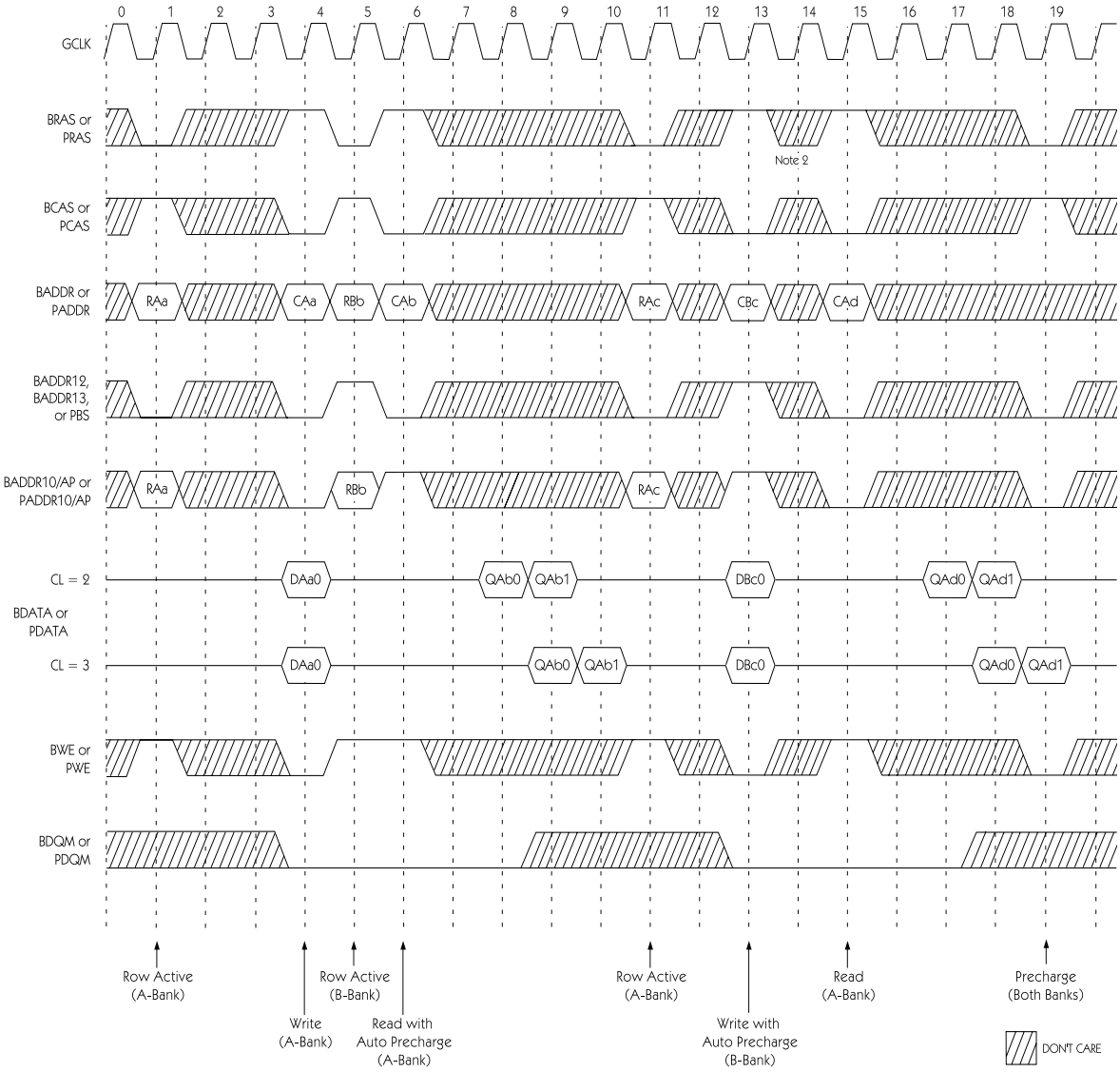
FIG. 12 SDRAM WRITE INTERRUPTED BY PRECHARGE COMMAND & WRITE BURST STOP @ BURST LENGTH = FULL PAGE



NOTES:

1. *At full page mode, burst is end at the end of burst. So auto precharge is possible.*
2. *Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of* t_{RDL}.
   BDQM or PDQM at write interrupt by precharge command is needed to prevent invalid write.
   BDQM or PDQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. *Burst stop is valid at every burst length.*

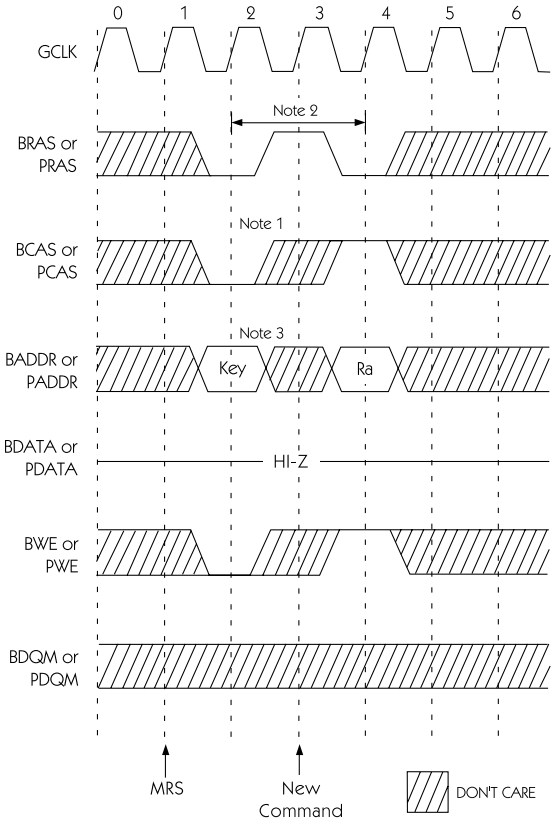
FIG. 13 SDRAM BURST READ SINGLE BIT WRITE CYCLE @ BURST LENGTH = 2



NOTES:

1. *BRSW modes enabled by setting A9 "High" at MRS (Mode Register Set).*
   At the BRSW Mode, the burst length at Write is fixed to "1" regardless of programmed burst length.
2. *When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated.*
   Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

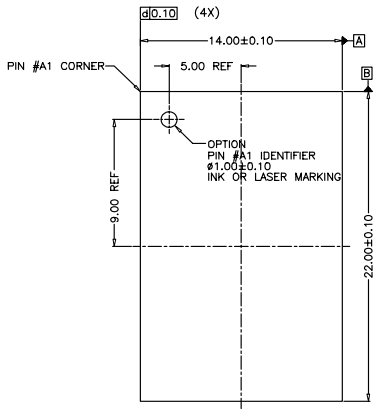
FIG. 14
SDRAM MODE REGISTER SET CYCLE



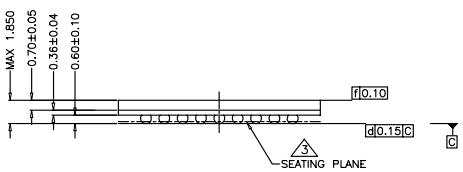
**Both banks precharge should be completed before Mode Register Set cycle.*

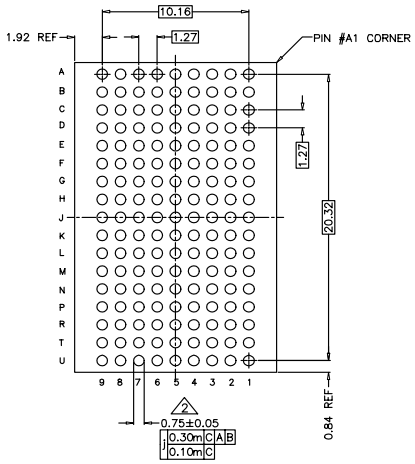
NOTES:
MODE REGISTER SET CYCLE
1. BRAS or PRAS, BCAS or PCAS & BWE or PWE activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new BRAS or PRAS activation.
3. Please refer to Mode Register Set table.

PACKAGE DESCRIPTION: 153 LEAD BGA 14MM X 22MM



TOP VIEW





BOTTOM VIEW

NOTE
1. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y 14.5M–1994.
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C .
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. THE SURFACE FINISH OF THE PACKAGE SHALL BE EDM CHARMILLE #24–#27
5. UNLESS OTHERWISE SPECIFIED TOLERANCE : DECIMAL ±0.05
ANGULAR ±2°

Note: Ball attach pad for above BGA package is 480 microns in diameter. Pad is solder mask defined.

ORDERING INFORMATION

WED9LAPC2B16P8BC	Commercial Temperature:	0°C to +70°C
WED9LAPC2B16P8BI	Industrial Temperature:	-40°C to +85°C