TELTONE® M-900

M-900 DTMF FILTER AND DECODER SET

T-75-27-13

The Teltone® M-900 is a two-LSI chip set that decodes Dual-Tone Multifrequency (DTMF) telephone signals. The set consists of a TT6177 DTMF Filter and a TT6174 Digital Tone Receiver, as shown in Figure 1. Input is from Touch-Tone® telephones, radio, prerecorded tape, or other sources. Output formats are 2 of 8, 1 of 12, binary, or blank. Outputs drive CMOS, low-power Schottky TTL, or transistor drivers.

The set includes a buffer amplifier, dial tone filter, bandsplit filters, and a crystal-controlled digital frequency detector capable of detecting all 16 DTMF digits. A dial pulse counter detects rotary dial digits. The set can be programmed to accept DTMF signals only, rotary dial pulses only, or mixed DTMF and rotary dial input. DTMF signaling is ideal when long distance audio level transmission is required.

The M-900 is manufactured under U.S. Patent 4,145,576.

Features

- Meets CEPT overall performance requirement of less than one false operation per 10,000 digits dialed
- Meets CCITT recommendations for tone receivers
- Provides superior signal-to-noise characteristics and speech immunity
- Flexible gain parameters
- Input filter rejects high-frequency noise
- Buffered clock outputs
- Performance not layout sensitive, no specific trace pattern required between the chips

Telephone Switching Applications

- Central office products
- PBX and intercom systems
- Consumer-oriented special feature phones and systems
- Radio equipment interface to telephone network

Access and Control Applications

- Answering and recording devices
- Radio communication remote switching
- Remote control of machinery or microprocessors
- Monitoring equipment

Data Entry Applications

- Remote computer and peripheral systems interface
- Consumer credit and shopping systems
- Telephone banking, credit, and bill-paying systems

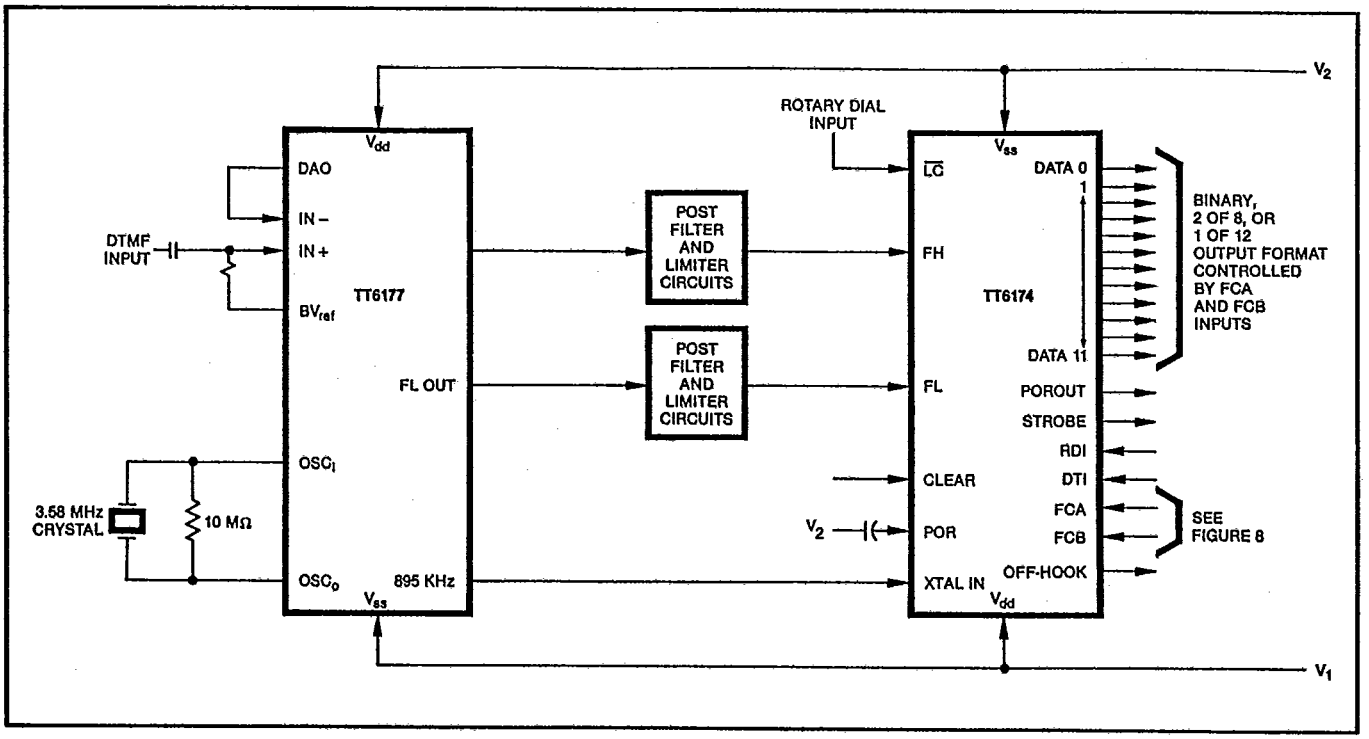

Figure 1 Block Diagram

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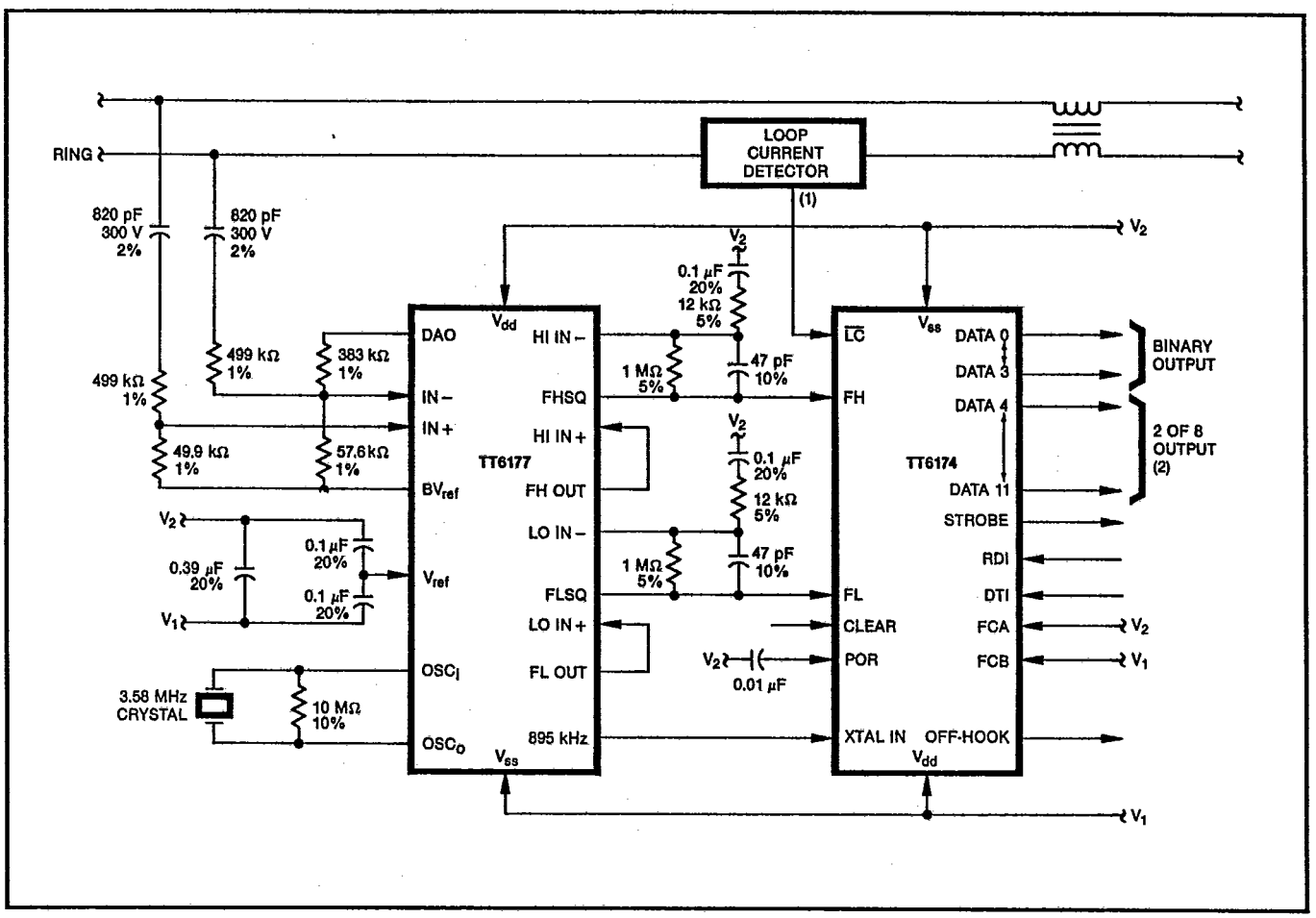


Figure 2 M-900 Typical Application

Table 1 Ordering Information

Ordering Number	Description	Part Number
M-900-01	TT6174-03 Receiver, 40-Pin Plastic TT6177-01 Filter, 18-Pin Plastic	617-00004-03 617-00007-01
M-900-02	TT6174-11 Receiver, 28-Pin Plastic TT6177-01 Filter, 18-Pin Plastic	617-00004-11 617-00007-01
M-900-03	TT6174-04 Receiver, 40-Pin Cer-DIP TT6177-02 Filter, 18-Pin Cer-DIP	617-00004-04 617-00007-02
M-900-04	TT6174-12 Receiver, 28-Pin Cer-DIP TT6177-02 Filter, 18-Pin Cer-DIP	617-00004-12 617-00007-02

Table 2 Typical Application Specifications

Parameter	Typical (Note 1)	Units	Conditions
Input Impedance	500	k ohm	at 1 kHz
Common Mode Noise, 15 Hz to 100 Hz	60	Vrms	
Dial Tone Tolerance	−5	dBm	f ≤ 500 Hz
Precise Dial Tone Tolerance	0	dBm	each tone, 350 Hz and 440 Hz
Signal Detect Level	−30 to +6	dBm	per tone
Signal Reject Level	−40	dBm	per tone
Twist	±10	dB	
Signal-to-Noise Ratio	15	dB	Note 2
Signal Detect Time	38	ms	
Signal Reject Time	27	ms	
Interdigital Pause Detect Time	35	ms	
Interdigital Pause Reject Time	22	ms	

NOTES:
1. These values may vary with your particular circuit arrangements.
2. With the signal level -25 dBm per tone, the signal 50 ms on and 50 ms off, no twist or frequency deviation, all 16 digits signalled randomly, 0 thru 3 kHz flat Gaussian noise, and an error rate of less than one in 10,000. This is essentially the test method of EIA, USITA, and AT & T.

TT6177 Filter

Features

- Internal input amplifier accepts either differential or single-ended signals and provides programmable gain
- Uncommitted op-amps available for use as limiters with programmable gain
- Buffered reference voltage internally derived and externally available
- Greater than 50 dB rejection of each precise dial tone component (350 and 440 Hz)
- Greater than 15 dB of attenuation at 600 Hz
- Greater than 30 dB of intergroup attenuation
- Single or dual power supply operation

Functional Description

As shown in Figure 4, the TT6177 consists of clock circuits, an analog ground circuit, and a multistage DTMF filter circuit with optional limiters.

The clock circuits require only a low-cost 3.579545 MHz television color burst crystal and a 10-megohm resistor as external components. The 149.148 kHz and 27.965 kHz clocks provide the sampling frequencies for the switched-capacitor filter circuits. The buffered 894.886 kHz clock is used to drive the TT6174 Receiver.

The analog ground circuit provides the buffered reference voltage for the switched-capacitor filter circuits. If required, the external capacitors shown in Figure 2 may be added to reduce noise on V_{ss} and V_{dd}. The buffered reference voltage is available externally to bias the Tip and Ring inputs to the DTMF filter and can serve as a reference to compatible external circuits.

The input stages of the DTMF filter circuit consist of a differential amplifier which provides common mode rejection, a low-pass filter which provides high-frequency noise rejection, and a high-pass filter which provides dial tone rejection. The output stages of the DTMF filter consist of two bandsplit filters for separating the high- and low-group DTMF signal components, two low-pass smoothing filters, and two uncommitted operational amplifiers. When connected as shown in Figure 2, the op-amps provide post filtering, gain, and square-wave inputs to the TT6174.

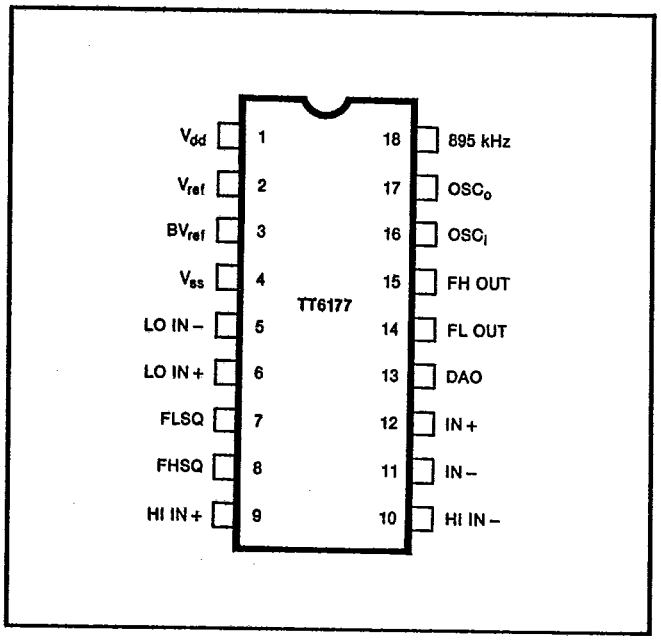


Figure 3 TT6177 Pin Configuration

Table 3 TT6177 Pinouts

Pin Number	Designation	Description	
1	V_{dd}	Positive power supply (+V)	
2	V_{ref}	Reference voltage (input)	
3	BV_{ref}	Buffered reference voltage (output)	
4	V_{ss}	Negative power supply (–V)	
5	LO IN –	Low group limiter inverting input	These two uncommitted op amps may be used for purposes other than limiting.
6	LO IN +	Low group limiter noninverting input	
7	FLSQ	Low group limiter output	
8	FHSQ	High group limiter output	
9	HI IN +	High group limiter noninverting input	
10	HI IN –	High group limiter inverting input	
11	IN –	Differential amplifier inverting input (Ring)	
12	IN +	Differential amplifier noninverting input (Tip)	
13	DAO	Differential amplifier output	
14	FL OUT	Low group smoothing filter output	
15	FH OUT	High group smoothing filter output	
16	OSC_I	Oscillator input	A 3.579545-MHz crystal in parallel with a 10-megohm resistor completes the internal oscillator.
17	OSC_O	Oscillator output	
18	895 kHz	894.886-kHz clock output for use with the TT6174	

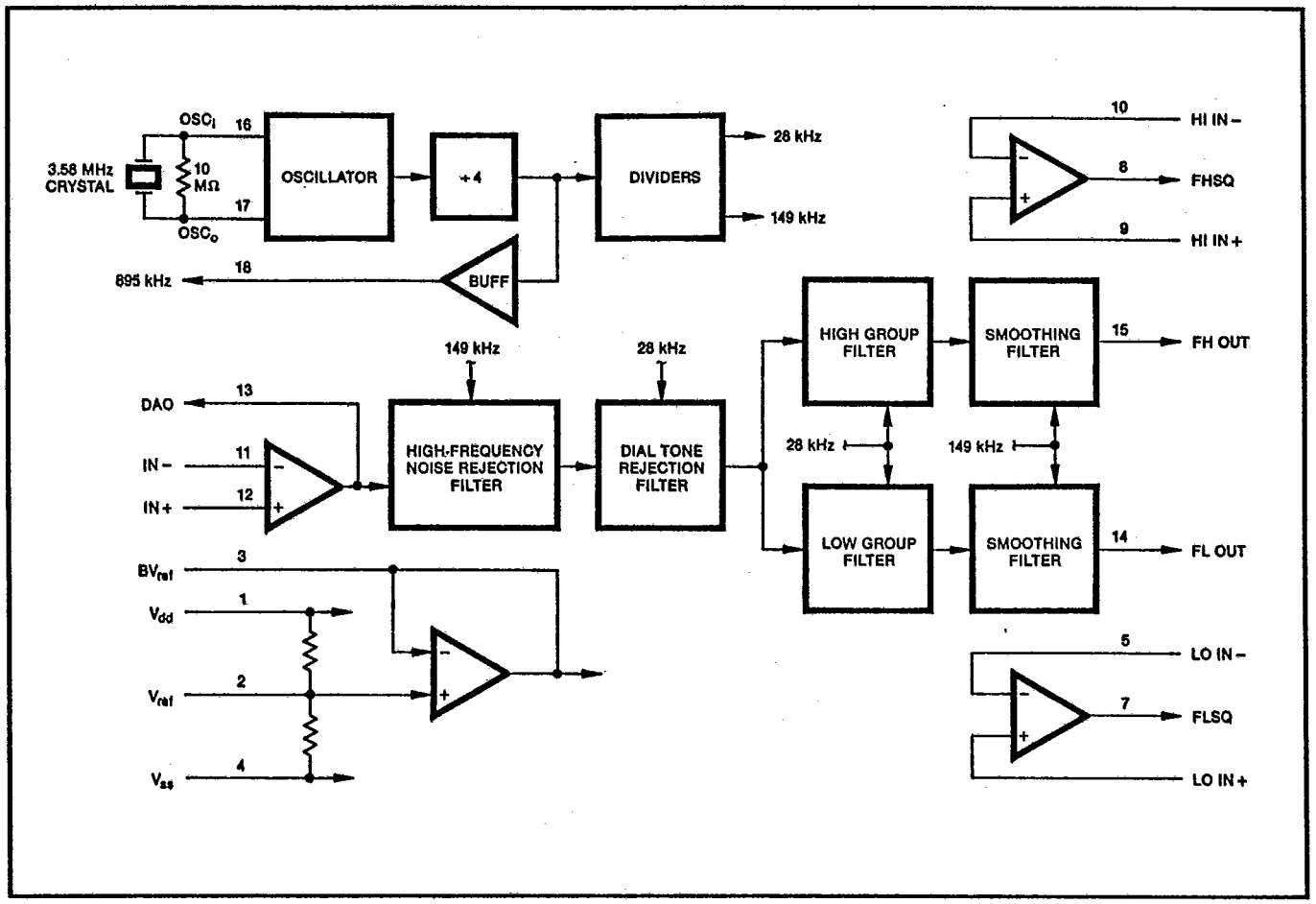


Figure 4 TT6177 Block Diagram

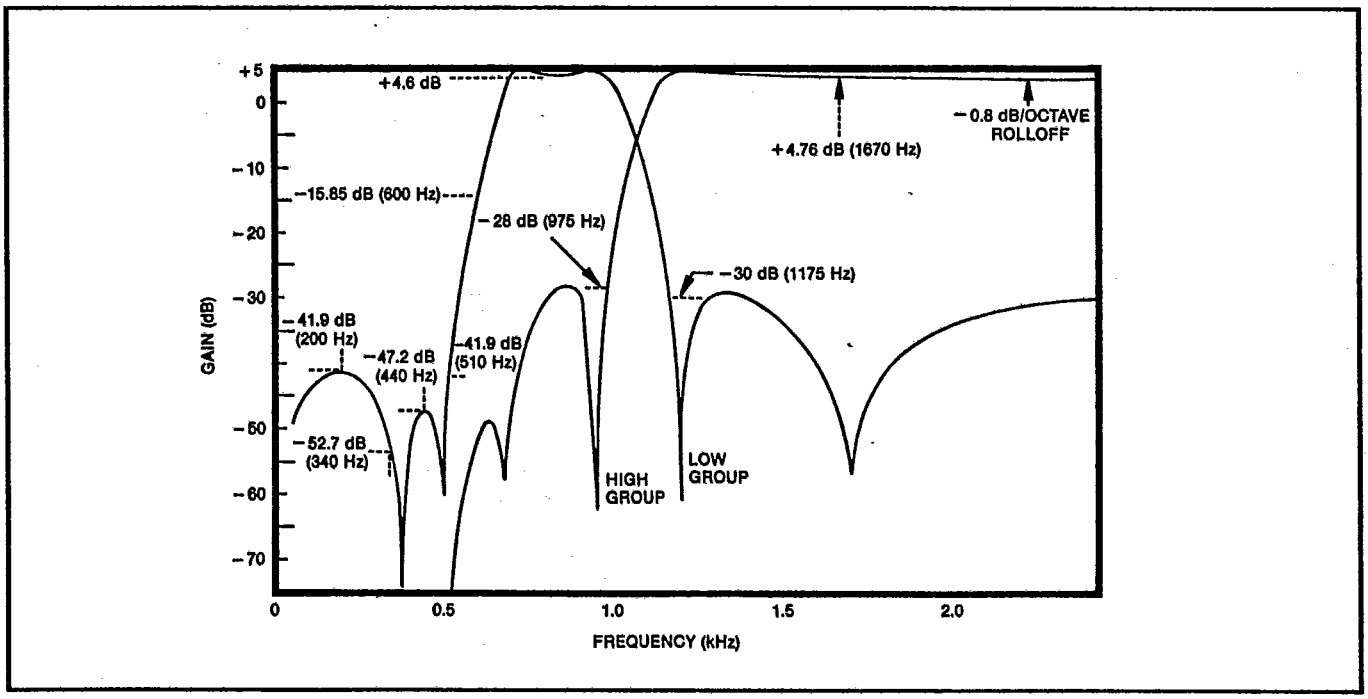


Figure 5 Filter Characteristics

Table 4 TT6177 Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	13.5 V
Power Dissipation	610 mW
Voltage on Any Pin	$(V_2 + 0.3\ V)$ to $(V_1 - 0.3\ V)$
Storage Temperature	−55° to 125° C
Operating Temperature	0° to 70° C ambient air
Lead Soldering Temperature	260° C for 5 seconds at 0.035 inches from package

Notes:
1. Exceeding these ratings may cause permanent damage.
2. V_2 (positive supply) referenced to V_1 (negative supply). V_2 may be at ground.

Table 5 TT6177 DC Electrical Characteristics

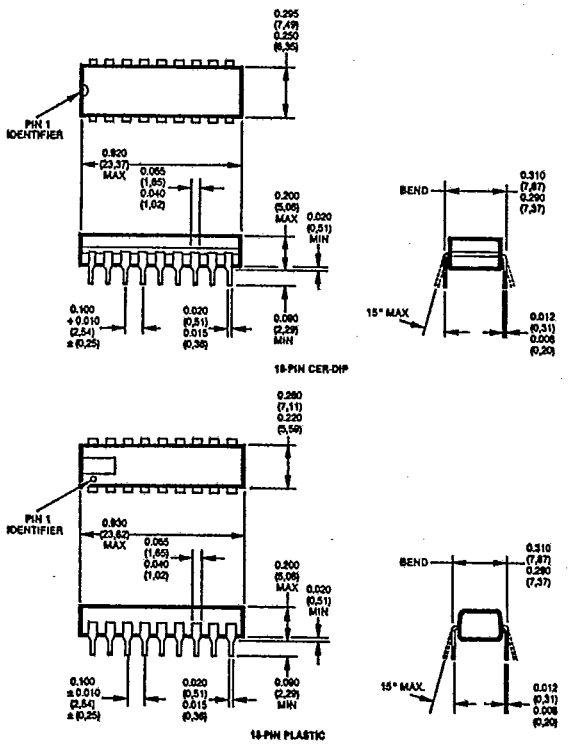
	Parameter	Min	Typ	Max	Units
SUPPLY	Supply Current		30	45	mA
	Supply Voltage	9.5		13.5	V
	BV_{ref}	5.9	6.0	6.1	V
	Ripple Voltage			50	mV
OP AMPS (See note)	Input Resistance	10			MΩ
	Input Offset Voltage		10	25	mV
	Output Signal Voltage		1.5	10.5	V
	Common Mode Voltage	1.5		9.5	V
	Output Load Resistance	40			kΩ
	Output Load Capacitance			10	pF

Note:
Op amps include the input differential amplifier single-ended input and the two uncommitted amplifiers connected as limiters in Figure 2.

Table 6 TT6177 AC Electrical Characteristics

	Parameter		Min	Typ	Max	Units	Conditions
FILTER	Distortion Components				−40	dBm	Signal level at Pin 13 (DAO) no greater than +3 dBm per tone (Note 1)
	Idle Channel Noise				−57	dBm	
	Low Group Bandwidth	low limit		684		Hz	−2 dB from max
		high limit		957		Hz	−2 dB from max
	High Group Bandwidth	low limit		1188		Hz	−2 dB from max
		high limit		1660		Hz	−2 dB from max
	Inband Ripple				2	dB	
	Intergroup Rejection		31			dB	
	300-450 Hz	low group	50			dB	
	Dial Tone Rejection	high group	70			dB	
	600 Hz Rejection	low group	15			dB	
		high group	50			dB	
	Passband Gain		5.5	6.0	6.5	dB	
	Group Delay			4.5	6	ms	Amplitude within 1 dB of final value
OP AMPS (Note 2)	Open Loop Gain		60			dB	
	Input Capacitance				15	pF	
	Unity Gain Bandwidth		1.5			MHz	
	Common Mode Rejection		70			dB	

Notes:
1. Voltage levels stated in dBm are obtained using a standard voltmeter calibrated to provide a scaled voltage measurement in dBm for a 600-ohm impedance. No termination should be applied for this measurement.
2. Op amps include the input differential amplifier which can be used with a single-ended input and the two uncommitted amplifiers connected as limiters in Figure 2.



Package Dimensions

TT6174 Tone Receiver

Features

- Decodes all 16 DTMF digits
- Provides fully time-guarded rotary dial pulse counting
- Three different enable/disable inputs
- Digit presence outputs
- Selectable output formats
- Precision clock outputs

Functional Description

As shown in Figure 9, the TT6174 consists of a multistage digit validation circuit, digit presence logic, an output register/decoder, and a clock circuit. See Table 7 for a complete description of all inputs and outputs.

The digit validation circuit consists of a control stage which enables or inhibits other receiver circuits as determined by its inputs, a DTMF stage which compares the FLSQ and FHSQ outputs of the TT6177 Filter with internal models of the DTMF frequencies, and a rotary dial stage which times and counts makes and breaks of loop current. Detection of a valid digit causes an indication of the digit's presence to be forwarded to the digit presence logic and the identity of the digit to be forwarded to the output register/decoder. The output register/decoder translates the digit into the output format specified by the FCA and FCB inputs. See Figure 8. The 895 kHz output from the TT6177 Filter drives the clock circuit of the TT6174, which in turn provides outputs for use by other devices.

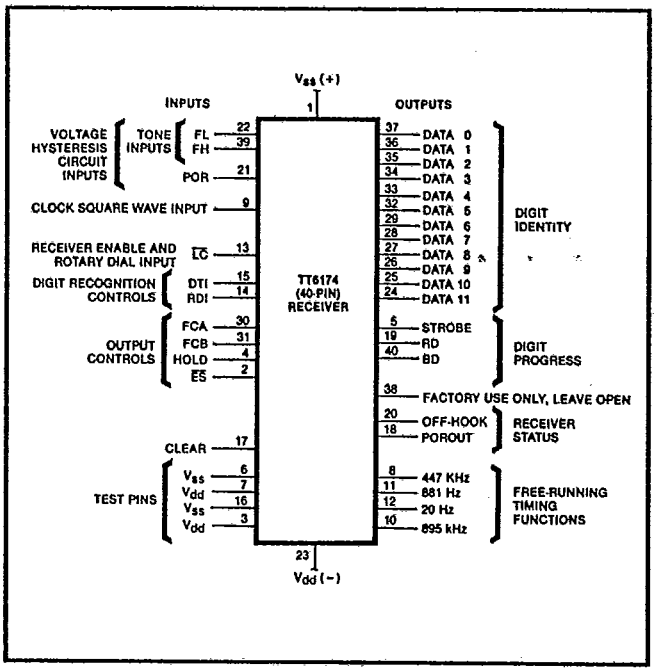


Figure 6 40-pin Receiver Configuration

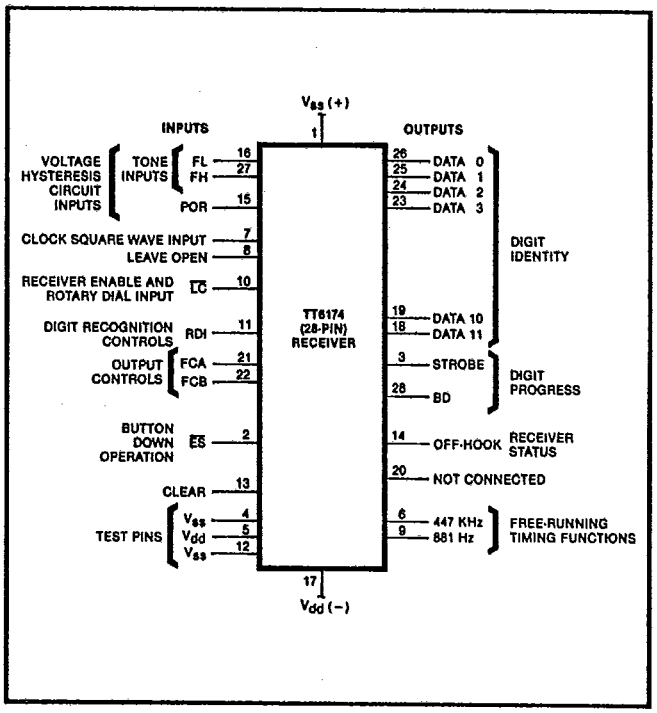


Figure 7 28-pin Receiver Configuration

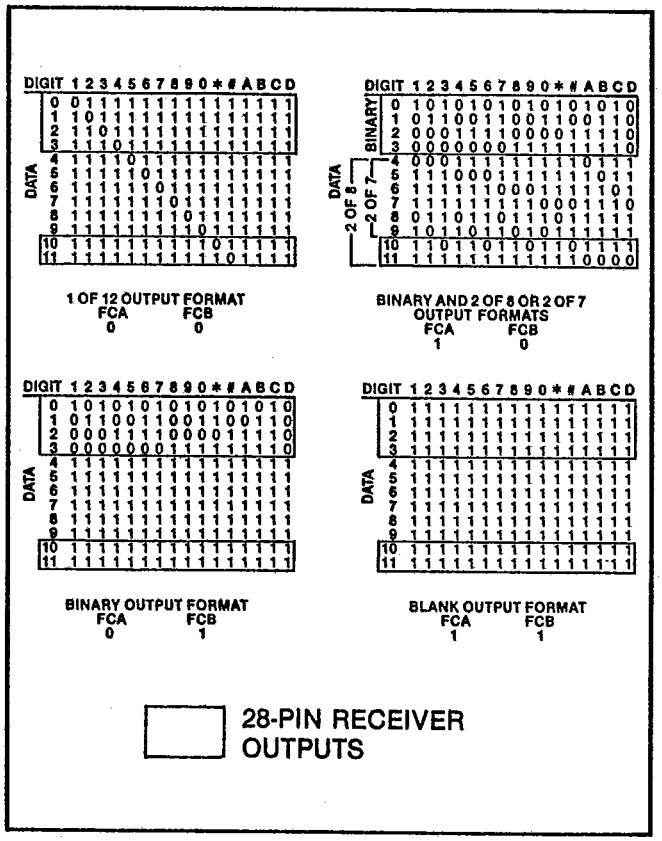
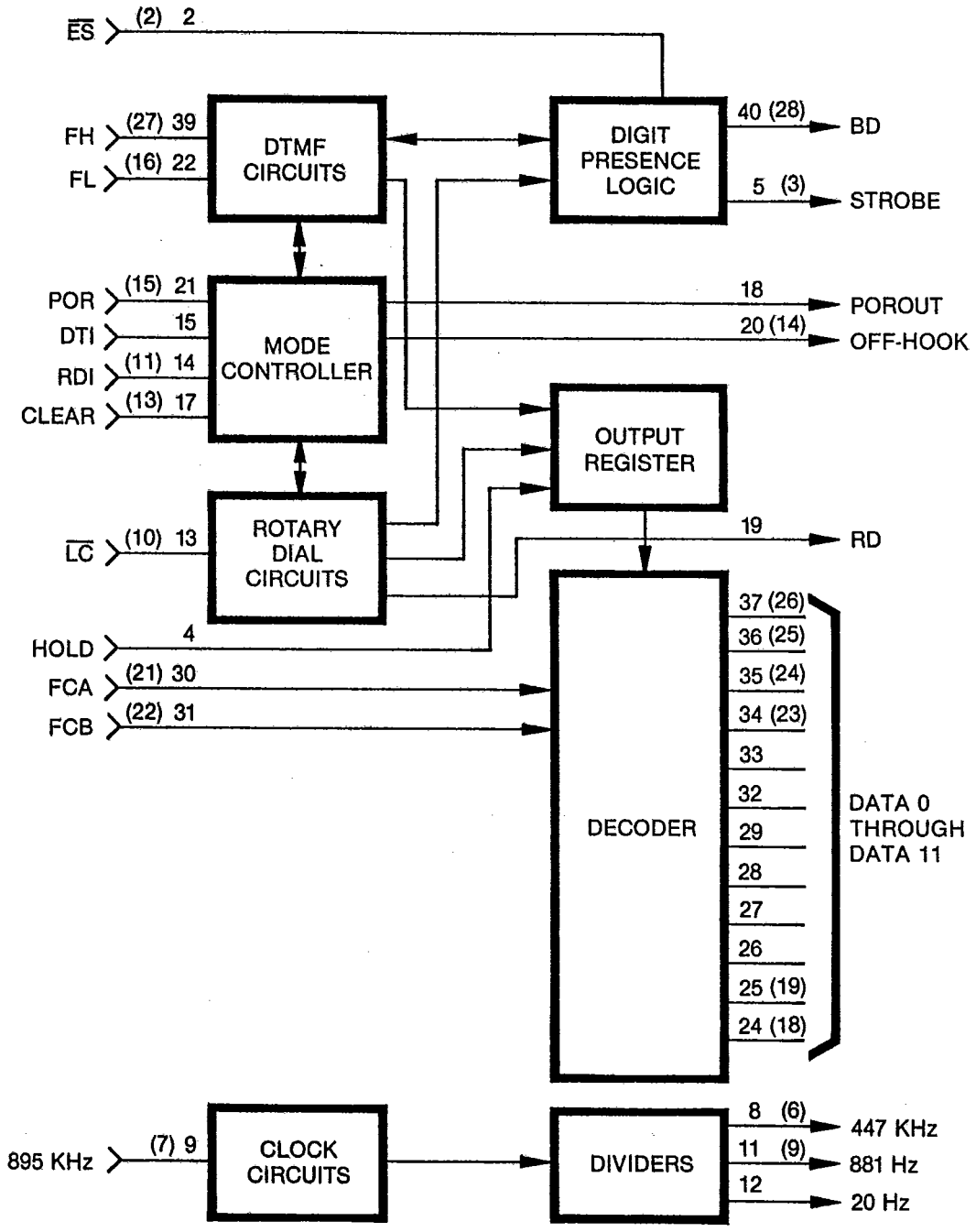


Figure 8 Output Formats



( ) Indicates pin numbers for 28-pin chip.

Figure 9 TT6174 Block Diagram

Table 7 TT6174 Pinouts (Part 1 of 2)

Pin Number	Mnemonic	Description
1 (1)	V_{SS}	Positive power supply (V_3)
2 (2)	$\overline{ES}$	Early Split Not input. When pulled to logic 0 (V_1), ES enables the early tone presence (BD) output.
3		Connect to logic 0.
4	HOLD	Input. For applications where the output data has to remain unchanged for an extended time period, whether or not additional digits have been received, pull HOLD to logic 1 after STROBE goes to logic 1.
5 (3)	STROBE	Valid data output. When DTMF digits are being detected, STROBE goes to the logic 1 state 10 microseconds after the DATA outputs change and returns to the logic 0 state 25 milliseconds (ms) after the end of DTMF detection. When rotary dial digits are being detected, STROBE goes to logic 1 for 200 ms after the interdigital pause is recognized. To read DATA during DTMF signal presence, use the leading edge of STROBE (button-down operation). To read DATA after DTMF signal presence, use the trailing edge of STROBE (button-up operation).
6 (4)		Test input. Connect to logic 1.
7 (5)		Test input. Connect to logic 0.
8 (6)	447 kHz	50-percent duty cycle, PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 2.
9 (7)	CLOCK IN	895-kHz input from the TT6177 Filter.
10 (8)	XTAL OUT	Not used. Leave open.
11 (9)	881 Hz	50-percent duty cycle, PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 1016.
12	20 Hz	50-percent duty cycle, PMOS logic level signal for external use. Actual frequency is the clock frequency divided by 44,704.
13 (10)	$\overline{LC}$	Loop Current Not input. $\overline{LC}$ is both a receiver enable/disable input and the rotary dial pulse input. The TT6174 interprets a logic 0 as an off-hook condition, interdigital pause, or a make period. The TT6174 interprets a logic 1 as an on-hook condition or break period. For DTMF operation only, $\overline{LC}$ can be connected to V_1; then, with POR connected as described below, the receiver is enabled as long as CLEAR is at logic 0.
14 (11)	RDI	Rotary Dial Inhibit Input — For mixed DTMF and rotary dial operation, connect DTI and RDI to logic 0. For rotary dial operation only, connect DTI to logic 1. For DTMF operation only, connect RDI to logic 1. For mode locking on the first digit detected, connect both DTI and RDI to STROBE. The mode lock will be held until the detection circuits are reset.
15	DTI	DTMF Inhibit Input
16 (12)		Test input. Connect to logic 1.
17 (13)	CLEAR	Receiver enable/disable input. A logic 1 applied to the CLEAR input instantaneously resets all detection circuits and forces the DATA outputs to the "D" column of the currently enabled output format (see Figure 8).
18	POROUT	POR output. Responds to input on POR pin.
19	RD	Rotary Dial output. RD provides an early dial pulse presence signal that starts at the leading edge of the first break pulse and ends 100 ms after the trailing edge of the last pulse.
20 (14)	OFF-HOOK	Output. OFF-HOOK goes to the logic 1 state 100 ms after $\overline{LC}$ is pulled to logic 0. OFF-HOOK goes to the logic 0 state 300 ms after $\overline{LC}$ is pulled to logic 1.
21 (15)	POR	Power-On Reset, receiver enable/disable input. A 0.01 µF capacitor connected to V_2 and POR (see Figure 2) causes POROUT to go to logic 1 (V_2) for approximately 10 ms after power is applied. This pulse resets all detection circuits and forces the DATA outputs to the "D" column of the currently enabled output format (see Figure 8).
22 (16)	FL	FLSQ input from the TT6177 Filter
23 (17)	V_{dd}	Negative power supply (V_1)
24 (18)	DATA 11	Data outputs. See Figure 8 for the outputs associated with each output format. A DTMF digit is outputted when it has persisted for 35 ms. A rotary dial digit is outputted when an interdigital pause is recognized.
25 (19)	DATA 10	
26	DATA 9	
27	DATA 8	
28	DATA 7	
29	DATA 6	
(20)		Not used.
30 (21)	FCA	Format Control A input
31 (22)	FCB	Format Control B input — As shown in Figure 8, FCA and FCB determine the DATA output format. FCA and FCB can also be used as a data strobe. By holding both inputs at logic 1, all data outputs will remain at logic 1 until FCA and/or FCB are pulled to logic 0.

Note: Pin numbers for 28-pin receivers are shown in parentheses.

Table 7 TT6174 Pinouts (Part 2 of 2)

Pin Number	Mnemonic	Description
32	DATA 5	
33	DATA 4	
34 (23)	DATA 3	See description to DATA 6 through 11.
35 (24)	DATA 2	
36 (25)	DATA 1	
37 (26)	DATA 0	
38		Leave open.
39 (27)	FH	FHSQ input from the TT6177 Filter
40 (28)	BD	Button Down output. When enabled by $\overline{ES}$ being at logic 0, BD goes to the logic 1 state within 16 ms after a tone pair is detected. BD then returns to the logic 0 state 25 ms after the tone pair ends.

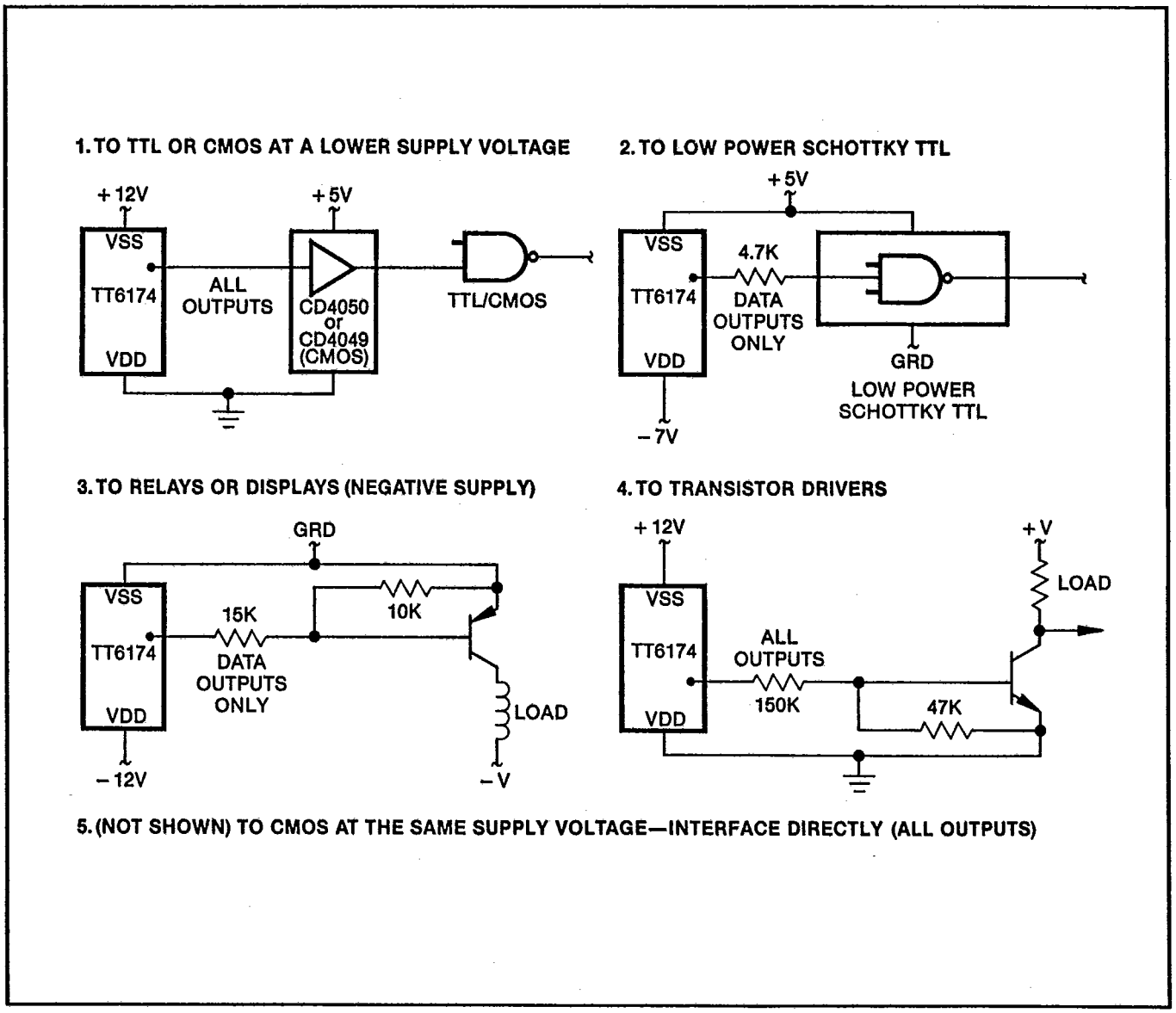


Figure 10 Output Interface Techniques

Table 8 TT6174 Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	14.5 V
Power Dissipation	600 mW
Voltage on Any Pin	$(V_2 + 0.3\ V)$ to $(V_1 - 0.3\ V)$
Storage Temperature	−40° to 150° C
Operating Temperature	0° to 70° C ambient air
Lead Soldering Temperature	260° C for 5 seconds at 0.035 inches from package

Notes:
1. Exceeding these ratings may cause permanent damage.
2. V_2 (positive supply) referenced to V_1 (negative supply). V_2 may be at ground.

Table 9 TT6174 DC Electrical Characteristics

	Parameter	Min	Typ	Max	Units	Conditions
Supply Requirements	Supply Voltage	+11	+12	+14.5	V	V_2 referenced to V_1 (Note 1)
	Ripple Voltage			250	mV	Measured peak-to-peak at 120 Hz
	Supply Current		25	35	mA	14.5 V at 0°C
Logic Inputs	Logic 0 Level			$V_1 + 3.2$	V	
	Logic 1 Level	$V_2 - 2.5$			V	
	Capacitance			15	pF	
	Input Current (Note 2)			50	μA	
Analog Inputs	Logic 0 Threshold	0.57 (ΔV)	0.65 (ΔV)	0.73 (ΔV)	V	ΔV = $V_2 - V_1$
	Logic 1 Threshold	0.43 (ΔV)	0.35 (ΔV)	0.27 (ΔV)	V	ΔV = $V_2 - V_1$
	Capacitance			15	pF	
	Input Current (Note 2)			±50	μA	
Data Outputs	Logic 0 Current Sink			1	mA	Output at $V_1 + 7$ V
	Logic 1 Current Source			100	μA	Output at $V_2 - 2$ V
Non-Data Outputs	Logic 0 Current Sink			100	μA	Output at $V_1 + 2$ V
	Logic 1 Current Source			100	μA	Output at $V_2 - 2$ V

Notes:
1. V_2 more positive than V_1. V_2 may be at ground.
2. The load current must be sourced or sunk to drive an input to its opposite state.

Table 10 TT6174 AC Electrical Characteristics

	Parameter	Min	Typ	Max	Units	Conditions
FL and FH Inputs	Signal Detect Time	27		30	ms	
	Interdigital Pause Detect Time (Note 1)	26		34	ms	
	Interdigital Pause Reject Time (Note 1)	26			ms	
	Signal Detect Bandwidth	−1.5% −2 Hz		+1.5% +2 Hz	Hz	Of each nominal DTMF frequency
	Signal Reject Bandwidth	−3.5%		+3.5%	Hz	Of each nominal DTMF frequency
Inputs Other Than FL and FH	Pulse Width Required to Reset with CLEAR or POR Inputs			25	μs	
	Off-Hook Recognition	95	100	105	ms	$\overline{LC}$ at Logic 0
	Off-Hook Blanking (Note 2)	285	300	315	ms	$\overline{LC}$ at Logic 0
	Break Recognition	24.5		29.5	ms	$\overline{LC}$ at Logic 1
	Make Recognition	7	9	11	ms	$\overline{LC}$ at Logic 0
	End of Digit Recognition	95	100	105	ms	$\overline{LC}$ at Logic 0
	Rotary Interdigital Blanking	190	200	210	ms	
	On-Hook Recognition	290	300	310	ms	$\overline{LC}$ at Logic 1
Available Frequencies	447.433 kHz Pulse Width	2.232	2.234	2.237	μs	
	861 Hz Pulse Width	0.567	0.568	0.569	ms	
	20 Hz Pulse Width (Note 3)	24.95	24.98	25	ms	

Notes:
1. The Interdigital Pause Detect Time is that interval of loss of tones after which the return of the valid tone pair is considered a new digit. The Interdigital Pause Reject Time is the interval a valid tone pair can be interrupted without being treated as a new digit when it returns.
2. Off-Hook Blanking is the delay between $\overline{LC}$ going to logic 0, from being at logic 1 longer than 300 ms, and enabling the digit detection circuits.
3. 40-pin receivers only.

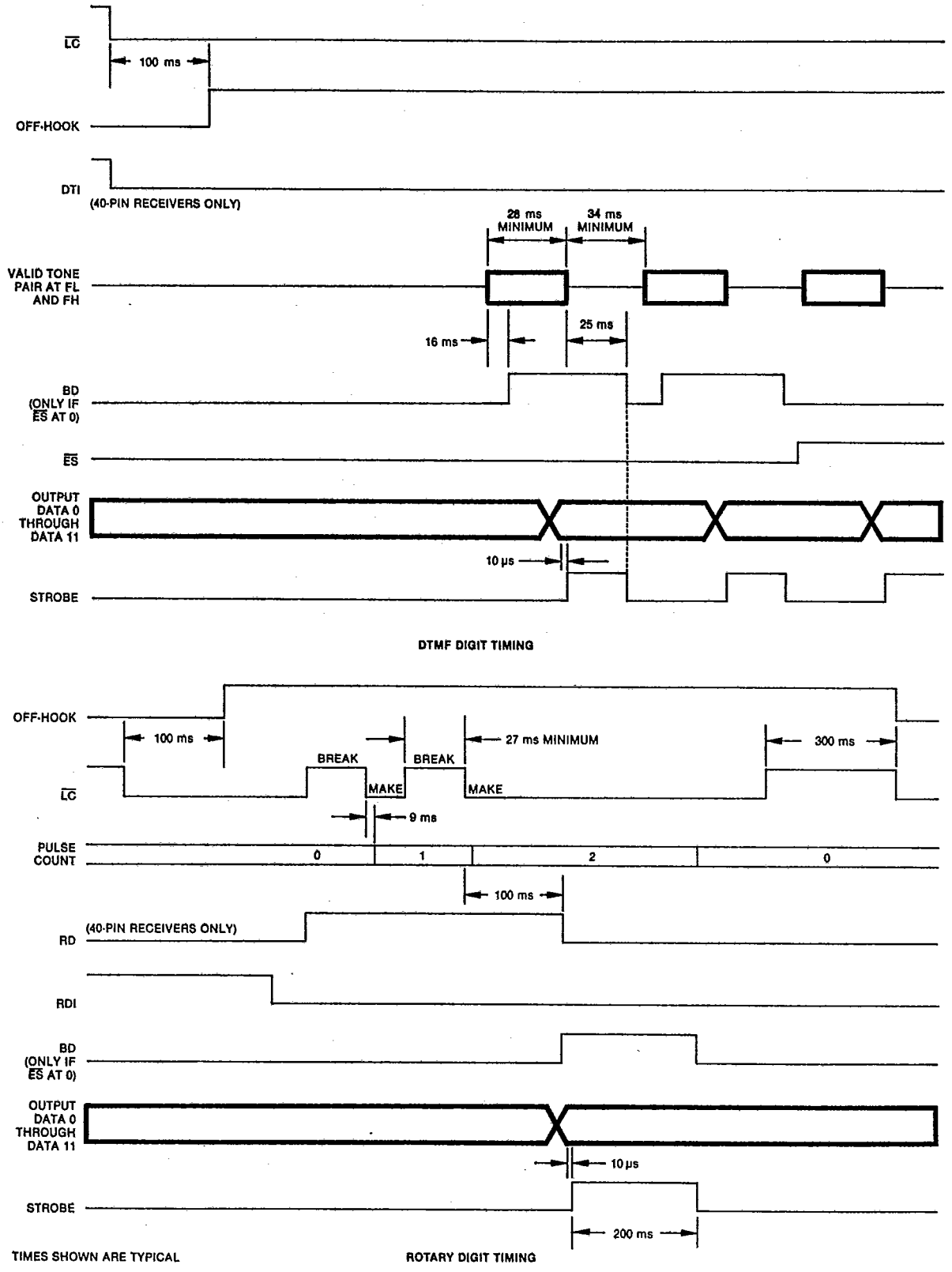


Figure 11 Timing Diagram

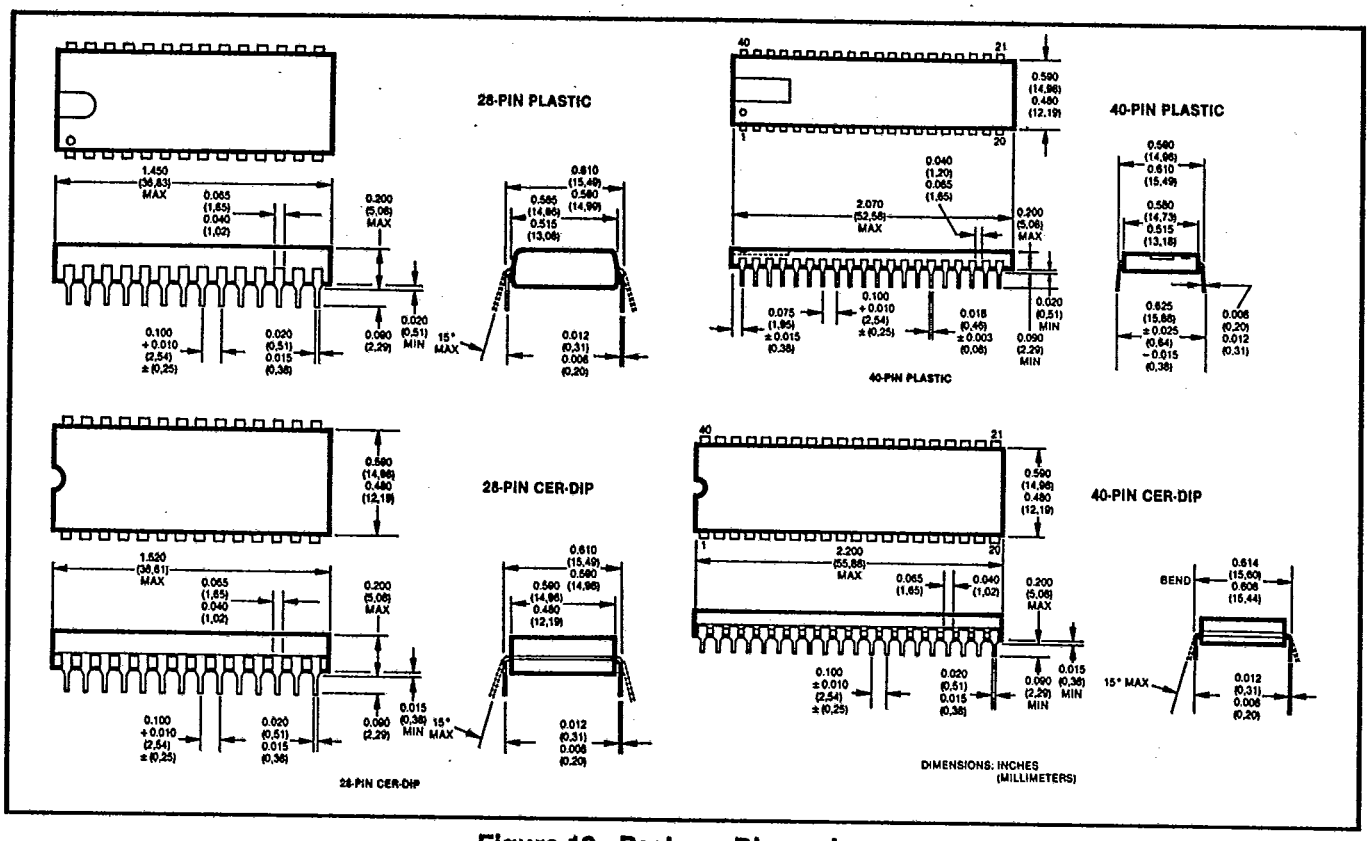


Figure 12 Package Dimensions