QPB9319

Dual-Channel Switch LNA Module

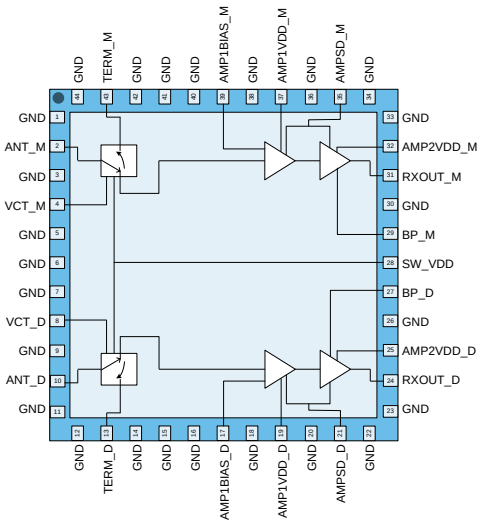
Product Overview

The QPB9319 is a highly integrated front-end module targeted for TDD base stations. The switch LNA module integrates a two-stage LNA and a high power switch in a dual channel configuration. The second stage LNA has integrated bypass mode. Power down and bypass capability for the LNAs can be controlled with control pins on the module.

The QPB9319 can be utilized across the 1.8 – 4.2 GHz range to provide 1.45 dB noise figure for operation in the receive mode and 0.7 dB insertion loss in the transmit mode at 2.7GHz. The LNAs utilize Qorvo's high performance E-pHEMT process while the SOI technology based switch supports input RF power signals of 8W average power. The product only needs a +5V supply to operate the high power switch and the LNAs.

The QPB9319 is packaged in a RoHS-compliant, compact 7 mm x 7 mm surface-mount leadless package. The switch LNA module is targeted for wireless infrastructure applications configured for TDD-based MIMO architectures. The module can be used for next generation 5G or pre-5G solutions or small cell base-station applications.

Functional Block Diagram



Top View

44 Pin 7 mm x 7 mm leadless SMT Package

Key Features

- 1.8-4.2 GHz Frequency Range
- Dual Channel
- Second LNA has bypass mode
- Pin (Tx path): 8W Pavg
- 37 dB Gain (Rx mode, High Gain state)
- 19 dB Gain (RX mode, Low Gain state)
- +34 dBm OIP3 (Rx mode, High gain state)
- +29.5 dBm OIP3 (Rx mode, Low Gain state)
- 1.8V TTL logic compatibility
- 3-5V operation for switch and LNAs
- Compact package size, 7x7 mm

Applications

- Wireless Infrastructure
- Small cell BTS
- Pre-5G / 5G Massive MIMO systems
- TDD-based architectures

Ordering Information

Part No.	Description
QPB9319EVB-01	Evaluation Board
QPB9319SR	100 pcs on 13" reel
QPB9319TR13	2500 pcs on a 13" reel

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
Supply Voltage (Pins 17, 19, 25, 32, 37, 39)	+7 V
Pin at ANT, Rx mode (Pavg, 8 dB PAR, 100% DC, 105°C)	27 dBm
Pin at ANT, Tx mode (Pavg, 8 dB PAR, 88% DC, 8.8ms max pulse-width, 105°C)	39 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
LNA Voltage	+3	+5	+5.25	V
Switch V_{DD}	+3	+5	+5.5	V
T_{CASE}	−40		+105	°C
Tj at max T_{CASE} (1)			+136	°C
Tj (2) (>1e6 hrs MTTF condition)			+125	°C

Notes:

1. For RX Mode operation
2. For TX Mode operation with 5W Pavg power in at 105 °C T_{CASE}.

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Parameter	Conditions (1)	Min	Typ	Max	Units
Operational Frequency Range		1800		4200	MHz
Test Frequency			2700		MHz
Gain (2)	Rx mode, High Gain state	35	37	39	dB
Gain (2)	RX mode, Low Gain state	17	19	21	dB
Gain Flatness	Rx mode, Any 100 MHz BW within band		0.8		dB
Noise Figure (2)	Rx mode		1.45	1.7	dB
Output IP3	Rx mode, High Gain state Pout/tone = +3dBm, Δf = 1MHz	+30	+34		dBm
	Rx mode, Low Gain state Pout/tone = +3dBm, Δf = 1MHz	+25	+29.5		dBm
OP1dB (2)	RX mode, High Gain state	+17	+19		dBm
	RX mode, Low Gain state	+12	+15		dBm
Insertion Loss (2)	Tx mode		0.72	1	dB
Input Return Loss	RX mode		12		dB
Output Return Loss	RX mode		6.5		dB
Return Loss	TX mode		25		dB
Switch Isolation	ANT to TX in RX mode		>25		dB
Switch Isolation	ANT to RX in TX mode		>60		dB
Channel Isolation	RX mode		>40		dB
Channel Isolation	TX mode		>40		dB
LNA Supply Voltage			+5		V
LNA Current	Rx mode, High gain state, Per channel		120	150	mA
LNA Current	Rx mode, Low gain state, Per channel		60	75	mA
LNA Shutdown Current	Per channel		6		mA
LNA and Switch Control Voltage (Pins 4,8,21,27,29,35)	V_{low}	0		+0.63	V
	V_{high}	+1.17		V_{DD}	V
Switch Current	Tx mode		<0.5		mA
Switch switching time	ANT-TX rise time		890		ns
	ANT-TX fall time		780		ns
	ANT-RX rise time		980		ns
	ANT-RX fall time		610		ns
Thermal Resistance	Tx Mode			22.7	°C/W
	Rx High Gain Mode			23	°C/W

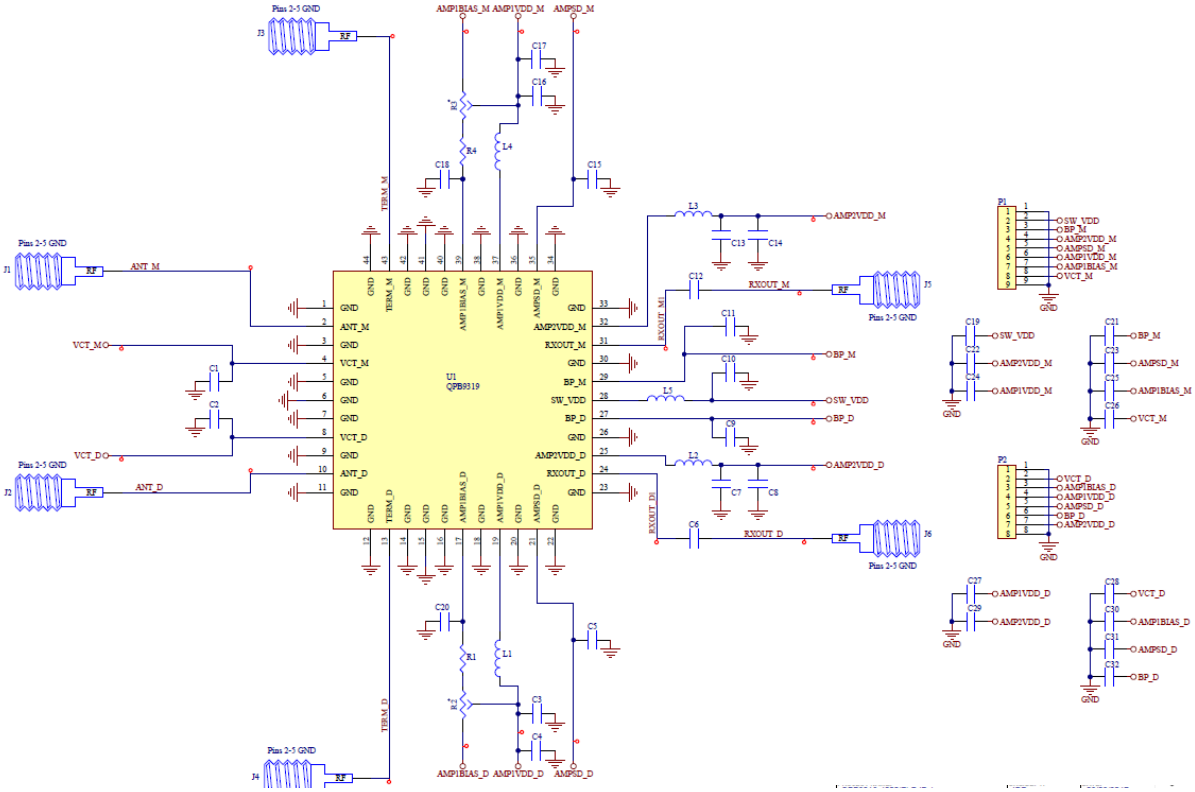
Notes:

1. Test conditions unless otherwise noted: Temp = +25 °C, 50 Ω system.
2. Trace loss de-embedded.

Control bits settings for Switch state and Rx path gain mode.

	VCT (switch control) Pins 4 & 8 (J7 & J8 on EVB)	AMPSD Pins 21 & 35 (J14 & J11 on EVB)	BP Pins 27 & 29 (J16 & J18)
RX mode (high gain state)	0	0	0
RX mode (low gain state)	0	0	1
TX mode	1	1	0

Evaluation Board Schematic

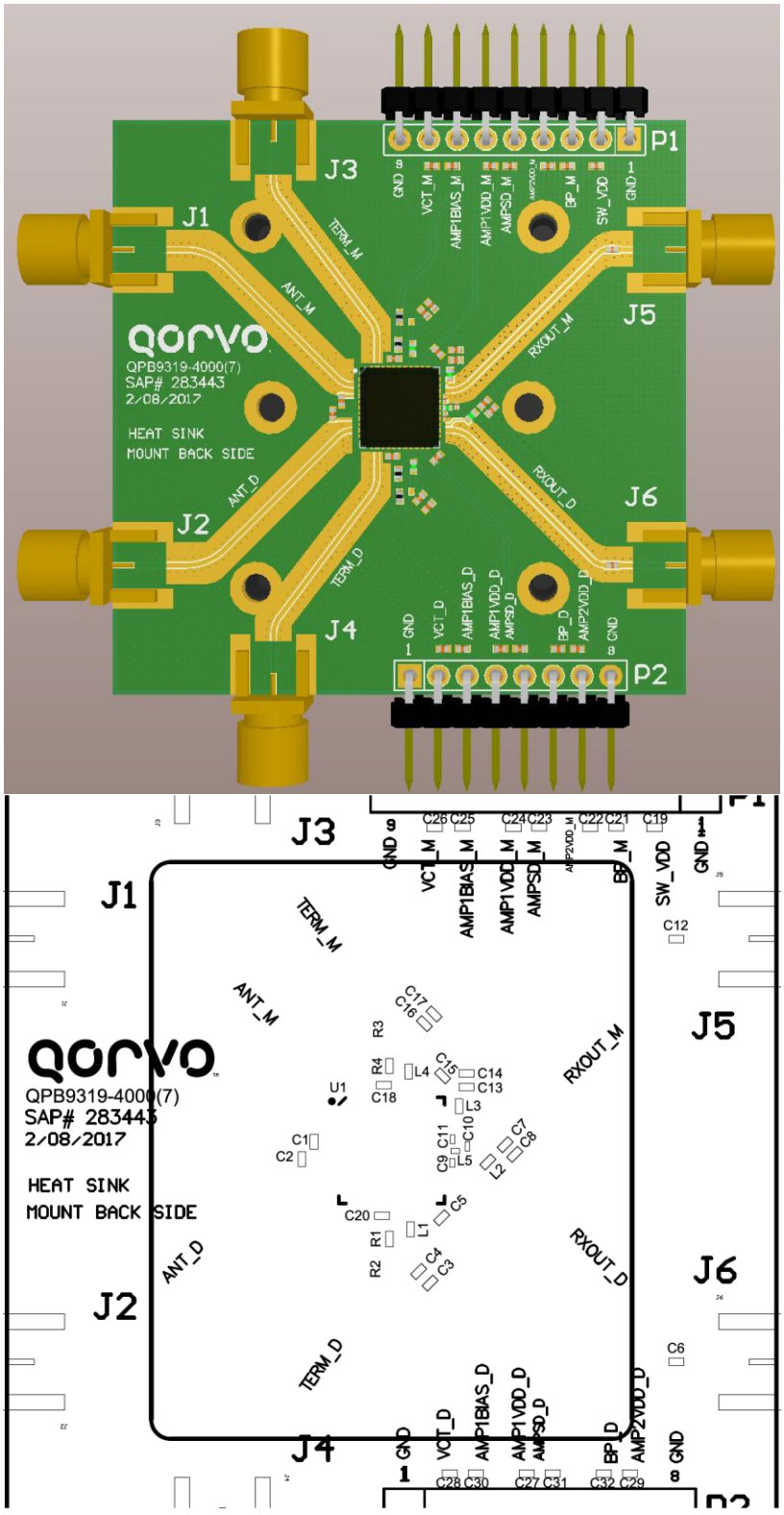


Bill of Material – Evaluation Board

Reference Des.	Value	Description	Manuf.	Part Number
U1	N/A	Dual-Channel Switch-LNA Module	Qorvo	QPB9319
PCB	n/a	PCB, QPB9319		
C6,C12	100 pF	CAP, 5%, 50V, C0G, 0402	MURATA	GRM1555C1H101JA01D
C22,C24,C27,C29	0.1 uF	CAP, 10%, 10V, X7R, 0402	TAIYO	LMK105B7104KV-F
C9,C11	1000 pF	CAP, 10%, 16V, X7R, 0201	AVX	0201YC102KAT2A
C1,C2,C4,C5,C7,C13,C15,C16,C18,C20,C21,C32	1000 pF	CAP, 10%, 25V, STD, 0402	TDK	C1005X7R1E102K
C3,C8,C14,C17	1 uF	CAP, 10%, 6.3V, X7R, 0402	MURATA	GRM155R70J105KA12D
C10	0.01 uF	CAP, 10%, 6.3V, X7R, 0201	MURATA	GRM033R70J103KA01D
R2,R3	0 Ω	RES, 5%, 1/10W, 0402	Kamaya	RMC1/16SJPTH
R1,R4	5.1K Ω	RES, 5%, 1/16W, 0402	KOA Speer	RK73B1ETTP512J
L2,L3	10 nH	IND, 3%, W/W, 0402	MURATA	LQW15AN10NH00D
L1,L4	4.7 nH	IND, +/-0.1nH, W/W, 0402	MURATA	LQW15AN4N7B00D
L5	5.6 nH	IND, 3%, T/F, 0201	MURATA	LQP03TG5N6H02D

Note:
1. Heatsink is recommended on the board when operating at high power levels when in Tx mode.

Evaluation Board Layout



Typical Performance

Test conditions unless otherwise noted: V_{DD}=+5 V, Temp=+25°C

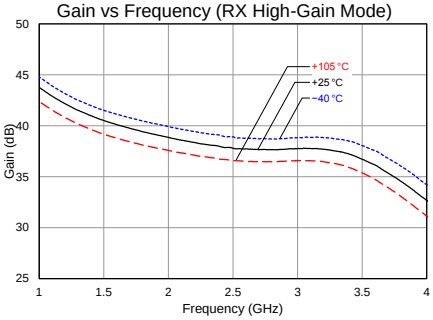
Parameter	Conditions	Typical Values			Units
Frequency		1800	2700	3800	MHz
Gain	ANT-Rx Path, High Gain Mode	39.4	37.7	34.5	dB
Input Return Loss	ANT-Rx Path, High Gain Mode	15.5	12	11.5	dB
Output Return Loss	ANT-Rx Path, High Gain Mode	12.5	6.7	11.3	dB
Gain	ANT-Rx Path, Low Gain Mode	18.7	19.1	17.9	dB
Input Return Loss	ANT-Rx Path, Low Gain Mode	14	14	12.6	dB
Output Return Loss	ANT-Rx Path, Low Gain Mode	21	10.5	15	dB
Insertion Loss	ANT-Tx Path	0.6	0.72	0.72	dB
Output P1dB	ANT-Rx Path, High Gain Mode	+20.7	+19.5	+19	dBm
Output P1dB	ANT-Rx Path, Low Gain Mode	+19	+15.2	+15.8	dBm
OIP3	Pout=+3 dBm/tone, Δf=1 MHz (ANT-Rx Path, High Gain Mode)	+34.5	+33.7	+35	dBm
OIP3	Pout=+3 dBm/tone, Δf=1 MHz (ANT-Rx Path, Low Gain Mode)	+34.5	+31.2	+34.5	dBm
Noise figure (1)	ANT-Rx Path	1.3	1.45	1.6	dB
Isolation	Ant-RX	62	68	62	dB
	Ant-TX	39	31	33	dB
	RX-RX	47	52	50	dB
	TX-TX	67	68	66	dB

Note: 1) Noise figure data has input trace loss de-embedded.

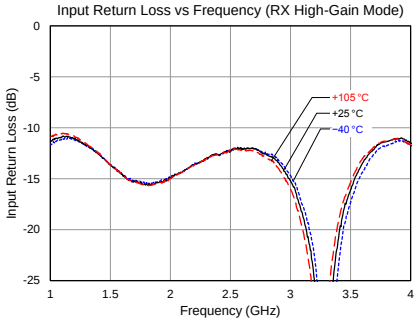
Performance Plots

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp.= +25 °C

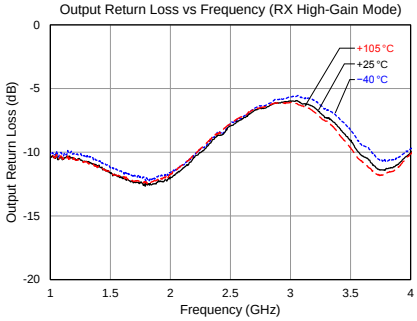
Gain vs Frequency (RX High-Gain Mode)



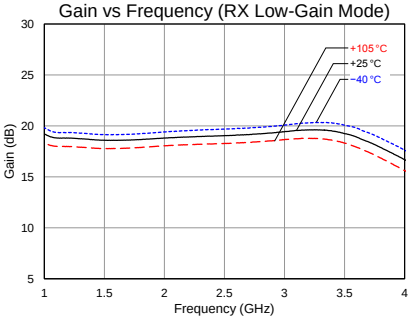
Input Return Loss vs Frequency (RX High-Gain Mode)



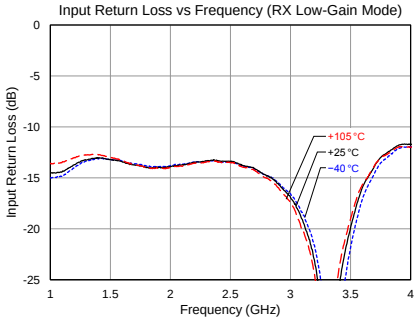
Output Return Loss vs Frequency (RX High-Gain Mode)



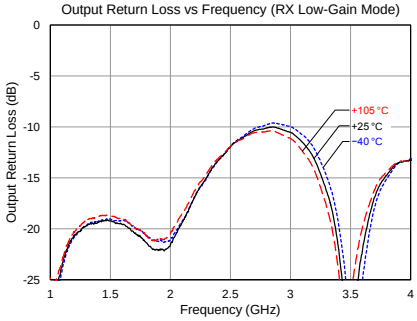
Gain vs Frequency (RX Low-Gain Mode)



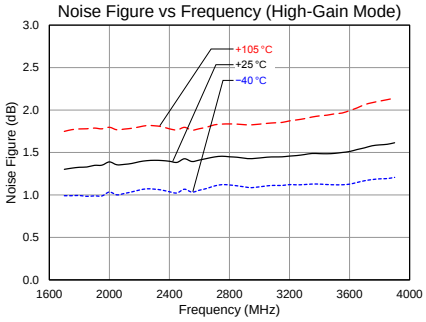
Input Return Loss vs Frequency (RX Low-Gain Mode)



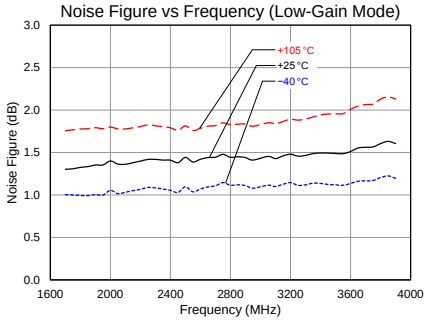
Output Return Loss vs Frequency (RX Low-Gain Mode)



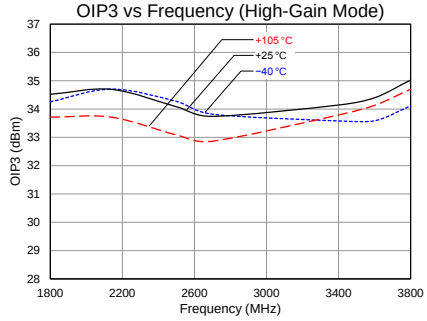
Noise Figure vs Frequency (High-Gain Mode)



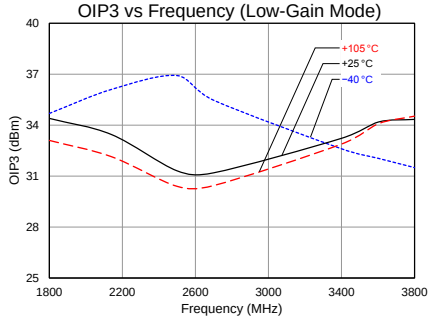
Noise Figure vs Frequency (Low-Gain Mode)



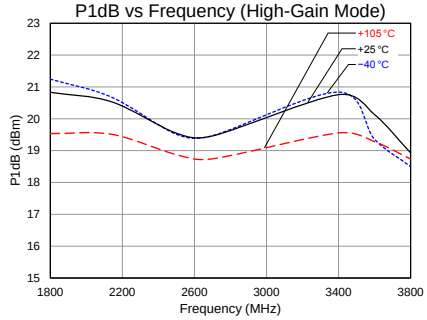
OIP3 vs Frequency (High-Gain Mode)



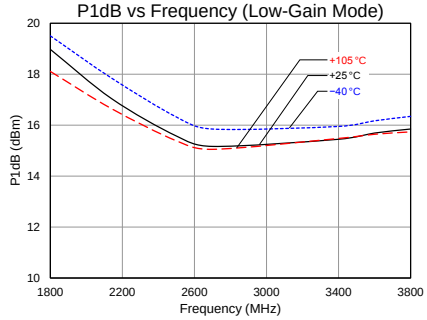
OIP3 vs Frequency (Low-Gain Mode)



P1dB vs Frequency (High-Gain Mode)



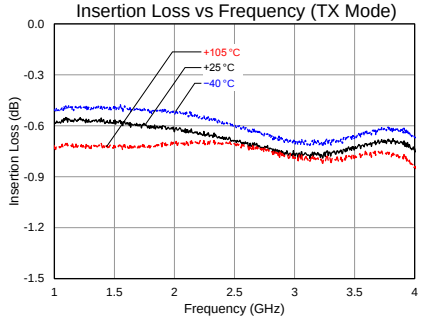
P1dB vs Frequency (Low-Gain Mode)



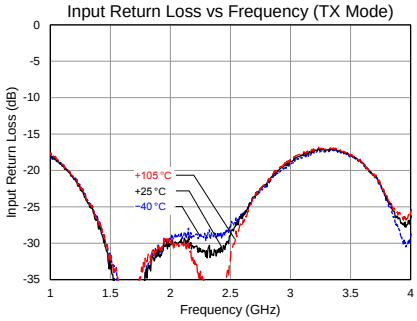
Performance Plots Contd.

Test conditions unless otherwise noted: V_{DD} = +5 V, Temp.= +25 °C

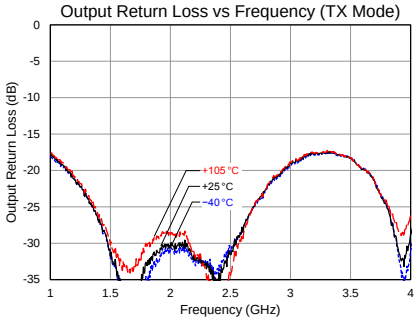
Insertion Loss vs Frequency (TX Mode)



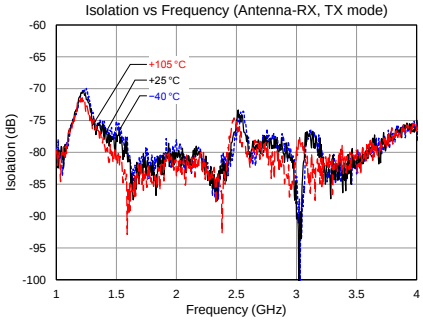
Input Return Loss vs Frequency (TX Mode)



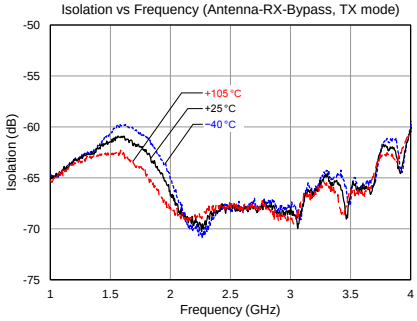
Output Return Loss vs Frequency (TX Mode)



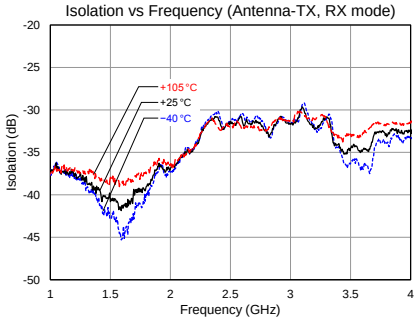
Isolation vs Frequency (Antenna-RX, TX mode)



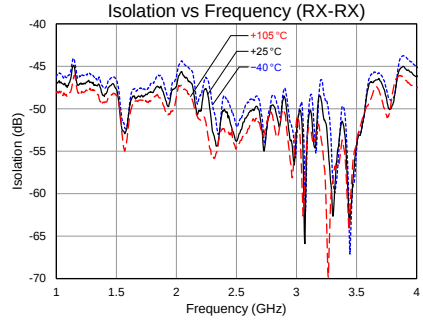
Isolation vs Frequency (Antenna-RX-Bypass, TX mode)



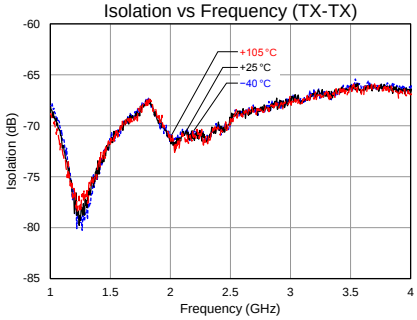
Isolation vs Frequency (Antenna-TX, RX mode)



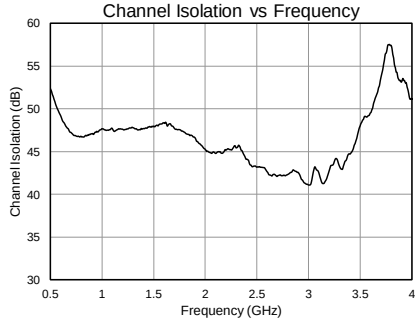
Isolation vs Frequency (RX-RX)



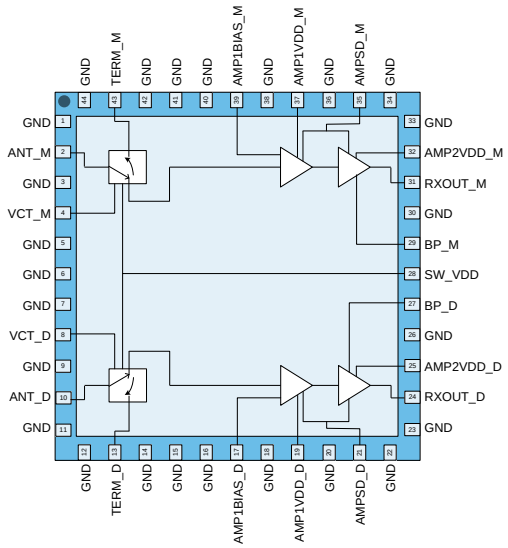
Isolation vs Frequency (TX-TX)



Channel Isolation vs Frequency



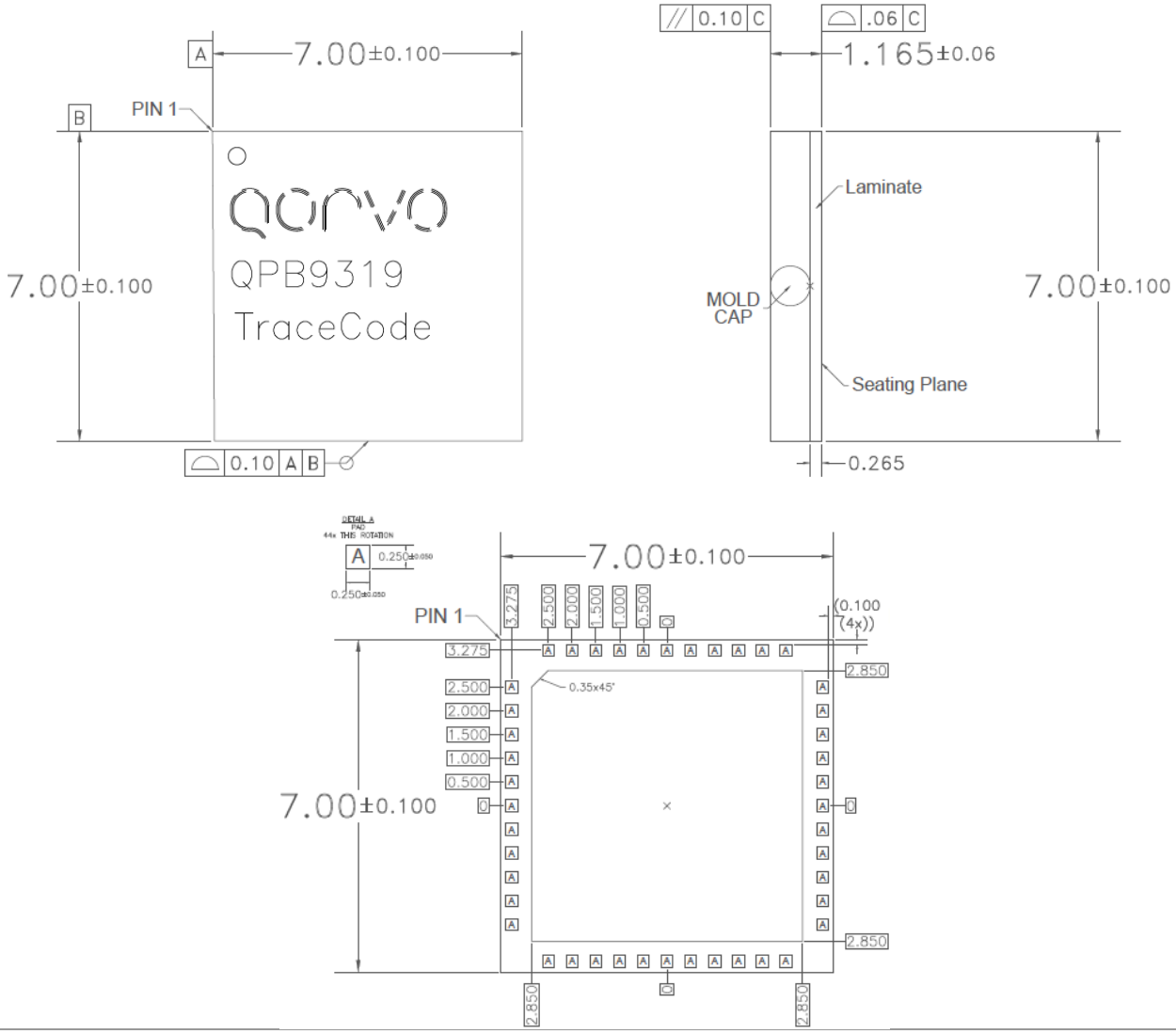
Pin Configuration and Description



Top View

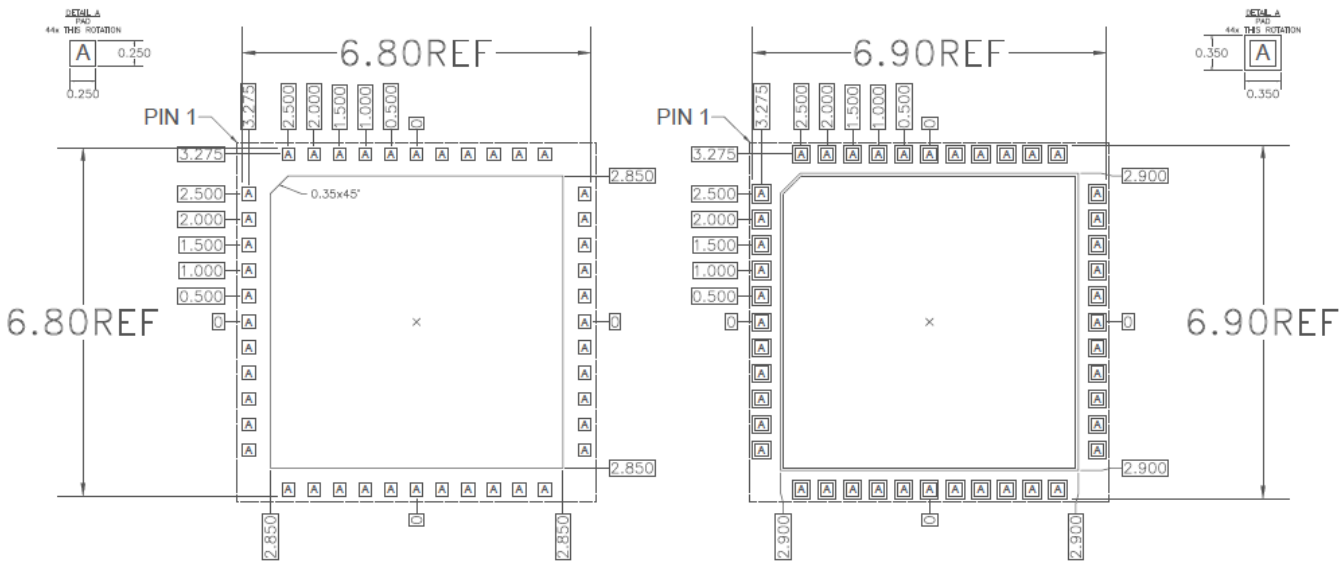
Pin No.	Label	Description
1, 3, 5, 6, 7, 9, 11, 12, 14, 15, 16, 18, 20, 22, 23, 26, 30, 33, 34, 36, 38, 40, 41, 42, 44	GND	RF/DC ground connection. Recommended to be grounded on PCB to help with isolation and good mounting integrity.
2	ANT_M	Main channel Antenna port of switch.
4	VCT_M	Main channel switch control voltage.
8	VCT_D	Diversity channel switch control voltage.
10	ANT_D	Diversity channel Antenna port of switch.
13	TERM_D	Diversity channel TX or termination port of switch. Switch set to ANT-TERM path can handle 5W average power provided there is a good 50 Ohm load.
17	AMP1BIAS_D	Diversity channel RX path first LNA bias control pin. External series resistor at this pin tied to VDD sets the bias point. Value of resistor can be varied to change current draw.
19	AMP1VDD_D	Diversity channel RX path first LNA supply voltage pin. External choke and bypass caps needed.
21	AMPSD_D	Diversity channel RX path control voltage to turn OFF both AMPs.
24	RXOUT_D	Diversity channel RX path RF output port. External DC block needed.
25	AMP2VDD_D	Diversity channel RX path second LNA supply voltage. External choke and bypass caps needed.
27	BP_D	Diversity channel RX path control voltage to switch second AMP to bypass mode.
28	SW_VDD	Switch DC supply voltage for both channels. External bypass caps recommended.
29	BP_M	Main channel RX path control voltage to switch second AMP to bypass mode.
31	RXOUT_M	Main channel RX path RF output port. External DC block needed.
32	AMP2VDD_M	Main channel RX path second LNA supply voltage. External choke and bypass caps needed.
35	AMPSD_M	Main channel RX path control voltage to turn OFF both AMPs.
37	AMP1VDD_M	Main channel RX path first LNA supply voltage pin. External choke and bypass caps needed.
39	AMP1BIAS_M	Main channel RX path first LNA bias control pin. External series resistor at this pin tied to VDD sets the bias point. Value of resistor can be varied to change current draw.
43	TERM_M	Main channel TX or termination port of switch. Switch set to ANT-TERM path can handle 5W average power provided there is a good 50 Ohm load.
Backside Pad	GND	Ground connection. PCB vias under the device are required. Refer ‘PCB Mounting Pattern’ on pg. 7.

Package Marking and Dimensions



Notes:
1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

PCB Mounting Pattern



Notes:

1. A heat sink underneath the area of the PCB for the mounted device is recommended for proper thermal operation.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU. This product also has the following attributes:

- Product uses RoHS Exemption 7c-I to meet RoHS Compliance requirements.
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

For technical questions and application information: **Email:** appsupport@qorvo.com

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