

*ASSP*

# 3-Channel 8-Bit D/A Converter

## MB40958

### ■ DESCRIPTION

The MB40958 is an 8-bit resolution high-speed digital-to-analog converter, designed for video processing applications.

The MB40958 has 8-bit resolution 3 channel D/A converters. Digital signals are input to the 8-bit digital input ports, and the input digital data are converted to the analog signals in minimum 60 Mega sample per seconds (MSPS). The analog output voltage is provided in a range of DC +3V to +5V (2Vp-p level) .

The MB40958 is fabricated by the Fujitsu's advanced bipolar process and housed in a 48-pin plastic QFP.

The MB40958 is designed for video signal processing applications, and it is suitable for TVs and VCRs.

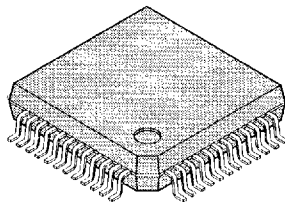
### ■ FEATURES

- 8-bit x 3 channels D/A converters
- Max. 60 MHz input clock frequency providing 60 MSPS data conversion rate
- Linearity error : Max. +/-0.2%
- Analog input voltage range : 3V to 5V (2Vp-p level)
- Digital input voltage level : TTL level

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### ■ PACKAGE

48 pin, Plastic QFP



(FPT-48P-M15)

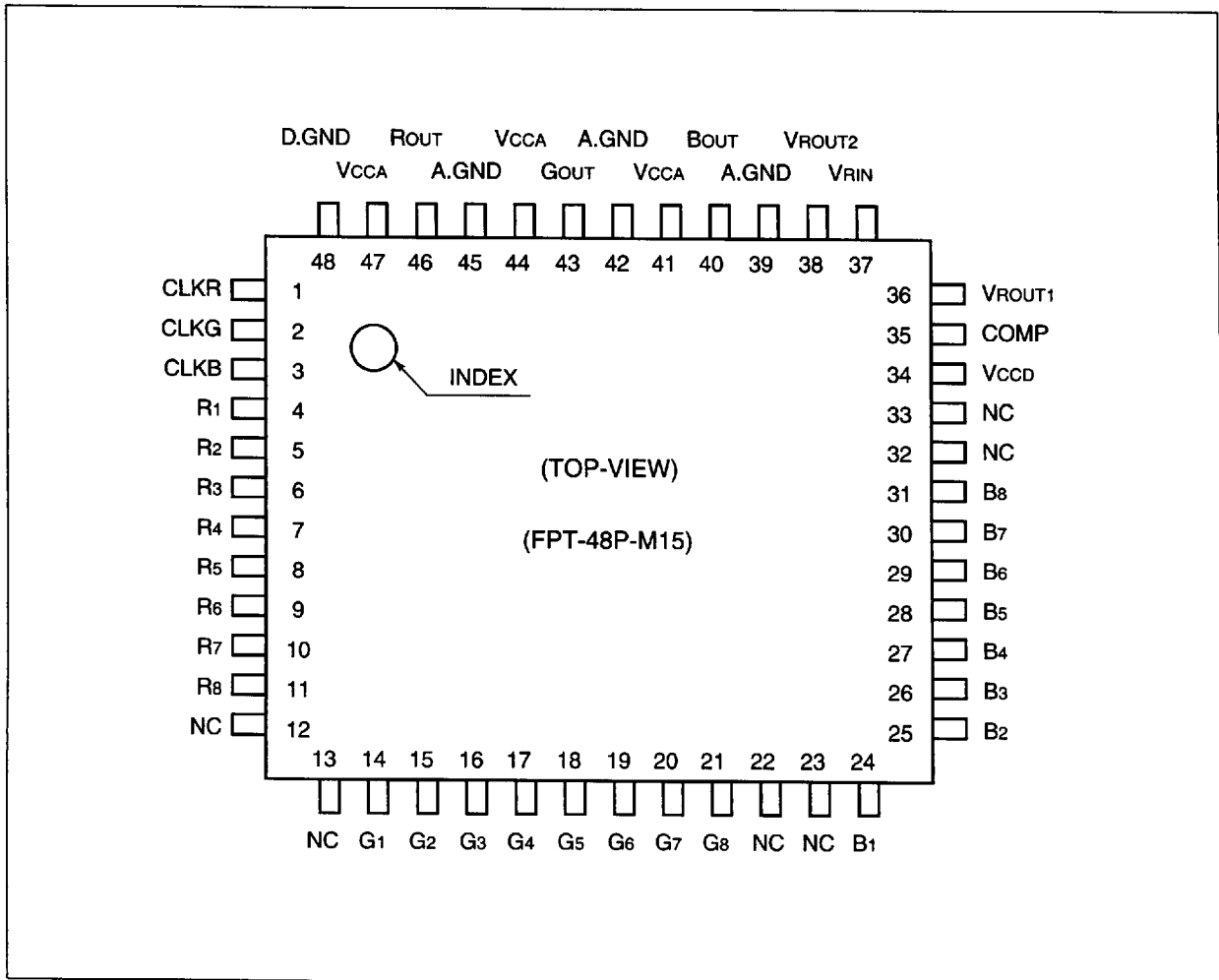
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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- On-chip reference voltage outputs :
  - Output by resistor divided ( $0.6 \times V_{CCA}$ )
  - Output by band gap reference ( $V_{CCA} - 2[V]$ )
- Low power consumption :   Typical 400mW at 2Vp-p analog output voltage  
                                   Typical 300mW at 1Vp-p analog output voltage
- Single +5V power supply
- Operating temperature range :  $-20^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$
- Fujitsu's advanced bipolar process
- Package : 48-pin plastic QFP (Suffix : -PF)

## ■ PIN ASSIGNMENT



## ■ PIN DESCRIPTION

Symbol	Pin No.	Type	Name & Function
<b>Power Supply</b>			
VCCD	34	—	+5V DC power supply pins for digital block.
D. GND	48	—	Ground pin for digital block.
VCCA	41, 44, 47	—	DC power supply pins for analog block.
A. GND	39, 42, 45	—	Ground pins for analog block.
<b>Clock</b>			
CLKR	1	I	Clock input pin for R channel.
CLKG	2	I	Clock input pin for G channel.
CLKB	3	I	Clock input pin for B channel.
<b>Digital Input</b>			
R1 R2 R3 R4 R5 R6 R7 R8	4 5 6 7 8 9 10 11	I	Digital data input pins for R channel. 8-bit data is input to the pins. The R1 pin is the MSB and the R8 pin is the LSB.
G1 G2 G3 G4 G5 G6 G7 G8	14 15 16 17 18 19 20 21	I	Digital data input pins for G channel. 8-bit data is input to the pins. The G1 pin is the MSB and the G8 pin is the LSB.
B1 B2 B3 B4 B5 B6 B7 B8	24 25 26 27 28 29 30 31	I	Digital data input pins for B channel. 8-bit data is input to the pins. The B1 pin is the MSB and the B8 pin is the LSB.

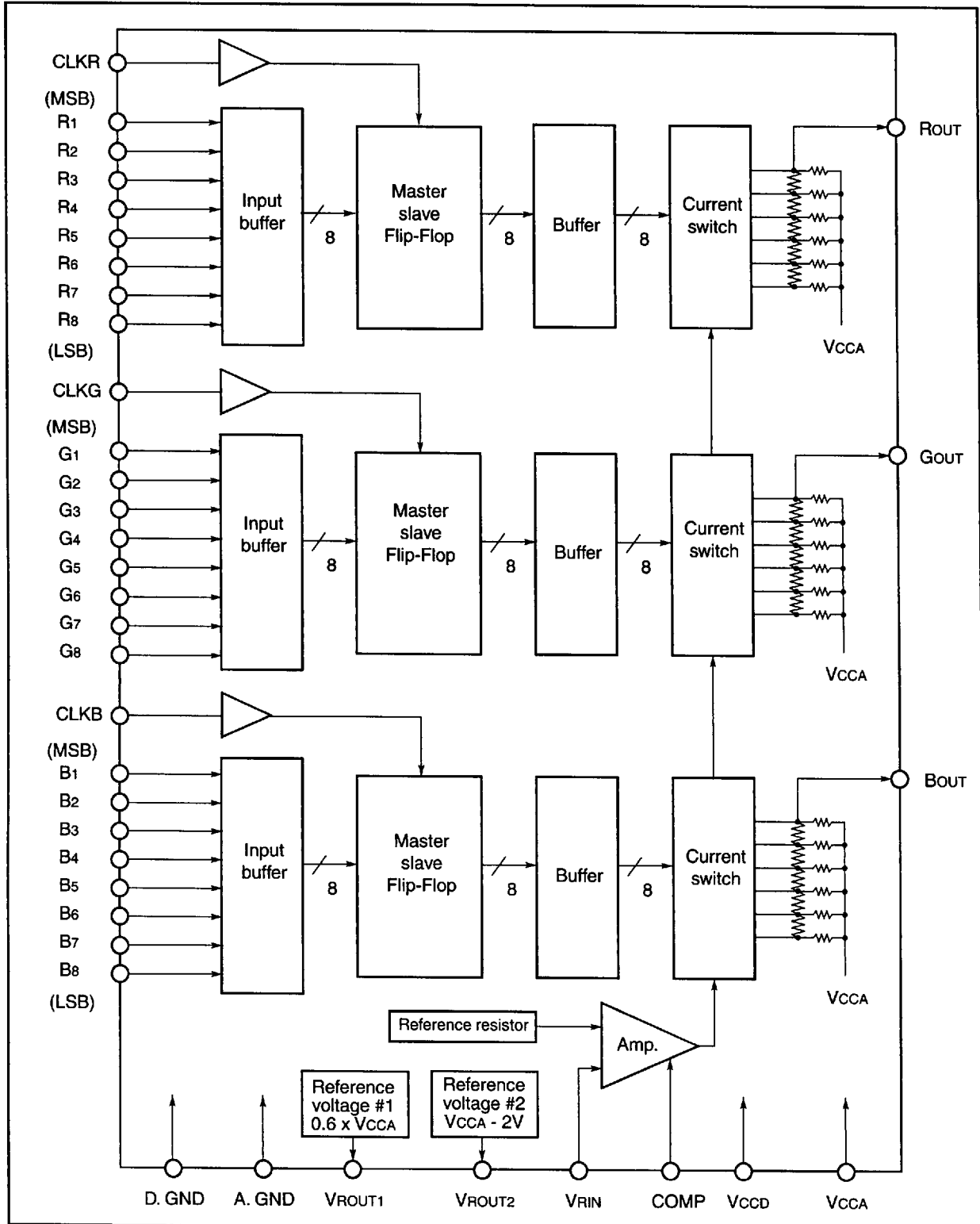
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Symbol	Pin No.	Type	Name & Function
<b>Analog Output</b>			
ROUT	46	O	Analog signal output pin for R channel.
GOUT	43	O	Analog signal output pin for G channel.
BOUT	40	O	Analog signal output pin for B channel.
<b>Reference Voltage</b>			
VRIN	37	I	Reference voltage input pin. This pin is used to set the analog output dynamic range. When the internal reference voltage is used, this pin is connected with VROUT1 pin (36 pin) or VROUT2 pin (38 pin). When the reference voltage is supplied from the external generator, 2.65V to 4.3V or $V_{CCA} - VRIN = 0.7V$ to 2.2V is input to this pin.
VROUT1	36	O	Reference voltage output #1 pin. The output voltage is set to $0.6 \times V_{CCA}$ by the resistor divided method. When this pin is connected with VRIN pin (37 pin), an analog voltage is output from this pin in a range of $0.6 \times V_{CCA}$ to $V_{CCA}$ .
VROUT2	38	O	Reference voltage output #2 pin. The output voltage is set to $V_{CCA} - 2V$ by the band-gap reference method. When this pin is connected with VRIN pin (37 pin), an analog voltage is output from this pin in a range of $V_{CCA} - 2V$ to $V_{CCA}$ .
<b>Compesation Capacitor</b>			
COMP	35	—	Phase compesation capacitor pin. A phase compesation capacitor of $0.1\mu F$ or greater is connected between this pin and A. GND pin.
<b>No Connection</b>			
NC	12, 13, 22, 23, 32, 33	—	No connection, Leave those pins open.

## ■ BLOCK DIAGRAM



# MB40958

## ■ ABSOLUTE MAXIMUM RATINGS

(A. GND = D. GND = 0V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V <sub>CCA</sub> , V <sub>CCD</sub>	-0.5 to +7.0	V
Power supply voltage difference	V <sub>CCD</sub> - V <sub>CCA</sub>	1.5	V
Analog reference voltage	V <sub>RIN</sub>	-0.5 to V <sub>CCA</sub> +7.0	V
Digital input Voltage	V <sub>ID</sub>	-0.5 to +7.0	V
Storage temperature	T <sub>stg</sub>	-55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ■ RECOMMENDED OPERATING CONDITIONS

(A. GND = D. GND = 0V)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V <sub>CCA</sub> , V <sub>CCD</sub>	4.75	5.00	5.25	V
Power supply voltage difference	V <sub>CCA</sub> - V <sub>CCD</sub>	-0.2	—	0.2	V
Analog reference voltage	V <sub>CCA</sub> - V <sub>RIN</sub>	0.70	2.00	2.20	V
	V <sub>RIN</sub>	2.65	3.00	4.30	V
Digital "H" level input voltage	V <sub>IHD</sub>	2.0	—	—	V
Digital "L" level input voltage	V <sub>ILD</sub>	—	—	0.8	V
Clock frequency	f <sub>CLK</sub>	—	—	60	MHz
Setup time	t <sub>SU</sub>	8.0	—	—	ns
Hold time	t <sub>H</sub>	2.0	—	—	ns
Minimum clock "H" level pulse width	t <sub>WH</sub>	6.5	—	—	ns
Minimum clock "L" level pulse width	t <sub>WL</sub>	6.5	—	—	ns
Phase compensation capacitance	C <sub>COMP</sub>	0.1	—	—	μF
Operating ambient temperature	T <sub>OP</sub>	-20	—	70	°C

## ■ ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions Otherwise Noted)

### 1. DC Characteristics

Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Resolution	—	—	—	8	bit	—
Linearity error	LE	—	—	±0.2	%	DC Accuracy
Digital "H" level input current	I <sub>IHD</sub>	—	—	20	μA	V <sub>IHD</sub> = 2.7 (V)
Digital "L" level input current	I <sub>ILD</sub>	-100	—	—	μA	V <sub>ILD</sub> = 0.4 (V)
Reference input current	I <sub>RIN</sub>	—	—	10	μA	V <sub>RIN</sub> = 3.000 (V)
Reference voltage (Resister divided)	V <sub>ROUT1</sub>	2.900	3.000	3.100	V	V <sub>CCA</sub> = V <sub>CCD</sub> = 5.00 (V)
Reference voltage (BGR)	V <sub>ROUT2</sub>	V <sub>CCA</sub> -2.100	V <sub>CCA</sub> -2.000	V <sub>CCA</sub> -1.900	V	—
Reference voltage (BGR)	—	—	100	—	ppm/°C	—
RGB output voltage ratio	FSR	0	—	6	%	V <sub>CCA</sub> = V <sub>CCD</sub> = 5.00 (V)
Full-scale output voltage	V <sub>OFS</sub>	V <sub>CCA</sub> -20	V <sub>CCA</sub>	—	mV	—
Zero-scale output voltage	V <sub>OZS</sub>	2.938	3.008	3.078	V	V <sub>CCA</sub> = V <sub>CCD</sub> = 5.00 (V) V <sub>RIN</sub> = 3.000 (V)
Output resistance	R <sub>O</sub>	192	240	288	Ω	T <sub>a</sub> = 25°C
Supply current	I <sub>CC</sub>	—	80*	133	mA	V <sub>CCA</sub> = V <sub>CCD</sub> = 5.25 (V) V <sub>RIN</sub> = V <sub>ROUT1</sub>

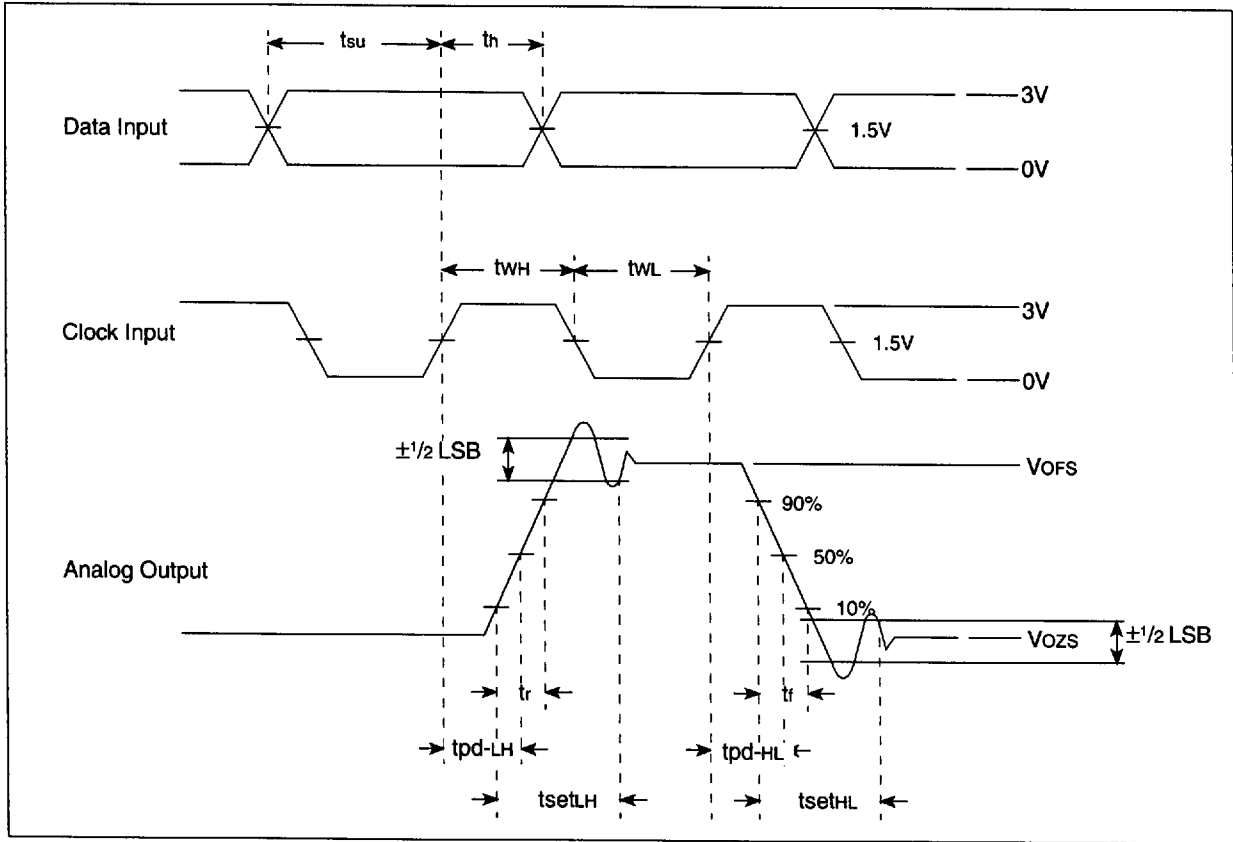
\* : V<sub>CCA</sub> = V<sub>CCD</sub> = 5.00V

### 2. AC Characteristics

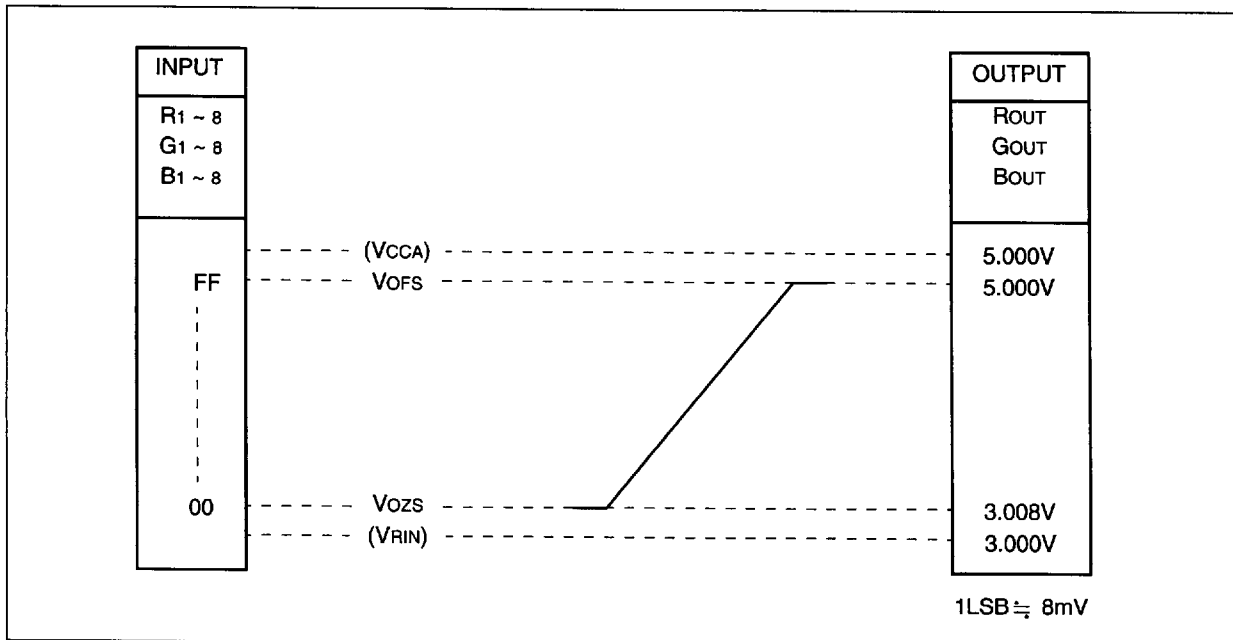
Parameter	Symbol	Value			Unit	Remark
		Min.	Typ.	Max.		
Maximum conversion rate	F <sub>s</sub>	60	—	—	MSPS	Terminated A. OUT pin with 240Ω, C <sub>L</sub> = 15pF
Output propagation delay time	t <sub>pd</sub>	—	7	—	ns	
Output rising time	t <sub>r</sub>	—	5	—	ns	
Output falling time	t <sub>f</sub>	—	5	—	ns	
Setting time	t <sub>set</sub>	—	15	—	ns	

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## ACTIMINT CHART



## DAC OUTPUT VOLTAGE RANGE



## ■ CALCULATION OF DAC OUTPUT VOLTAGE AT IDEAL CONVERSION

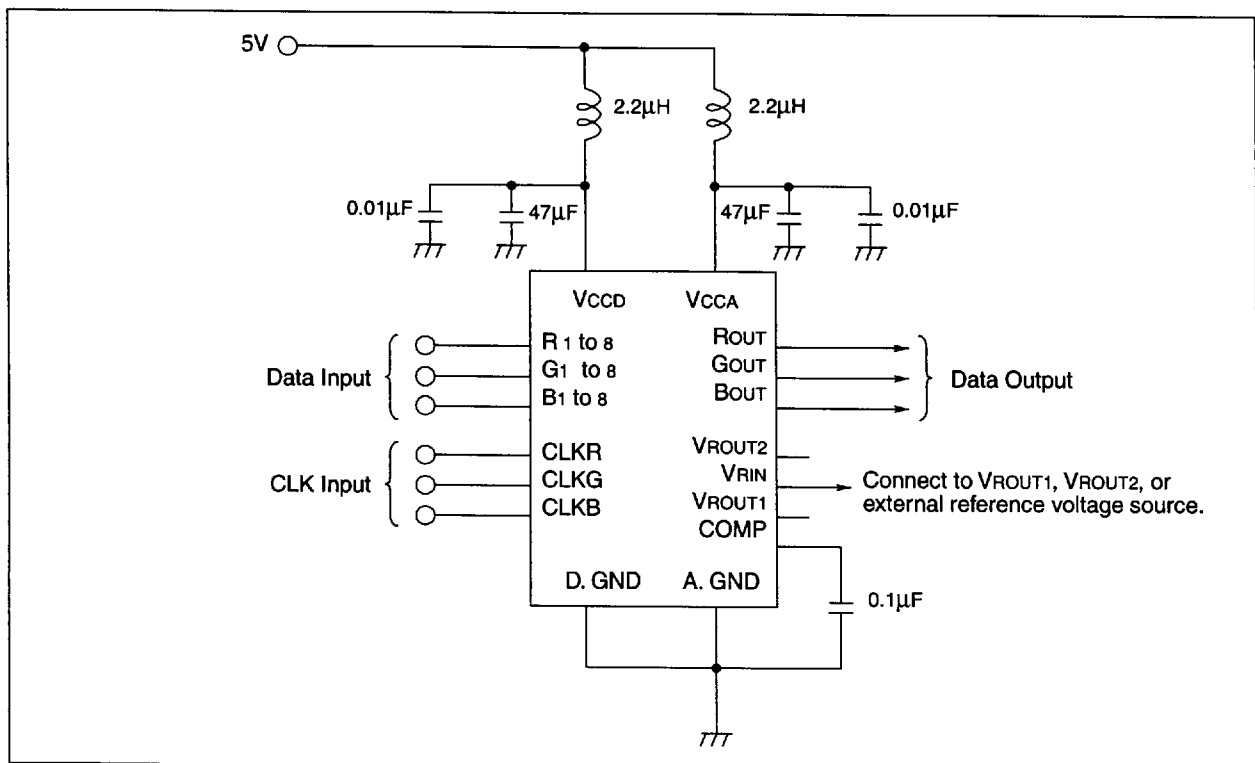
$$R_{OUT} \text{ (GOUT, BOUT)} = V_{CCA} - \frac{255 - N}{256} \times (V_{CCA} - V_{RIN})$$

[ N : Digital Input Code (0 to 255) ]

$$V_{OFS} = V_{CCA}$$

$$V_{OZS} = V_{CCA} - \frac{255}{256} \times (V_{CCA} - V_{RIN})$$

## ■ TYPICAL CONNECTION EXAMPLE



## ■ NOTES ON USE

### 1. Power Supply Patterns of the PCB

The power supply wire patterns (Vcc and GND patterns) of the PCB should be designed as wide as possible in order to reduce parasitic impedance.

### 2. Switching Noise

In order to reduce switching noise as much as possible, noise limit capacitor must be connected between Vccd and D. GND pins and VCCA and A. GND pins.

In this case, the capacitor should be connected to the GND pins side as near as possible.

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## ■ PACKAGE DIMENSION

