PW-8X010P6, PW-8X030P6, PW-8X075P6
MAGNUM MOTOR DRIVE® SERIES
75A, 30A, 10A 600V MAGNUM MOTOR DRIVES

Make sure the next Card you purchase has...

DDC® on Board

FEATURES

- 600 VDC Drive for 270 VDC Motors
- 10 Amps @25°C, 10 Amps @85°C
- 30 Amps @25°C, 30 Amps @85°C
- 75 Amps @25°C, 50 Amps @85°C
- Half-Bridge Drive
- Half-Bridge Drive with Current Sense
- Half-Bridge Drive with Regenerative Clamp
- Operates with Brushless, Brush, and Induction Motors
- Input to Output Ground Isolation with Floating Output Stage
- Short Circuit Protection
- Trapezoidal or Sinusoidal Compatible
- DSP/Microprocessor Compatible

DESCRIPTION

The PW-8X010P6, PW-8X030P6, and PW-8X075P6 series are half-bridge IGBT drive modules containing isolated switch drivers, a pair of solid-state switches, and an isolated power supply. The Magnum motor drive series are available in current ratings of 10, 30 and 75 amps. Additionally, each current rating group is available with a current sense or a regenerative clamp feature to accommodate numerous design requirements. The three modules can be used in any combination to create drives for brush, brushless DC, or AC induction motors. The current sense signal and logic inputs are compatible with DSP/microprocessors and/or FPGA/ASIC circuits used to control the motor drives. These modular drives are capable of operating from either a ±135Vdc or 270Vdc power source that is electrically isolated from the logic input signals. The modules are fault tolerant from output shorts, loss of any or all power supplies, and power supply sequencing.

APPLICATIONS

The high reliability and flexibility of these drives make them suitable for Military and Aerospace applications. Among the many applications are: actuator systems for primary and secondary flight controls on aircraft, fan and compressor motor drives for environment conditioning, pump motors for fuel and hydraulic fluid, antenna and radar positioning, and thrust vector position control of missiles, drones, and RPV's.

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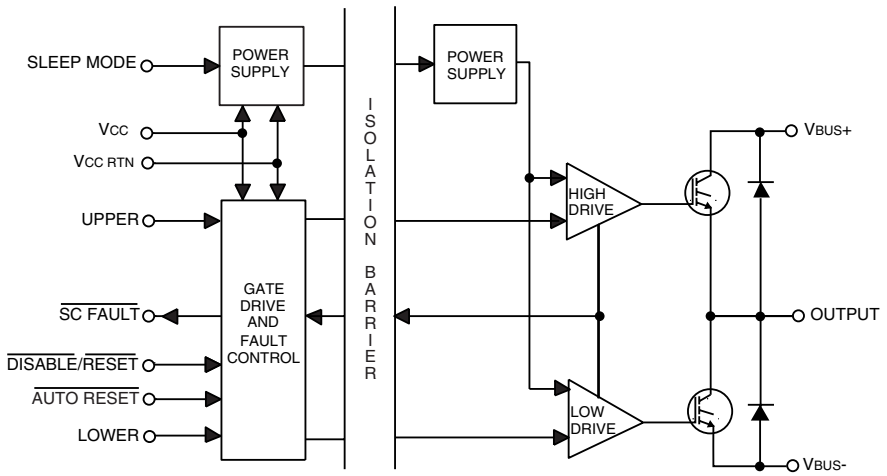


FIGURE 1A. PW-83010P6/83030P6/83075P6 BLOCK DIAGRAM

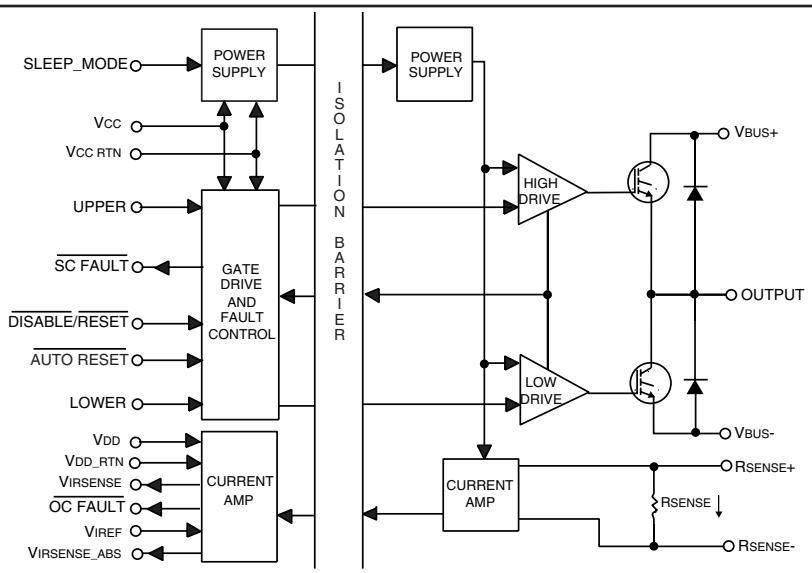


FIGURE 1B. PW-84010P6/84030P6/84075P6 BLOCK DIAGRAM

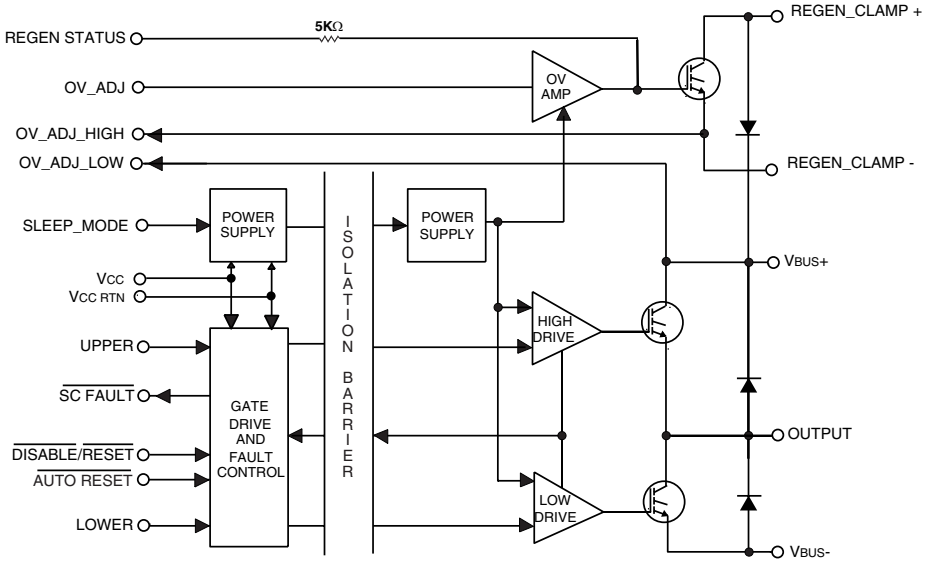


FIGURE 1C. PW-85010P6/85030P6/85075P6 BLOCK DIAGRAM

TABLE 1. PW-8X010P6/8X030P6/8X075P6 ABSOLUTE MAXIMUM RATINGS (Tc = +25°C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TYPE	VALUE			UNITS
			PW-8X010P6	PW-8X030P6	PW-8X075P6	
Drive Supply Voltage	V_{BUS+} to V_{BUS-}	All	600	600	600	VDC
Logic Supply Voltage	V_{CC}	All	5.5	5.5	5.5	VDC
Input Logic Voltage	UPPER, LOWER, $\overline{\text{DISABLE}}$/$\overline{\text{RESET}}$, SLEEP_MODE, $\overline{\text{AUTO RESET}}$	All	5.5	5.5	5.5	VDC
Current Amplifier Supply Voltage	V_{DD}	PW-84XXX	5.5	5.5	5.5	VDC
Continuous Output Current	I_C	All	75	75	75	A
Output Current Peak (10mS, T_C=85°C)	$I_{C.PEAK}$	All	110	110	110	A
$\overline{\text{SC\_FAULT}}$ Output Voltage	V_{OH}	All	5.5	5.5	5.5	VDC
$\overline{\text{SC\_FAULT}}$ Output Current	I_{OH}	All	8	8	8	mA
R_{SENSE} Continuous Current	I_{RSENSE}	PW-84XXX	30	54	100	A
R_{SENSE} Peak Current (10mS, T_C=85°C)	$I_{RSENSE.PEAK}$	PW-84XXX	36	120	220	A
$V_{IRSENSE}$ Output Voltage	$V_{IRSENSE}$	PW-84XXX	5.5	5.5	5.5	VDC
$V_{IRSENSE\_ABS}$ Output Voltage	$V_{IRSENSE\_ABS}$	PW-84XXX	5.5	5.5	5.5	VDC
$V_{IRSENSE}$ Output Current	$I_{IRSENSE}$	PW-84XXX	20	20	20	mA
$V_{IRSENSE\_ABS}$ Output Current	$I_{IRSENSE\_ABS}$	PW-84XXX	20	20	20	mA
$\overline{\text{OC\_FAULT}}$ Output Voltage	V_{OH}	PW-84XXX	5.5	5.5	5.5	VDC
$\overline{\text{OC\_FAULT}}$ Output Current	I_{OH}	PW-84XXX	20	20	20	mA
Reference Input Voltage	V_{REF}	PW-84XXX	5.5	5.5	5.5	VDC
Overvoltage Transistor Collector-Emitter Voltage	V_{CE}	PW-85XXX	600	600	600	VDC
Overvoltage Transistor Continuous Current	I_C	PW-85XXX	40	40	40	A
Overvoltage Transistor Peak Current (10mS, T_C=85°C)	$I_{C.PEAK}$	PW-85XXX	85	85	85	A
Overvoltage Flyback Diode Continuous Current	I_D	PW-85XXX	5	5	5	A
Overvoltage Flyback Diode Peak Current (10mS, T_C=85°C)	$I_{D.PEAK}$	PW-85XXX	100	100	100	A
REGEN_STATUS Output Current	V_{OH}	PW-85XXX	10	10	10	mA
Intermittent Case Operating Temperature Range	$T_{C.I}$	All	-55 to +125	-55 to +125	-55 to +125	°C
Continuous Case Operating Temperature Range	T_C	All	-55 to +100	-55 to +100	-55 to +100	°C
Storage Temperature Range	T_{CS}	All	-65 to +150	-65 to +150	-65 to +150	°C
Junction Temperature, Power Devices	$T_{J.POWER}$	All	+150	+150	+150	°C
Junction Temperature, Other Components	$T_{J.OTHER}$	All	+135	+135	+135	°C
Isolation Voltage (Note 1)	V_{ISO}	All	2500	2500	2500	VDC

Note 1: From V_{CC-RTN} to V_{BUS+}, V_{BUS-}, OUTPUT, REGEN_CLAMP+, R_{SENSE+}, R_{SENSE-}.

TABLE 2. PW-8X010P6/8X030P6/8X075P6 GENERAL SPECIFICATIONS COMMON TO ALL TYPES
(Tc = -55°C TO 100°C FOR MIN, MAX VALUES, Tc = 25°C FOR TYPICAL VALUES UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	PW-8X010P6			PW-8X030P6			PW-8X075P6			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT STAGE												
Drive Supply Voltage	V_{BUS+} to V_{BUS-}	Unipolar/Bipolar		270	600		270	600		270	600	VDC
Transistors												
Continuous Output Current capability	I_{C25}	25°C case	10			30			75			A
	I_{C85}	85°C case	10			30			50			A
Peak Current	$I_{C.PEAK}$	85°C case,<10mS	110			110			110			A
Short Circuit Trip Current	I_{SC}	Note 1	200	350		200	350		200	350		A
Saturation Voltage	$V_{CE(SAT)}$	Ic = I_{C85}		1.5	2		1.8	2.2		2.2	2.6	VDC
Turn-On Energy Per Pulse	E_{ON}	V_{CE} = 270, Ic = I_{C85}, Tj = 125°C		0.3			0.9			1.5		mJ
Turn-Off Energy Per Pulse	E_{OFF}	V_{CE} = 270, Ic = I_{C85}, Tj = 125°C		0.6			1.6			2.7		mJ
Flyback Diode												
Forward Voltage	V_F	Ic = I_{C85}		1.4	1.8		1.6	2		1.7	2.1	VDC
Reverse Leakage	I_R	85°C case			6			6			6	mA
Reverse Recovery Peak Current	Irr (FIGURE 2B)	I_F=I_{C85} and 85°C case di/dt=480A/µs		15			17			19		A
Reverse Recovery Time	trr (FIGURE 2B)	I_F=I_{C85} and 85°C case di/dt=480A/µs		130			150			175		nS
OUTPUT SWITCHING CHARACTERISTICS												
Turn-On Propagation Delay	$t_{d(on)}$ (FIGURE 2H)		150		650	150		650	150		650	nS
Turn-Off Propagation Delay	$t_{d(off)}$ (FIGURE 2H)		640		1700	640		1700	640		1700	nS
DISABLE/RESET Delay to Enabled	$t_{d(on)}$ (FIGURE 2C)	Open Collector Source		27			27			27		µS
DISABLE/RESET Delay to Disabled	t_{dd}(off)			850	1700		850	1700		850	1700	nS
Turn-On Rise Time	t_r (FIGURE 2H)		100		200	100		200	100		200	nS
Turn-Off Fall Time	t_f (FIGURE 2H)		140		200	140		200	140		200	nS
Sleep_Mode Delay (from sleep)	$t_{dsleep(on)}$ (FIGURE 2D)			2			2			2		mS
Sleep_Mode Delay (to sleep)	$t_{dsleep(off)}$ (FIGURE 2D)			3.7			3.7			3.7		mS
Output Switching Frequency	f_{PWM} (FIGURE 2A)	Note 2	0			0			0			kHz
Upper-Lower Deadtime Requirement	t_{DEAD} (FIGURE 2A)		2			2			2			µS
AUTO RESET Delay to Output Off	$t_{doff.auto}$			202			202			202		mS
AUTO RESET Delay to Output On	$t_{don.auto}$ (FIGURE 2F)	Open Collector Source		3			3			3		mS
RESET Pulsewidth to Clear SC FAULT	$t_{pw.reset}$ (FIGURE 2G)		200			200			200			nS
AUTO RESET Retry Cycle Time	$t_{cycle.auto}$ (FIGURE 2E)	AUTO RESET tied to SC FAULT	40	100		40	100		40	100		mS
CONTROL INPUTS												
AUTO RESET, DISABLE/RESET, UPPER, LOWER		Vcc=4.5V										
High Level Input Voltage	V_{IH}		2.45		3.50	2.45		3.50	2.45		3.50	VDC
Low Level Input Voltage	V_{IL}		1.00		2.28	1.00		2.28	1.00		2.28	VDC
Hysteresis Voltage	V_{HYST}		0.44		2.50	0.44		2.50	0.44		2.50	VDC
UPPER, LOWER												
High Level Input Current	I_{IH}	V_{IH}=V_{CC}			25			25			25	µA
Low Level Input Current	I_{IL}	V_{IL}=0V	-1000	0.1	1000	-1000	0.1	1000	-1000	0.1	1000	nA

Note 1: V_{BUS+} to V_{BUS-} must be > 10V (during short circuit for short circuit protection to operate).
Note 2: Maximum Output Switching Frequency limited only by junction temperature.
Note 3: Tc refers to case temperature.
Note 4: N/A means 'Not Applicable'.

TABLE 2 TIMING DIAGRAMS

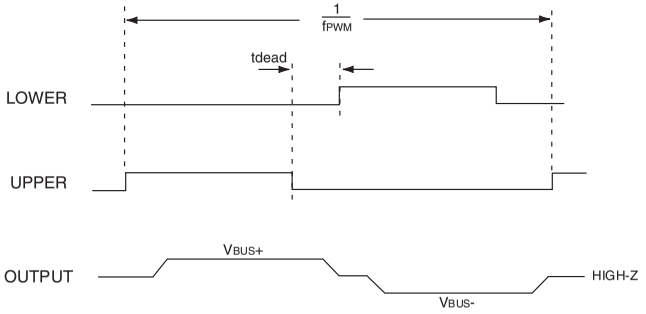


FIGURE 2A. STANDARD TIMING OPERATION

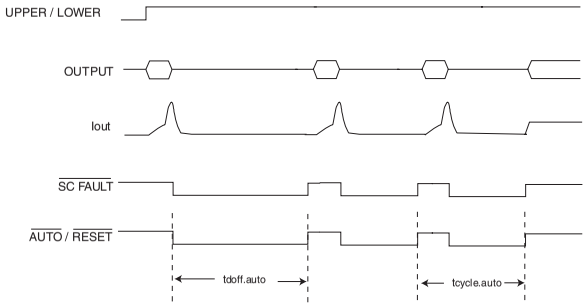


FIGURE 2E. AUTO RESET OPERATION WITH SHORT AT TURN ON THAT CLEARS

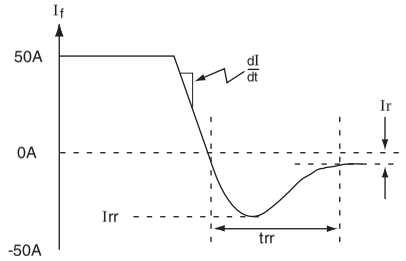


FIGURE 2B. DIODE REVERSE RECOVERY

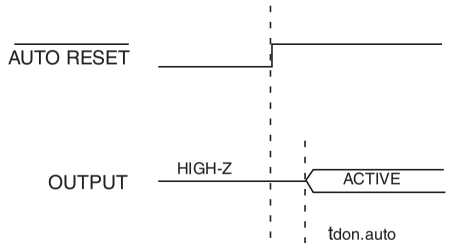


FIGURE 2F. tdon.auto TIMING

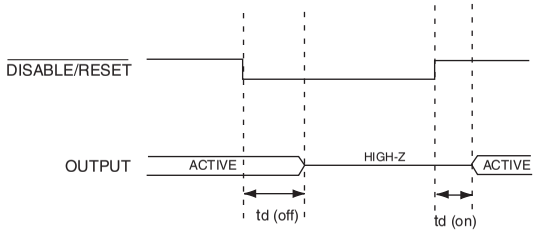


FIGURE 2C. DISABLE / RESET PROPAGATION DELAY

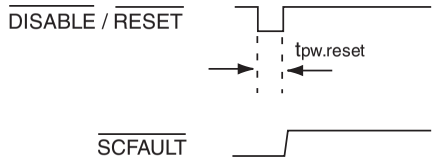


FIGURE 2G. DISABLE / RESET PULSE WIDTH

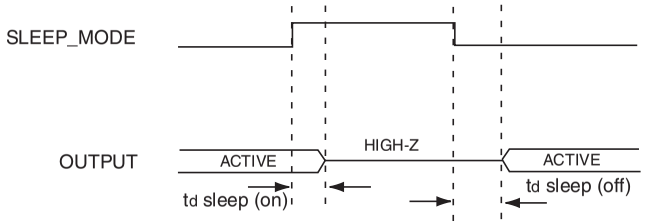


FIGURE 2D. SLEEP MODE DELAY

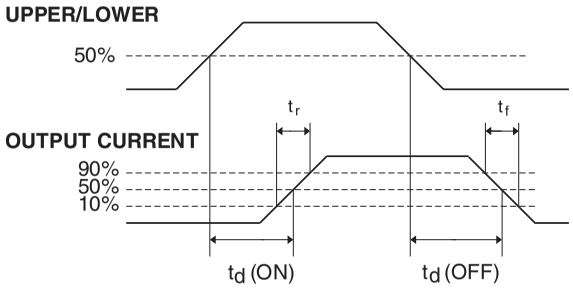


FIGURE 2H. OUTPUT TIMING

TABLE 2. (CONT) PW-8X010P6/8X030P6/8X075P6 GENERAL SPECIFICATIONS COMMON TO ALL TYPES
(Tc = -55°C TO 100°C FOR MIN, MAX VALUES, Tc = 25°C FOR TYPICAL VALUES UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	PW-8X010P6			PW-8X030P6			PW-8X075P6			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
CONTROL INPUTS (CONT)												
DISABLE/RESET												
High Level Input Current	I_{IH}	$V_{IH}=V_{CC}$	-1000	0.1	1000	-1000	0.1	1000	-1000	0.1	1000	nA
Low Level Input Current	I_{IL}	V_{IL}=0V	-25			-25			-25			µA
AUTO RESET												
High Level Input Current	I_{IH}	$V_{IH}=V_{CC}$	-1000	0.1	1000	-1000	0.1	1000	-1000	0.1	1000	nA
Low Level Input Current	I_{IL}	V_{IL}=0V	-1.6			-1.6			-1.6			mA
SLEEP_MODE												
High Level Input Voltage	V_{IH}		2.4			2.4			2.4			VDC
Low Level Input Voltage	V_{IL}				0.8			0.8			0.8	VDC
High Level Input Current	I_{IH}	$V_{IH}=V_{CC}$	-1000	0.1	1000	-1000	0.1	1000	-1000	0.1	1000	nA
Low Level Input Current	I_{IL}	V_{IL}=0V	-600			-600			-600			µA
CONTROL OUTPUTS												
SC FAULT												
High Level Output Current	I_{OH}	$V_{OH}=V_{CC}$			80			80			80	µA
Low Level Output Current	I_{OL}	V_{IL}=0.4V	5	12		5	12		5	12		mA
THERMAL												
Thermal Resistance - IGBT	θjc	Each Output Transistor		0.45	0.55		0.45	0.55		0.45	0.55	°C/W
- Diode	θjc	Each Flyback Diode		0.8	0.87		0.8	0.87		0.8	0.87	°C/W
Junction Temperature Range	Tj	Output Transistors & Diode	-55		+150	-55		+150	-55		+150	°C
		Other Components	-55		+125	-55		+125	-55		+125	°C
Case Operating Temperature Range	Tc	Continuous	-55		+100	-55		+100	-55		+100	°C
	Tc	<1% of the time	-55		+125	-55		+125	-55		+125	°C
Storage Temperature	Ts		-65		+125	-65		+125	-65		+125	°C
MECHANICAL												
Lead Soldering Temperature		10 Seconds			250			250			250	°C
Mounting Torque			3		6.5	3		6.5	3		6.5	in-lbs
Power Terminal Torque				N/A			N/A			N/A		in-lbs
D-Connector Screw Torque				N/A			N/A			N/A		in-lbs
Weight					3.1			3.1			3.1	oz
					(88)			(88)			(88)	(g)

Note 1: V_{BUS}+ to V_{BUS}- must be > 10V (during short circuit for short circuit protection to operate).
Note 2: Maximum Output Switching Frequency limited only by junction temperature.
Note 3: Tc refers to case temperature.
Note 4: N/A means 'Not Applicable'.

TABLE 3. SPECIFICATIONS FOR CURRENT SENSE FEEDBACK PW-84XXX TYPES (T_C = +25°C, V_{CC} = V_{DD} = 5.0V UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	PW-84010P6			PW-84030P6			PW-84075P6			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
VIRSENSE Gain *	GVOUT	VREF = 5.0V		218.3			67.46			19.84		mV/A
VIRSENSE Gain Error	EVOUT		-5		5	-5		5	-5		5	%
VIRSENSE Gain Drift	TCGVOUT		-330	20	330	-330	20	330	-330	20	330	ppm/°C
VIRSENSE Offset *	VOS	VREF = 5.0V	-31		31	-31		31	-31		31	mV
VIRSENSE Offset Drift *	TCVOS	VREF = 5.0V	-115		115	-115		115	-115		115	µV/°C
VIRSENSE Output Resistance	ROUT			0.2			0.2			0.2		Ω
VIRSENSE Output Current	IVOUT		1	3		1	3		1	3		mA
VIRSENSE_ABS Output Resistance	RABS			0.3			0.3			0.3		Ω
VIRSENSE_ABS Output Current	IABS		1	3		1	3		1	3		mA
VIRSENSE_ABS Gain *	GVABS			436.5			134.9			59.52		mV/A
Error_ABSVAL *	EVABS	VREF = 5.0V	-116	30	116	-116	30	116	-116	30	116	mV
VIRSENSE_ABS Gain Drift	ABSGdrift	VREF = 5.0V		±330			±330			±330		ppm/°C
VIRSENSE_ABS Offset *	VOSABS		-131		131	-131		131	-131		131	mV
VIRSENSE_ABS Offset Drift	TCVOSABS		-90		110	-90		110	-90		110	µV/°C
Sense Resistor, Resistance	RSENSE			22			6.8			2		m-Ohm
Delay Time	TDELAY (FIGURE 3A)	-55 to +100°C		9	20		9	20		9	20	µS
Bandwidth	FBW (FIGURE 3B)	-55 to +100°C	20	30		20	30		20	30		kHz
Linear Range	IRANGE	-55 to +100°C		9.1			30			100		A
$\overline{\text{OC\_FAULT}}$ Trip Level	IOC	-55 to +100°C	10.4	11.6	12.7	33.8	37.6	41.2	115	128	140	A
Trip Delay Time	tIOC (FIGURE 3C)	-55 to +100°C (10k pull up to VDD)		3	6		3	6		3	6	µS
Reference Voltage Input Current	IVREF	-55 to +100°C		0.26	1		0.26	1		0.26	1	mA
Reference Voltage Input	VREF	-55 to +100°C	4		VDD	4		VDD	4		VDD	Vdc
Reference Voltage Input Capacitance	CVREF			0.1			0.1			0.1		µF
OC_FAULT (-55 TO +100°C)												
High Level Output Current	IOH	VOH=VDD		0.2	15		0.2	15		0.2	15	µA
Low Level Output Current	IOL	VOL=0.8V	4			4			4			mA

* Note: These parameter values are proportional to VREF. Values shown are at VREF = 5V; when different VREF values are used, these values should be scaled accordingly. For example when operating at VREF = 4V, multiply each of the asterisk values by 0.8.

The VIRSENSE_ABS output is intended for use in gross overcurrent detection. For accurate current measurements VIRSENSE should be used.

The equation below shows how the specifications are used to compute overall error in VIRSENSE. (ΔT is the change in ambient temperature from 25°C).

$$V_{IRSENSE} = \left\{V_{IRSENSE.GAIN} \bullet \left(\frac{V_{REF}}{5V}\right) \bullet (1 + V_{IRSENSE.GAIN.ERROR}) \bullet (1 + V_{IRSENSE.GAIN.DRIFT} \bullet \Delta T)\right\} \bullet I_{RSENSE} + V_{IRSENSE.OFFSET} \bullet \left(\frac{V_{REF}}{5V}\right) + V_{IRSENSE.OFFSET.DRIFT} \bullet \left(\frac{V_{REF}}{5V}\right) \bullet \Delta T + \left(\frac{V_{REF}}{2}\right)$$

The equation below shows how to compare overall error in VIRSENSE.ABS. VIRSENSE.ABS is an output derived from VIRSENSE. The VIRSENSE error is composed of all VIRSENSE errors with the addition of the Error_ABSVAL.

$$V_{IRSENSE.ABS} = \left|\left\{Error_{\_ABSVAL} \bullet \left(\frac{V_{REF}}{5V}\right) + 2 \bullet \left(V_{IRSENSE} - \frac{V_{REF}}{2}\right)\right\}\right|$$

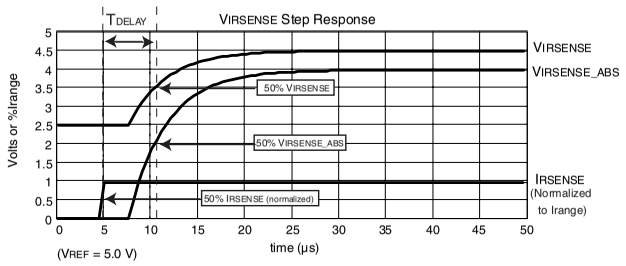


FIGURE 3A. VIRSENSE STEP RESPONSE

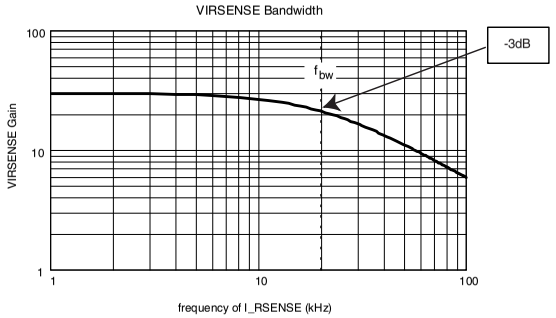


FIGURE 3B. VIRSENSE BANDWIDTH

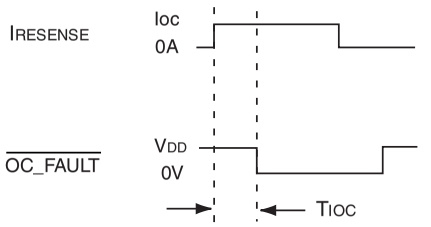


FIGURE 3C. OC FAULT TRIP RESPONSE TIME

TABLE 4. SPECIFICATIONS FOR OVERVOLTAGE PROTECTION PW-85XXX TYPES (V_{CC} = 5.0V UNLESS OTHERWISE SPECIFIED, T_C = -55°C TO +100°C FOR MIN, MAX VALUES, T_C = +25°C FOR TYPICAL VALUES UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITION	PW-85010P6			PW-85030P6			PW-85075P6			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OVERVOLTAGE PROTECTION CIRCUIT												
Transistor												
Collector-Emitter Voltage	V_{CE}				600			600			600	VDC
Continuous Current	I_{C25}	25°C case	40			40			40			A
	I_{C85}	85°C case	30			30			30			A
Peak Current	$I_{C.PEAK}$	85°C case, <10mS	85			85			85			A
Saturation Voltage	$V_{CE(SAT)}$	@ I_{C85}		2.00	3.00		2.00	3.00		2.00	3.00	VDC
Reverse Leakage	I_R	85°C case			0.4			0.4			0.4	mA
Flyback Diode												
Forward Voltage	V_F	@ I_{C85}		1.40	1.73		1.40	1.73		1.40	1.73	VDC
Reverse Leakage	I_R	85°C case			2			2			2	mA
REGEN STATUS		Referenced to V_{BUS}- or REGEN_CLAMP- Without										
Overvoltage Trip Threshold	V_{UPPER}	External Adjustment	358	400	440	358	400	440	358	400	440	VDC
Overvoltage Threshold Hysteresis	V_{HYST}		34	40	45	34	40	45	34	40	45	VDC
High Level Output Voltage	V_{OH}	No Load, V_{BUS+} > Upper Threshold	14.00	15.00	15.75	14.00	15.00	15.75	14.00	15.00	15.75	VDC
Low Level Output Voltage	V_{OL}	No Load, V_{BUS+} < Lower Threshold	0.00	0.05	0.20	0.00	0.05	0.20	0.00	0.05	0.20	VDC
Output Resistance	R_O		4.5	4.75	5.2	4.5	4.75	5.2	4.5	4.75	5.2	kΩ
V_{BUS+} Crossing Upper Threshold to Status ON Delay	$t_{don.status}$			36			36			36		nS
V_{BUS+} Crossing Lower Threshold to Status OFF Delay	$t_{doff.status}$			48			48			48		nS
VBUS+ Crossing Upper Threshold to Transistor ON Delay	$t_{don.transistor}$	@ I_{C85}		36			36			36		nS
VBUS+ Crossing Lower Threshold to Transistor OFF Delay	$t_{doff.transistor}$	@ I_{C85}		49			49			49		nS
THERMAL												
Thermal Resistance - IGBT	θ_{JC}			0.8	1.2		0.8	1.2		0.8	1.2	°C/W
- Diode	θ_{JC}			12	18		12	18		12	18	°C/W

TABLE 5. POWER SUPPLY SPECIFICATIONS FOR ALL TYPES (V_{CC} = V_{DD} = 5.0 V UNLESS OTHERWISE SPECIFIED, T_C = -55°C TO 100°C FOR MIN, MAX VALUES, T_C = 25°C FOR TYPICAL VALUES.)

PARAMETER	SYMBOL	TEST CONDITION	PW-8X010P6			PW-8X030P6			PW-8X075P6			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage for PW-83XXX Types	V_{CC}		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	VDC
Supply Current for PW-83XXX Types	I_{CC}	Note 1		110	200		110	200		110	200	mA
	$I_{CC.SLEEP}$	In SLEEP_MODE		11			11			11		mA
Supply Voltage for PW-84XXX Types	V_{CC}, V_{DD}		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	VDC
Supply Current for PW-84XXX Types	I_{CC}	Note 1		136	200		136	200		136	200	mA
	$I_{CC.SLEEP}$	In SLEEP_MODE		11			11			11		mA
Current Sense Amplifier Supply Current	I_{DD}			10	20		10	20		10	20	mA
Supply Voltage for PW-85XXX Types	V_{CC}		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	VDC
Supply Current for PW-85XXX Types	I_{CC}	Note 1		137	250		137	250		137	250	mA
	$I_{CC.SLEEP}$	In SLEEP_MODE		11			11			11		mA

Note 1: During initial power-on, a transient current of up to 100mA above I_{CC} may be observed until V_{CC} exceeds about 3.5 volts for the PW-8X010, PW-8X030 and PW-8X075.

INTRODUCTION

The PW-8X010P6, PW-8X030P6 and PW-8X075P6 Magnum families are a series of universal modular half-bridge motor drives intended for use with brush, brushless DC and AC induction motors in ground, sea and aerospace applications.

The PW-8X010P6, PW-8X030P6 and PW-8X075P6 motor drives contain an isolation barrier between the power and control stages, which attenuates ground noise generated from the high speed, high power switching. All signals from the control to the power sections are isolated from power and ground of the other section. This eliminates false triggering of the input signals and any need for creative grounding schemes. The isolation barrier also allows the user to operate the output stage from either unipolar or bipolar power supplies without level shifting the input signals. A built in power supply located in the control stage provides power to all electronics in the power stage. This eliminates the need for refresh cycles or external power supplies for the gate drive circuitry and allows switching duty cycles from 0 - 100%. (Reference FIGURES 1A, 1B, 1C)

The output power transistors on all modules are protected from a short circuit applied to the output pin. When a short circuit condition is detected, the output transistors are shut down and a flag $\overline{\text{SC FAULT}}$ is made active (logic low (L)) indicating a short has occurred. The PW-84010P6, PW-84030P6 and PW-84075P6 modules contain additional current sensing circuitry that can monitor either motor current or DC bus current. The output voltage of the current sensing circuit can be used as a feedback signal in a servo drive to create a torque loop (Reference FIGURE 1B).

All output power transistors can be protected from regenerative bus overvoltage when utilizing dynamic braking with the addition of one PW-85010P6, PW-85030P6 or PW-85075P6 module. This module contains an overvoltage switch that is enabled when an overvoltage condition is detected. This switch is normally wired to an external (user supplied, application specific) load dump resistor to provide a load across the high voltage bus when overvoltage is detected. During an overvoltage condition, the status flag REGEN_STATUS is active (logic high (H)) indicating an overvoltage condition is occurring. (Reference FIGURE 1C)

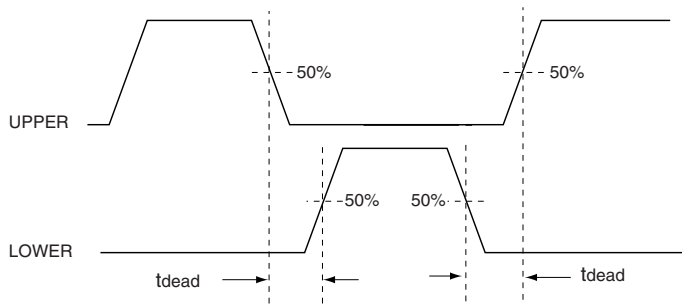


FIGURE 4. PW-8X010P6, PW-8X030P6 AND PW-8X075P6 DEAD BAND REQUIREMENT

PW-8X075P6, PW-8X030P6 AND PW-8X010P6

I/O AND OPERATION

UPPER, LOWER (INPUTS)

UPPER and LOWER are active high CMOS Schmitt-trigger inputs that control the gate drives of the output transistors (TTL compatibility requires external 10K pull-up resistors). Each input is electrically isolated from the output. As shown in FIGURE 4, a dead band (reference t_{dead} in TABLE 2) between turn off and turn on of UPPER and LOWER inputs is necessary to prevent output shoot through conduction.

$\overline{\text{SC FAULT}}$ (OUTPUT)

$\overline{\text{SC FAULT}}$ is an active low open collector output signal that indicates when the output of the module has experienced a short circuit condition. $\overline{\text{SC FAULT}}$ will remain active until $\overline{\text{DISABLE}}$/$\overline{\text{RESET}}$ is made active (L). The signal is inactive (high impedance) during normal operation. See SHORT CIRCUIT PROTECTION for more detail.

$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ (INPUT)

$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ is an active low CMOS Schmitt-trigger input. When $\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ is held active it does two things: 1.) Resets the $\overline{\text{SC FAULT}}$ (if it was active), and 2.) Disables the output (makes the output high impedance). If this line is used solely to clear $\overline{\text{SC FAULT}}$ then it only needs to be pulsed active. The duration of the $\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ active pulse must be at least tpw.reset to ensure that $\overline{\text{SC FAULT}}$ is cleared properly. When this line is inactive, the OUTPUT is allowed to respond to the other control lines of the module (UPPER, LOWER, SLEEP_MODE).

Note: TTL compatibility requires an external pull-up resistor.

$\overline{\text{AUTO RESET}}$ (INPUT)

$\overline{\text{AUTO RESET}}$ is an active low (L) input. When $\overline{\text{AUTO RESET}}$ is tied to $\overline{\text{SC FAULT}}$ the protection circuit will reset automatically after the short circuit fault has occurred, and a delay period, tcycle.auto, has expired. This automatic reset enables the output to respond to the input commands. See SHORT CIRCUIT PROTECTION for more detail.

SLEEP_MODE (INPUT)

SLEEP_MODE is an active high input that turns the internal power supply off. A logic low (L) enables the power supply and allows the motor drive to operate normally.

A logic high (H) on the SLEEP_MODE input disables the internal power supply, disabling the motor drive output. No damage will occur to the motor drive during turn on or turn off of the power supply. Additionally, no special power up sequence is required.

The UPPER and LOWER logic gate driver inputs should not be active while transitioning in and out of sleep mode. If the UPPER and LOWER logic inputs must be active while entering sleep

mode then $\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ must be held active while coming out of sleep mode.

Note: SLEEP_MODE has an internal pull-up resistor. If the input is not connected, it will default to logic high, turning the power supply and the motor drive off.

VCC,VCC-RTN (INPUTS)

The VCC and VCC-RTN are power connections that supply input power to the internal power supply, the gate drive and fault control circuits.

VBUS+, VBUS- (INPUTS)

VBUS+ and VBUS- are the high voltage power connections to the output stage. The high voltage can be either unipolar (+V and ground) or bipolar (+/- V). Care must be taken to ensure that the transient bus voltage VBUS at the module terminals never exceeds the absolute maximum supply ratings during switching excursions. External capacitor filtering will be required (See DDC's Applications Note AN/H-7).

OUTPUT (OUTPUT)

Output is the power switch output that is connected to one input of the motor and applies VBUS+, VBUS-, or high impedance to the motor based on the state of the control inputs. It is capable of sourcing or sinking up to the rated output current, and can withstand a short circuit to VBUS+ or VBUS- without any damage by automatically turning itself off (high impedance state).

SHORT CIRCUIT PROTECTION

The PW-8X010P6, PW-8X030P6 and PW-8X075P6 modules have provisions for complete short circuit protection from either a hard or soft short to the VBUS+ or VBUS- lines. Each output transistor on all PW-8X010P6, PW-8X030P6 and PW-8X075P6 modules are protected from a hard (direct, low impedance) short to the VBUS+ or VBUS- lines by circuitry that detects the de-saturation voltage for that transistor during a short condition. Once a hard short circuit condition is detected, the affected output transistor is shut down and $\overline{\text{SC FAULT}}$ output is set active (logic low (L)). The $\overline{\text{SC FAULT}}$ signal can be used by a controller as a signal to initiate a fault routine to reset or shut down the system. The $\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ input can be used to shut down the gate drivers if a short persists. If the $\overline{\text{AUTO RESET}}$ is tied to $\overline{\text{SC FAULT}}$, the circuit will automatically reset when a fault occurs. This inactivates $\overline{\text{SC FAULT}}$ and reactivates the output transistor within the tcycle.auto time period. If the short is still present, the circuit will repeat the shut down and automatically reset until the short is clear.

Protection against a soft-short requires the addition of current sensing Magnum Motor Drive modules and external circuitry. When a soft short occurs, the external circuit can set $\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$ low (L) to shut down the gate drivers.

PW-84010P6, PW-84030P6 AND PW-84075P6

I/O AND OPERATION

PW-84010P6, PW-84030P6 and PW-84075P6 modules can be added to a motor drive to provide current monitoring and overcurrent protection capability. The following section describes the PW-84010P6, PW-84030P6 and PW-84075P6 modules and their features.

VDD, VDD-RTN

VDD and VDD-RTN supplies input power to the current amplifier.

VIRSENSE (OUTPUT)

VIRSENSE is an output that provides a voltage proportional to the current passing through RSENSE. The voltage is scaled by a reference voltage VREF and is equal to VREF/2 to represent zero current. A voltage greater than VREF/2 indicates a positive current flow (positive voltage from RSENSE + to RSENSE -) through RSENSE. See FIGURE 1B.

This VIRSENSE voltage is scaled by the input voltage at VIREF, where:

VIRSENSE = (VREF/2) + (VIRSENSE Gain) * (IRSENSE) or VIRSENSE = (VREF/2) + (VREF / .504* RSENSE) * (IRSENSE)

Note: IRSENSE is current flowing through RSENSE (refer to Table 3 for RSENSE value). Zero amps in RSENSE is indicated when VIRSENSE = VREF/2. A voltage greater (less) than VREF/2 indicates a positive (negative) current flow through RSENSE with a value defined by the VIRSENSE equation. VIRSENSE is electrically isolated from the output stage. A positive (negative) current flow from RSENSE + to RSENSE - produces a positive (negative) voltage measurement (See FIGURE 1B). When the power supply is shut down (SLEEP_MODE input high), the voltage at VIRSENSE will indicate 0V.

Note: During normal operation 0 Volts at VIRSENSE represents maximum negative current.

VREF (INPUT)

A precision voltage reference from an external source is connected to the VREF pin to set the output voltage scale for VIRSENSE and VIRSENSE_ABS. Note: The accuracy of the VIRSENSE and VIRSENSE_ABS outputs are subject to the accuracy and temperature coefficient of VREF. These must be taken into account in calculating the overall accuracy of VIRSENSE.

RSENSE+, RSENSE- (INPUTS)

The RSENSE+ and RSENSE- pins are connected to an internal shunt resistor and monitoring circuitry. These pins can be connected anywhere within the isolation restrictions on the pins (600V to power pins, 2500V to logic pins). These pins are typi-

cally connected in series with the OUTPUT, VBUS+ or VBUS-, to measure motor drive current.

VIRSENSE_ABS (OUTPUT)

VIRSENSE_ABS output voltage is the absolute value of the VIRSENSE voltage signal. VIRSENSE_ABS is zero volts when there is no current flowing through the RSENSE resistor. It will increase towards the value of VIREF as the current in RSENSE approaches either ± full-scale current (measurement limits of VIRSENSE). VIRSENSE_ABS is an open source output and is "wire-OR-able". When two or more VIRSENSE_ABS outputs are "wire-OR-ed", the highest voltage will appear on the common signal. A typical use for combining these outputs is for determining when an overload condition has occurred. The VIRSENSE_ABS voltage is scaled by the input voltage VIRSENSE where:

$$V_{IRSENSE\_ABS} = 2 \times |V_{IRSENSE} - V_{REF}/2|$$

$\overline{\text{OC FAULT}}$ OUTPUT

$\overline{\text{OC FAULT}}$ is an active low open drain output that goes active when the current flowing through RSENSE has exceeded the $\overline{\text{OC FAULT}}$ trip level. This signal is not latched like $\overline{\text{SC FAULT}}$, and goes inactive as soon as the over current condition stops.

PW-85010P5, PW-85030P6 AND PW-85075P6

I/O AND OPERATION

PW-85010P6, PW-85030P6 and PW-85075P6 modules can be added to a motor drive to provide overvoltage protection capability. The following section describes the PW-85010P6, PW-85030P6 and PW-85075P6 modules and its features.

REGEN_STATUS (OUTPUT)

The REGEN_STATUS pin is referenced to VBUS-, and indicates the state of the regen clamp switch (H = on, L = off). An external opto-isolator input can be connected between REGEN_STATUS and VBUS- to translate this status to logic circuits if desired. The REGEN_STATUS output is connected to the overvoltage amp through a 5kΩ resistor. When the regen clamp switch is active (inactive), the overvoltage amp sources +15V (0V) through the 5KΩ resistor. (see FIGURE 1C).

REGEN_CLAMP (OUTPUT) (REF. R20 ON FIGURES 11 AND 12)

An external load dump resistor is connected between REGEN_CLAMP and VBUS+. When VBUS+ reaches the overvoltage trip level set by the OV_ADJ, the internal clamp circuit will apply the load dump resistor from VBUS+ to the VBUS-, thereby dissipating the regenerative energy of the bus into the external resistor.

OV_ADJ (INPUT)

The PW-85010P6, PW-85030P6 and PW-85075P6 modules are internally set for a trip voltage of 400V. The trip point can be adjusted to a higher or lower voltage by connecting an external overvoltage adjust resistor ROV_ADJ (Ref. R21 on FIGURES 11 and 12).

To set the overvoltage trip point to a voltage above 400 volts connect ROV_ADJ between the OV_ADJ and OV_ADJ_HIGH pins. To set the OV trip point to a voltage below 400 volts connect

PW-8X075P6, PW-8X030P6 AND PW-8X010P6 TYPICAL OVERVOLTAGE TRIP VS. OV ADJUST SETTINGS

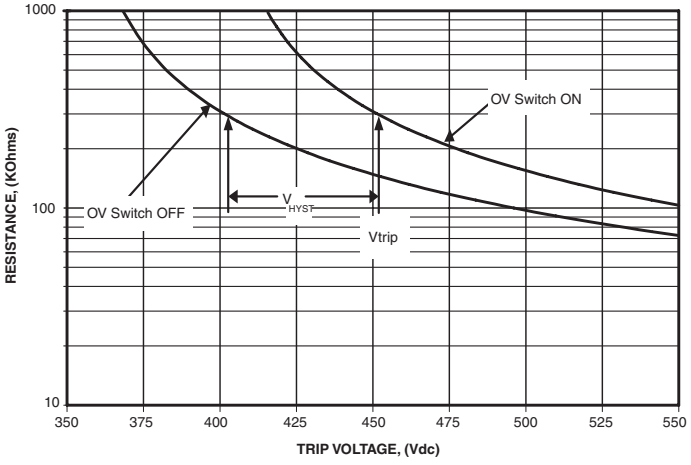


FIGURE 5A. EXTERNAL OV ADJUST RESISTOR CONNECTED TO OV_ADJ_HIGH

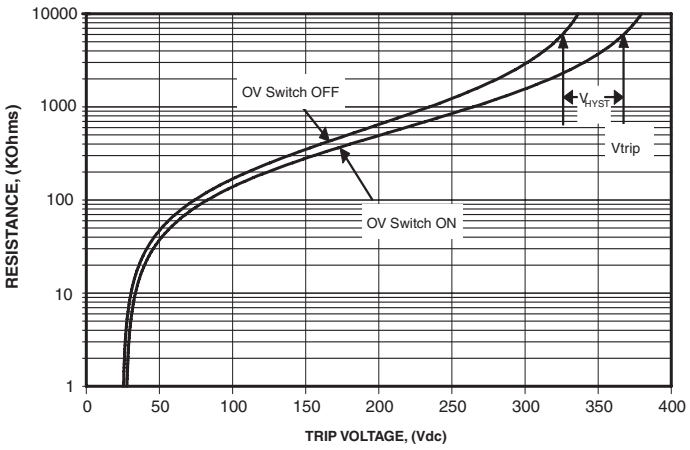


FIGURE 5B. EXTERNAL OV ADJUST RESISTOR CONNECTED TO OV_ADJ_LOW

R_{OV_ADJ} between the OV_ADJ and OV_ADJ_LOW pins. The value of R_{OV_ADJ} for voltages above (below) 400 volts should be selected based upon FIGURE 5A (5B).

POWER DISSIPATION

There are three major contributors to power dissipation in the motor drive: conduction losses, switching losses, and flyback diode losses. Consider the following arbitrary operating conditions for the 2 quadrant example using the PW-8X075.

$V_{BUS} = V_{CE} = +200V$
$f_{PWM} = 10kHz$
duty cycle = 50% (ton = 50µs; toff = 50µs)
$I_O = I_C = 40A$, Module Output Current (see FIGURE 6)
during toff, $I_f = I_O$

The power dissipation of the 2 quadrant example circuit shown in FIGURE 6 can now be calculated using information from the data sheet as follows:

Q1 - Transistor data (Output Stage)

$T_{J\ MAX} = 150\ °C$ (TABLE 2)
$\theta_{JC.IGBT} = 0.55°C/W$ (TABLE 2)
$V_{CE(SAT)} = 2.2V$
E_{ON} (50A, 270V) = 1.5 mJ (TABLE 2)
E_{OFF} (50A, 270V) = 2.7 mJ (TABLE 2)

CR1 - Flyback diode data

$T_{J\ MAX} = 150\ °C$
θ_{JC}.diode = 0.87°C/W (TABLE 2)
V_F(avg) = 1.7V

1. Q1 Transistor Conduction Losses (P_C)

$P_C = I_C \times V_{CE(SAT)} \times$ duty cycle
$P_C = 40A \times 2.2 \times 50\%$
$P_C = 40A \times 2.2 \times 0.5$
$P_C = 44W$

2. Q1 Transistor Switching Losses (P_S)

$P_S = [E_{ON}$ (scaled) + E_{OFF} (scaled)] x f_{PWM}
Note: $E_{ON/OFF}$ (scaled) from conditions in TABLE 2.
E_{ON} (scaled) = (E_{ON} @ 50A, 270V) x (V_{BUS} / 270V) x (I_O/50A)]
E_{ON} (scaled) = [(1.5mJ) x (200V / 270V) x (40A / 50A)]
E_{ON} (scaled) = 0.88 mJ

E_{OFF}(scaled) = [(E_{OFF} @ 50A, 270V) x (V_{BUS}/270V) x (I_O/50A)]
E_{OFF}(scaled) = [(2.7 mJ) x (200V/270V) x (40A/50A)]
E_{OFF}(scaled) = 1.6 mJ

P_S = (0.88 mJ + 1.6 mJ) x 10kHz
$P_S = 24.8W$

3. CR1 Flyback Diode Losses (Pd)

$P_d = I_C \times V_F$(avg) x [1 - duty cycle]
$P_d = 40A \times 1.7V$ x [1 - 50%]
$P_d = 40A \times 1.7V$ x [1 - 0.5]
$P_d = 40A \times 1.7V \times 0.5$
$P_d = 34W$

4. Q1 Transistor Power Dissipation (P_T)

$P_T = P_C + P_S$
$P_T = 44W + 24.8W$
$P_T = 68.8W$

5. Maximum Allowed Module Case Temperature

$T_{CASE.ALLOWED.IGBT} = Tjmax - \theta jc.IGBT \times P_T$
$T_{CASE.ALLOWED.IGBT} = 150°C - [(0.55°C/W) \times (68.8W)]$
$T_{CASE.ALLOWED.IGBT} = 112°C$

$T_{CASE.ALLOWED.diode} = Tjmax - \theta jc.diode \times Pd$
$T_{CASE.ALLOWED.diode} = 150°C - [(0.87°C/W) \times (34W)]$
$T_{CASE.ALLOWED.diode} = 120°C$

Maximum allowed case temperature for the module will be the lesser of the allowed diode and allowed IGBT case tempera-

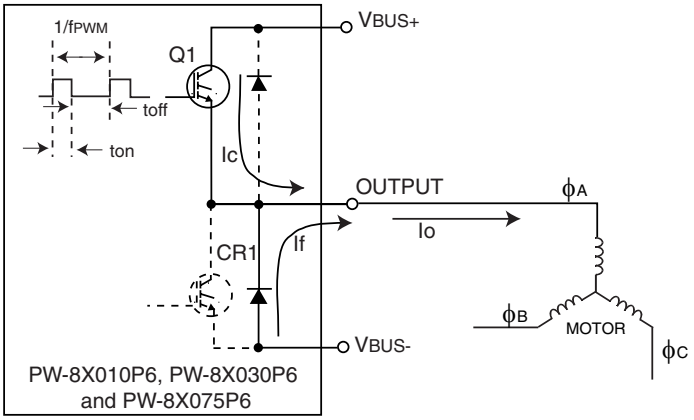


FIGURE 6. 2 QUADRANT POWER DISSIPATION CIRCUIT

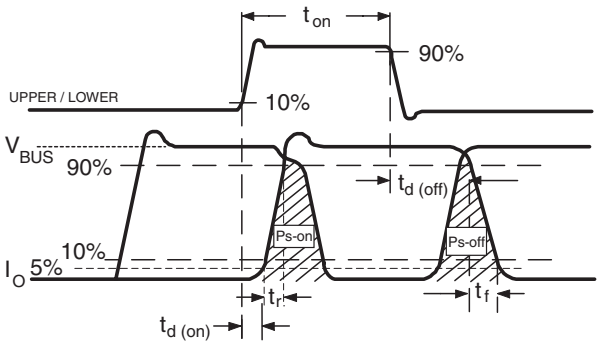


FIGURE 7. OUTPUT CHARACTERISTICS

TABLE 6. PW-8X010P6, PW-8X030P6 AND PW-8X075P6 TRUTH TABLE					
UPPER	LOWER	$\overline{\text{DISABLE}}$/$\overline{\text{RESET}}$	SLEEP-MODE	$\overline{\text{SC-FAULT}}$	OUT
0	0	X	X	X	Z
1	0	1	0	1	VBUS+
0	1	1	0	1	VBUS-
1	1	X	X	X	Z
1	0	1	0	0	*
0	1	1	0	0	*
X	X	0	X	X	Z
X	X	X	1	X	Z

X = Indicates that this input is irrelevant.
Z = High Impedance (off).
*= Fault will disable the transistor that caused the fault.
The output state could be Z or ON.

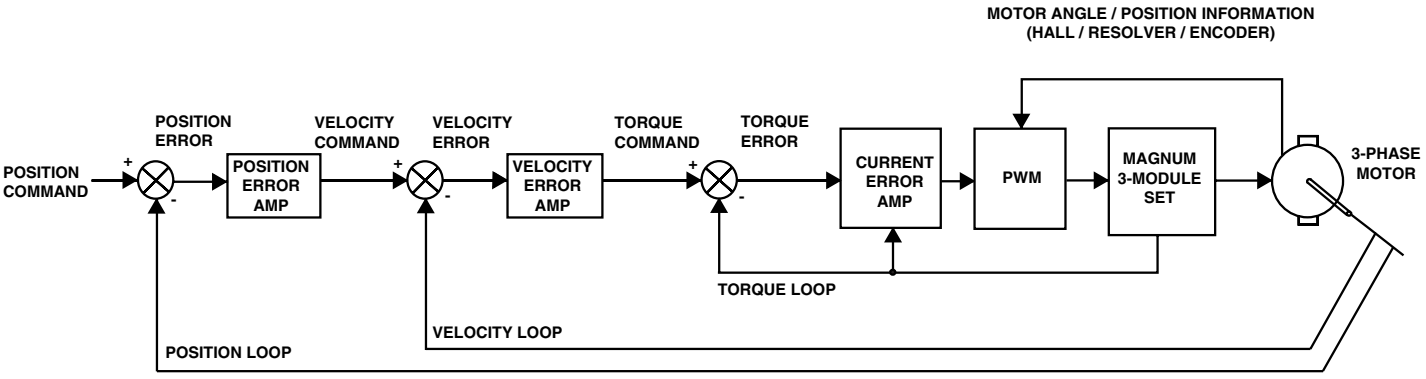


FIGURE 8. TYPICAL POSITION, VELOCITY AND TORQUE CONTROL LOOP

APPLICATIONS

POSITION OR VELOCITY CONTROL USING DSP

FIGURE 11 shows an example of position and/or velocity control hook-up with inner torque loop using the Digital Signal Processor (DSP) for motor control. Using software, the DSP can be implemented with one of several motor control algorithms such as FOC (Field Oriented Control) with SVM (Space Vector Modulation).

TORQUE CONTROL USING UC2625 MOTOR CONTROLLER

FIGURE 12 shows an example of torque control loop with regenerative clamp protection using a UC2625, two PW-84010P6, PW-84030P6 or PW-84075P6 modules, and one PW-85010P6, PW-85030P6 or PW-85075P6 module. The two PW-84010P6, PW-84030P6 or PW-84075P6 modules (½ bridge with current sense) sense the current in motor phase B and C. VIRSENSE pins on each of the PW-84010P6, PW-84030P6 or PW-84075P6 modules are connected to the decommuntation circuit (shown in FIGURE 14) to produce bipolar output voltage that is compared to the torque commanded input to produce an error signal. The UC2625 uses this error signal to regulate the output current (or torque) by controlling the duty cycle of the output transistors. The gain of the current decommuntation circuit shown in FIGURE 14 has been selected to accommodate a ±10V command input voltage.

For the case when a resolver is available instead of Hall-effect devices, the circuit shown in FIGURE 13 converts the resolver (sin and cos) signals to Hall signals which can be used to commutate the output transistors.

HALL SIGNAL COMMUTATION

The hall signals HAB, HBC, HCA are logic signals from the motor Hall-effect sensors. The UC2625 uses a phasing convention referred to as 120 degree spacing; that is, the output of HAB is in phase with motor back EMF voltage VAB, the output of HBC is in phase with motor back EMF voltage VBC, and the output of HCA is in phase with motor back EMF voltage VCA. Logic "1" (or HIGH) is defined by an input greater than 2.4Vdc or an open circuit to the controller; Logic "0"(or LOW) is defined as any Hall voltage input less than 0.8Vdc.

The UC2625 will operate with Hall phasing of 60° or 120° electrical spacing. If 60° commutation is used, then the output of HCA must be inverted as shown in FIGURES 9 and 10. In FIGURE 9 the Hall sensor outputs are shown with the corresponding back EMF voltage they are in phase with.

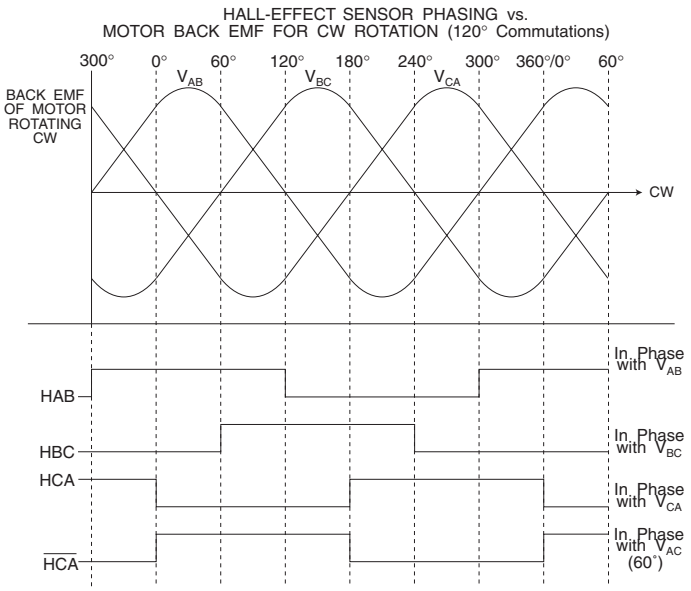


FIGURE 9. HALL PHASING

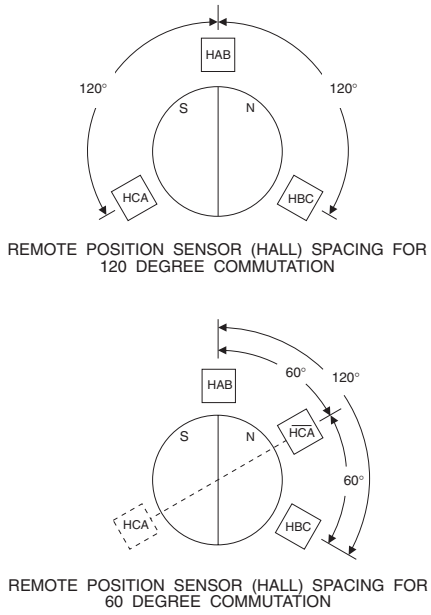
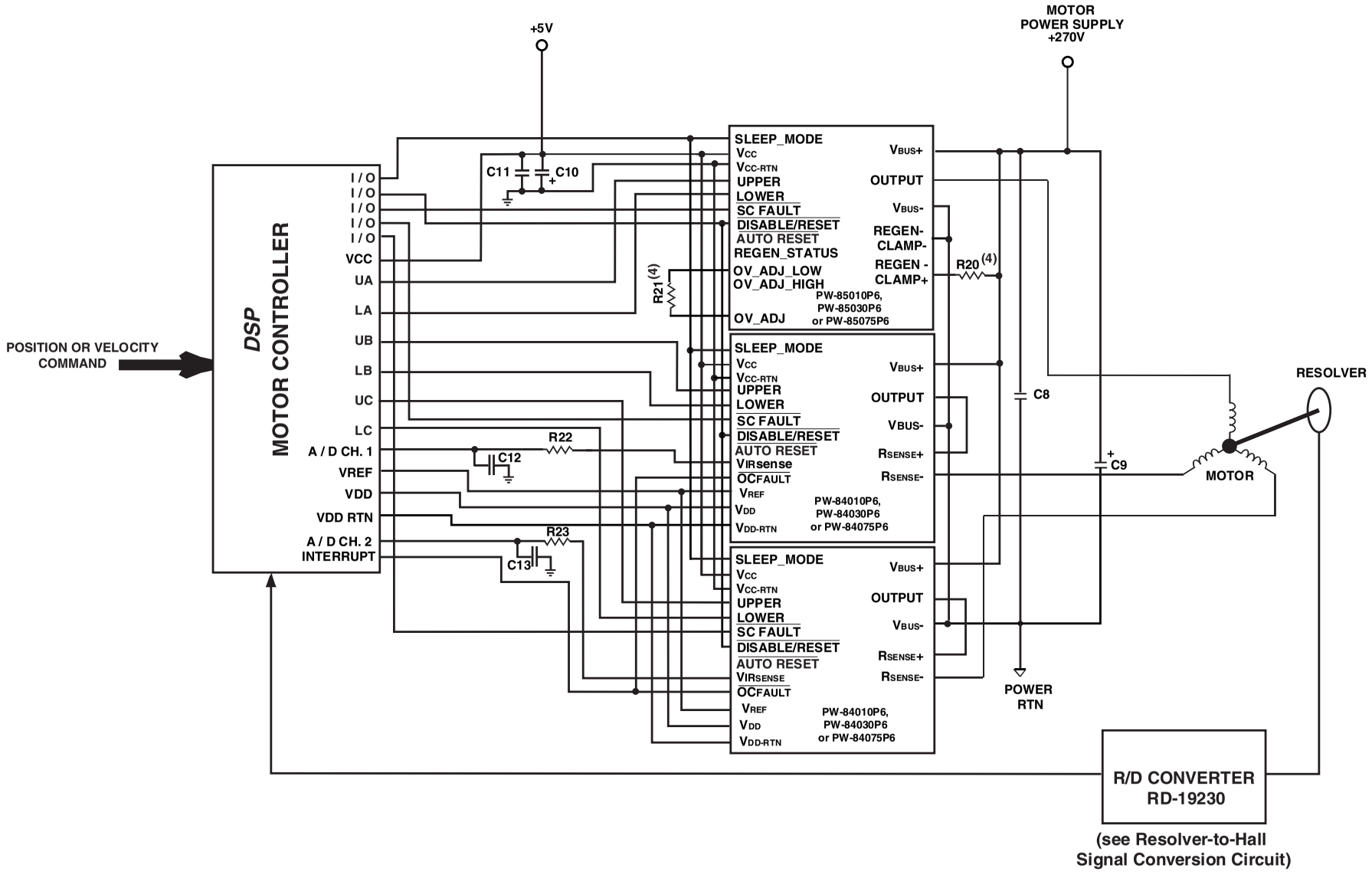
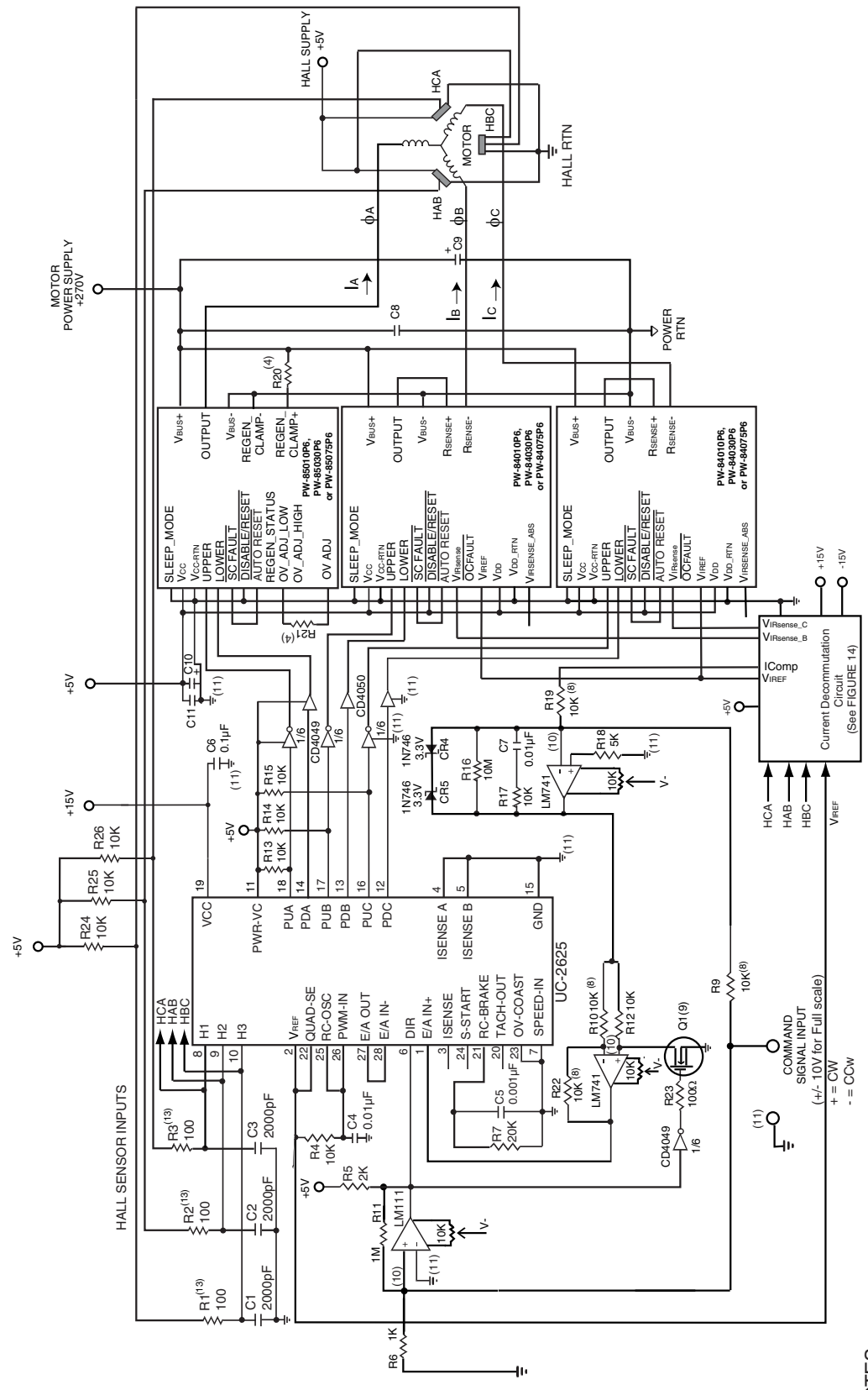


FIGURE 10. HALL SENSOR SPACING



NOTES:
1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/H-7, PW-82351 Motor Drive Power Supply, equation 1.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/H-7, PW-82351 Motor Drive Power Supply, equation 1.
3. C10 is 22 µF, 15 V electrolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20 (Load dump resistor), and R21 (OV Adjust resistor) is application specific. (See OV Adjust and Regen description for details)

FIGURE 11. PW-8X010P6, PW-8X030P6 AND PW-8X075P6 POSITION OR VELOCITY HOOK-UP USING DSP MOTOR CONTROLLER



NOTES:

1. C8 is a ceramic capacitor and should be selected per DDC Application Note AN/H-7, Magnum Motor Drive Power Supply Capacitor Selection.
2. C9 is an electrolytic capacitor and should be selected per DDC Application Note AN/H-7, Magnum Motor Drive Power Supply Capacitor Selection.
3. C10 is 22 µF, 15 V electrolytic capacitor. C11 is 0.1 µF, 50 V ceramic capacitor.
4. Resistance and power of R20 (Load dump resistor), and R21 (OV Adjust resistor) is application specific. (See OV Adjust and Regen description for details)
5. All resistors have a tolerance of ±10%, unless otherwise specified.
6. The CD4050 converts the +15V logic output of the UC-2625 to +5V logic signals.
7. The CD4049 inverts the +15V logic signal from the UC-2625, and converts it to a +5V logic signal.
8. 1% or better, depending on required accuracy.
9. Q1 can be either IRML2402 or IRMU014 or IRLD014.
10. These high impedance inputs and summing junctions of the operational amplifiers are highly sensitive to noise.
11. These grounds should be closely tied together to reduce ground noise effect.
12. Connect Hall sensor inputs to motor shaft position sensors that are 120 electrical degrees apart. Motors with 60 electrical degree position sensor coding can be used if one of the position sensor signals are inverted (See FIGURES 9 and 10).
13. May need to increase resistance to reduce excessive noise.

FIGURE 12. PW-8X010P6, PW-8X030P6 AND PW-8X075P6 TORQUE HOOK-UP USING UC-2625 MOTOR CONTROLLER

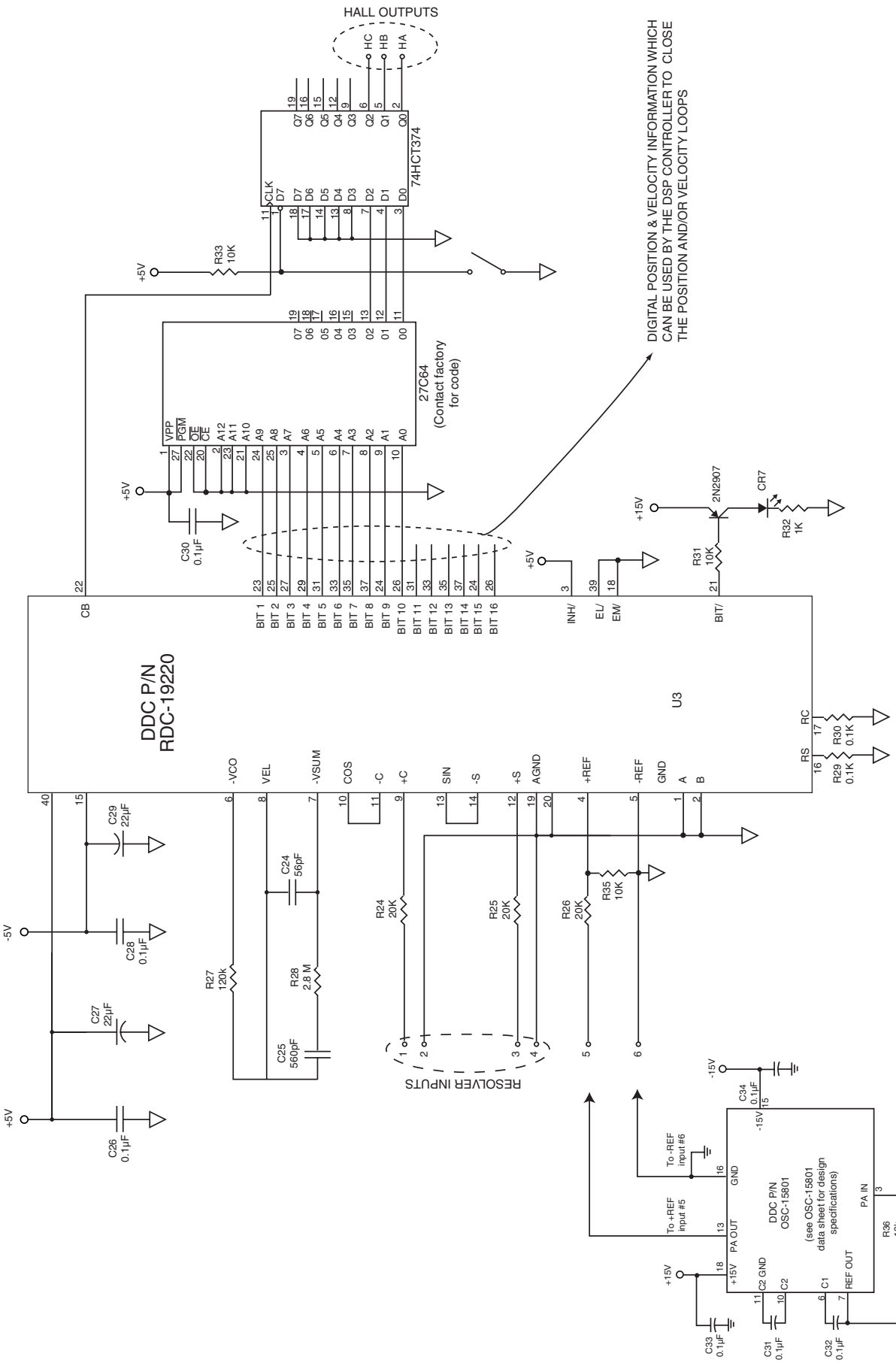
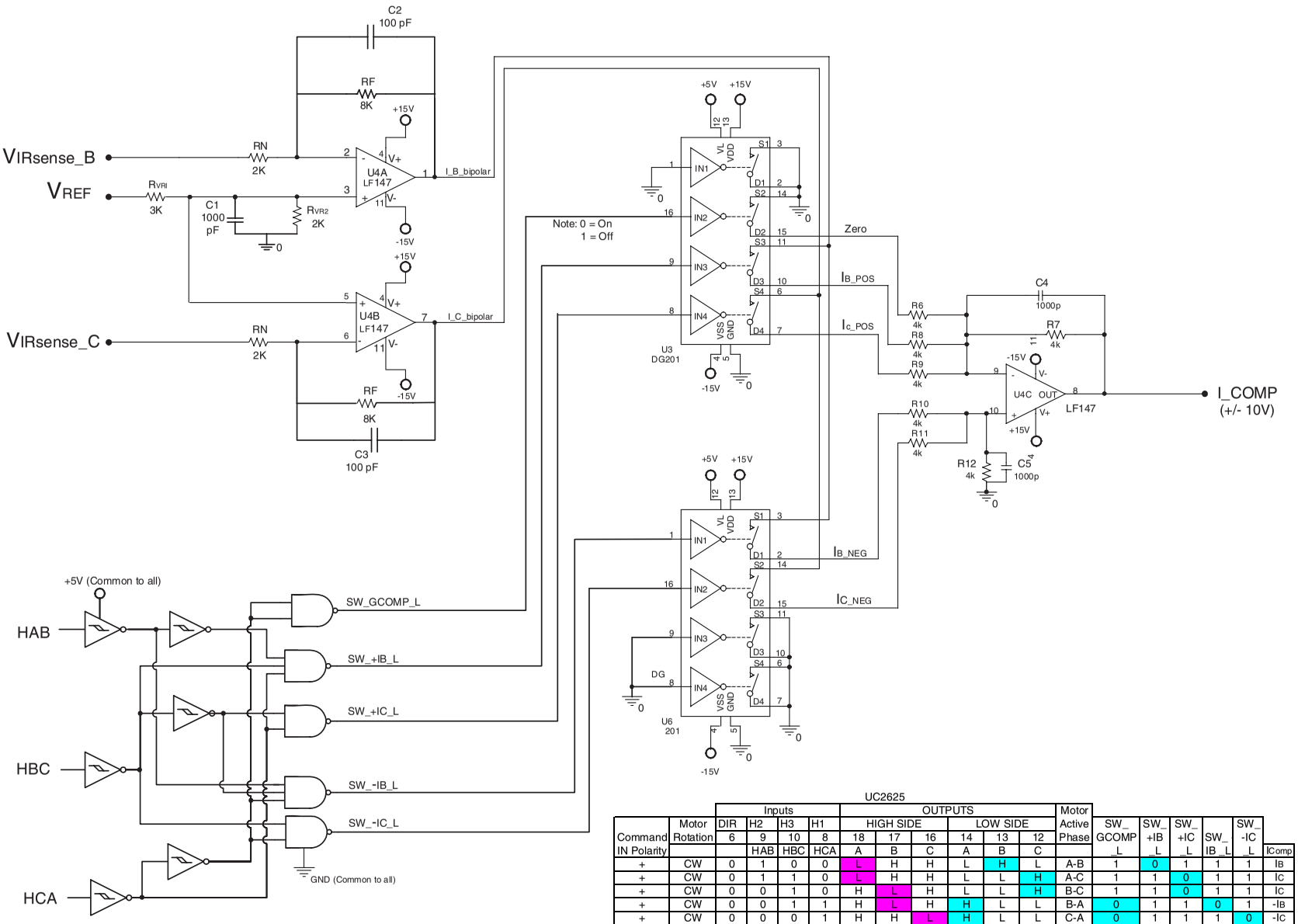


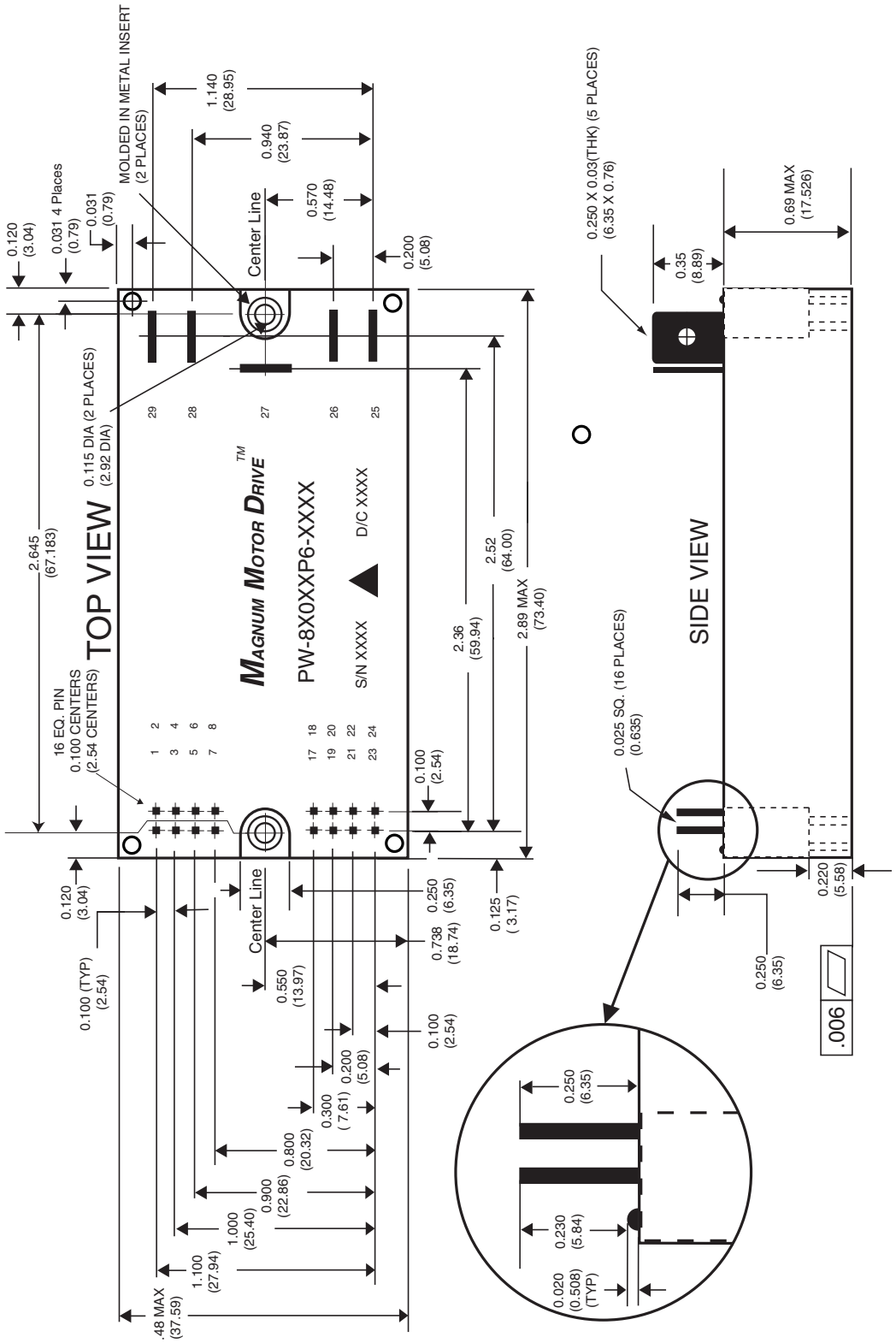
FIGURE 13. RESOLVER TO HALL SIGNAL CONVERSION CIRCUIT



UC2625

Command IN Polarity	Motor Rotation	Inputs DIR 6	H2 9	H3 10	H1 8	OUTPUTS HIGH SIDE 18	17	16	LOW SIDE 14	13	12	Motor Active Phase	SW_ GCOMP _L	SW_ +IB _L	SW_ +IC _L	SW_ IB _L	SW_ -IC _L	
			HAB	HBC	HCA	A	B	C	A	B	C							ICOMP
+	CW	0	1	0	0	L	H	H	L	H	L	A-B	1	0	1	1	1	IB
+	CW	0	1	1	0	L	H	H	L	L	H	A-C	1	1	0	1	1	IC
+	CW	0	0	1	0	H	L	H	L	L	H	B-C	1	1	0	1	1	IC
+	CW	0	0	1	1	H	L	H	H	L	L	B-A	0	1	1	0	1	-IB
+	CW	0	0	0	1	H	H	L	H	L	L	C-A	0	1	1	1	0	-IC
+	CW	0	1	0	1	H	H	L	L	H	L	C-B	0	1	1	1	0	-IC
-	CCW	1	1	0	1	H	L	H	L	L	H	B-C	0	1	1	1	0	-IC
-	CCW	1	0	0	1	L	H	H	L	L	H	A-C	0	1	1	1	0	-IC
-	CCW	1	0	1	1	L	H	H	L	H	L	A-B	0	1	1	0	1	-IB
-	CCW	1	0	1	0	H	H	L	L	H	L	C-B	1	1	0	1	1	IC
-	CCW	1	1	1	0	H	H	L	H	L	L	C-A	1	1	0	1	1	IC
-	CCW	1	1	0	0	H	L	H	H	L	L	B-A	1	0	1	1	1	IB

FIGURE 14. CURRENT SCALING AND DECOMMUNTATION CIRCUIT



NOTES:
1. Dimensions are in inches (mm).

MOUNTING CONSIDERATIONS:
For 2 or more modules, minimum spacing center line to center line - 1.5 inches (38.1 mm)

FIGURE 15. PW-8X010P6, PW-8X030P6, AND PW-8X075P6 OUTLINE

TABLE 7: PIN ASSIGNMENTS			
PIN #	FUNCTIONS DESCRIPTION		
	PW-83010P6 PW-83030P6 PW-83075P6	PW-84010P6 PW-84030P6 PW-84075P6	PW-85010P6 PW-85030P6 PW-85075P6
CONTROL PINS			
1	$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$	$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$	$\overline{\text{DISABLE}}$ / $\overline{\text{RESET}}$
2	V_{CC}	V_{CC}	V_{CC}
3	UPPER	UPPER	UPPER
4	$V_{CC\text{-}RTN}$	$V_{CC\text{-}RTN}$	$V_{CC\text{-}RTN}$
5	LOWER	LOWER	LOWER
6	SLEEP_MODE	SLEEP_MODE	SLEEP_MODE
7	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$	$\overline{\text{SC FAULT}}$
8	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$	$\overline{\text{AUTO RESET}}$
17	N/C	V_{REF}	OV_ADJ_HIGH (1) (2)
18	N/C	$V_{IRSENSE}$	REGEN_STATUS
19	N/C	$V_{IRSENSE\_ABS}$	N/C
20	N/C	V_{DD}	OV_ADJ
21	N/C	$V_{DD\text{-}RTN}$	N/C
22	N/C	$\overline{\text{OC FAULT}}$	OV_ADJ_LOW (1) (3)
23	N/C	N/C	N/C
24	N/C	N/C	N/C
POWER PINS			
25	N/C	R_{SENSE} -	REGEN_CLAMP+
26	N/C	R_{SENSE}+	REGEN_CLAMP-
27	V_{BUS}+	V_{BUS}+	V_{BUS}+
28	OUTPUT	OUTPUT	OUTPUT
29	V_{BUS}-	V_{BUS}-	V_{BUS}-

NOTES:
(1) Connection for external OV adjust resistor only.
(2) Caution: V_{BUS}- voltage present on this pin.
(3) Caution: V_{BUS}+ voltage present on this pin.

ORDERING INFORMATION

PW-8X 0XX P6- X X 0

Process Requirements:
See TABLE 8

Temperature Grade/Data Requirements:
C = -55°C to +100°C
2 = -40°C to +85°C
3 = 0°C to +70°C
G = -55°C to +100°C with Variables Test Data
5 = -40°C to +85°C with Variables Test Data
8 = 0°C to +70°C with Variables Test Data

Voltage Rating
6 = 600V

Current Rating
010 = 10A
030 = 30A
075 = 75A

Features
3 = Standard ½ Bridge
4 = Standard ½ Bridge w/ current sense
5 = Standard ½ Bridge w/ regenerative voltage clamp

These products contain tin-lead solder finish as applicable to solder dip requirements.

TABLE 8. DDC PROCESSING - IPC-A-610

PROCESS	PROCESS REQUIREMENT OPTION			
	1	3	5	7
Burn-In		•		•
Temperature Cycle			•	•

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