Feature

- Fully synchronous; all signals registered on positive edge of system clock
- Internal, pipelined operation; column address can be changed every clock cycle
- Four internal banks for concurrent operation
- Programmable Burst Lengths: 1, 2, 4 ,8 or continuous
- Auto precharge, includes concurrent auto precharge
- Auto Refresh and Self Refresh Modes
- Optional Partial Array Self Refresh (PASR) and Temperature Compensated Self Refresh (TCSR)
- Deep Power Down Mode (DPD)
- Selectable output drive strength (DS)
- LVTTL-compatible inputs and outputs
- V_{DD}/V_{DDQ}= 1.70~1.95V

Table 1: Key Timing Parameters (CL=3)

Speed Grade	Clock Rate (MHz)		Access Time(ns)	
	CL=2	CL=3	CL=2	CL=3
-6	111	166	8	5
-75	111	133	8	5.4

Table 2: Configuration Addressing

Architecture	32M x 16	16M x 32	16M x 32 Reduced page –size option[1]
Number of banks	4	4	4
Bank address balls	BA0, BA1	BA0, BA1	BA0, BA1
Row address balls	A[12:0]	A[12:0]	A[13:0]
Column address balls	A[9:0]	A[8:0]	A[7:0]
Refresh count	8k	8k	8k

Note: 1. For reduced page-size option, contact factory for availability.

Options — Marking

- V_{DD} /V_{DDQ}
  - -1.8V/1.8V — M
- Configuration
  - -32Meg x 16 (8 Meg x 16 x 4 banks) — 32M16
  - -16Meg x 32 (4 Meg x 32 x 4 banks) — 16M32
- Row-size option
  - -JEDEC-standard addressing
  - -JEDEC reduced page-size addressing
- Plastic “green” package
  - -54-ball VFBGA (x16: 8 x 9mm) — G
  - -90-ball VFBGA (x32: 8 x13mm) — K
- Timing – cycle time
  - -6.0ns @ CL=3 — S1
  - -7.5ns @ CL=3 — S2
- Operating temperature range
  - -Commercial (-25℃ to +85℃)
  - -Industrial (-40℃ to +85℃)

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Description

The 512Mb Mobile SDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a qual-bank DRAM.

The 512Mb chip is organized as 8Mbit x 4 banks x 16 I/O or 4Mbit x 4 banks x 32 I/O device. Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits. In the reduced page-size option, each of the x32's 134,217,728-bit banks are organized as 16,384 rows by 256 columns by 32 bits. To achieve high-speed operation, our LPSDR SDRAM are quad-bank DRAM that operate at 1.8V, pipelined architecture and include a synchronous interface. The pipelined architecture enables changing the column address on every clock cycle to achieve a high-speed, fully random access. All signals are registered on the positive edge of the clock signal, CLK. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provides seamless high-speed, random access operation.

LPSDR SDRAM, Read and Write access are burst oriented. The address bits registered coincident with the ACTIVE command to select the row in the specific bank. And then the address bits registered with the READ or WRITE command to select the starting column location in the bank for the burst access. The burst length can be programmed as 1, 2, 4, 8 or 16. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of burst access.

LPSDR SDRAM with Auto Refresh mode, and the Power-down mode for power saving. And the Deep Power Down Mode can achieve the maximum power reduction by removing the memory array power within Low Power DDR SDRAM. With this feature, the system can cut off almost all DRAM power without adding the cost of a power switch and giving up month-board power-line layout flexibility. Self Refresh mode with Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR) options, which allow users to achieve additional power saving. The TCSR and PASR options can be programmed via the extended mode register. The two features may be combined to achieve even greater power saving.

All inputs are LVCMOS compatible. Devices will have a V_{DD} and V_{DDQ} supply of 1.8V (nominal).

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Ordering Information

Green

Organization	Part Number	Package	Speed			
			^{t}CK (ns)	Clock (MHz)	Data Rate (Mb/s/pin)	CL
16M x32	NT6SM16M32AK-S1	90-Ball FBGA	6.0	166	166	3
	NT6SM16M32AK-S2		7.5	133	133	3
32M x16	NT6SM32M16AG-S1	54-Ball FBGA	6.0	166	166	3
	NT6SM32M16AG-S2		7.5	133	133	3

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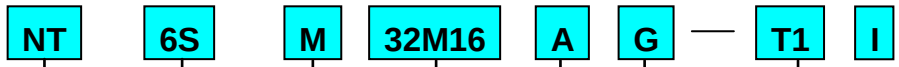
NANYA Mobile Component/Wafer Part Numbering Guide:



NANYA Technology

Product Family

6S =LPSDR SDRAM

6D =LPDDR SDRAM

6V =LPDDR2-S2 SDRAM

6T = LPDDR2-S4 SDRAM

6X = LPSDR/DDR comb

6Y = LPDDR2-S2/S4 comb

Interface & Power (V_{DD} & V_{DDQ})

M = LVCMOS (1.8V, 1.8V)

N = LVCMOS (1.8V, 1.2V)

Interface & Power (V_{DD1} , V_{DD2} , V_{DDQ} , V_{DDCA})

L = HSUL_12 (1.8V, 1.2V, 1.2V, 1.2V)

H = HSUL_12 (1.8V, 1.35V, 1.2V, 1.2V)

Organization (Depth, Width): M=Mono; T=DDP[1] ; F=QDP[2]

256Mb = 16M16 = 8M32 = 8M32R[3]

512Mb = 32M16 = 16M32 = 16M32R

1Gb = 64M16 = 32M32 = 32M32R

2Gb = 256M8 = 128M16 = 64M32 = 64M32R

4Gb = 256M16 = 128M32 = 64T64

8Gb = 128T64 = 128F64

Note1: DDP – Dual Die Package

Note2: F = Quartic Die Package

Note3: R= Reduced page size

Device Version

A = 1st version

B = 2nd version

C = 3rd version

Grade

I =Industrial Grade

N/A =Commercial Grade

Speed

LPSDR

S1 = 166MHz @ CL=3

S2 = 133MHz @ CL=3

LPDDR

T1 = 5.0ns @ CL=3

T2 = 5.4ns @ CL=3

T3 = 6.0ns @ CL=3

T4 = 7.5ns @ CL=3

LPDDR2-S2

T1 = 5.0ns @ RL=3

T3 = 6.0ns @ RL=3

LPDDR2-S4

G0 = 1.8ns @ RL=8

G1 = 2.5ns @ RL=6

G2 = 3.0ns @ RL=5

G3 = 3.7ns @ RL=4

G4 = 5.0ns @ RL=3

Package Code (Green)

G = 54-Ball BGA (LPSDR, x16)

D = 60-Ball BGA (LPDDR, x16)

K = 90-Ball BGA (LPSDR, x32)

C = 90-Ball BGA (LPDDR, x32)

A = 79-Ball BGA (LPDDR2, x16)

I = 134-Ball BGA (LPDDR2, x32)

Q = 168-Ball PoP-VFBGA (LPDDR2)

R = 216-Ball PoP-VFBGA (LPDDR2)

3 = 240-Ball PoP-VFBGA (LPDDR2)

0 = Wafer (KGD)

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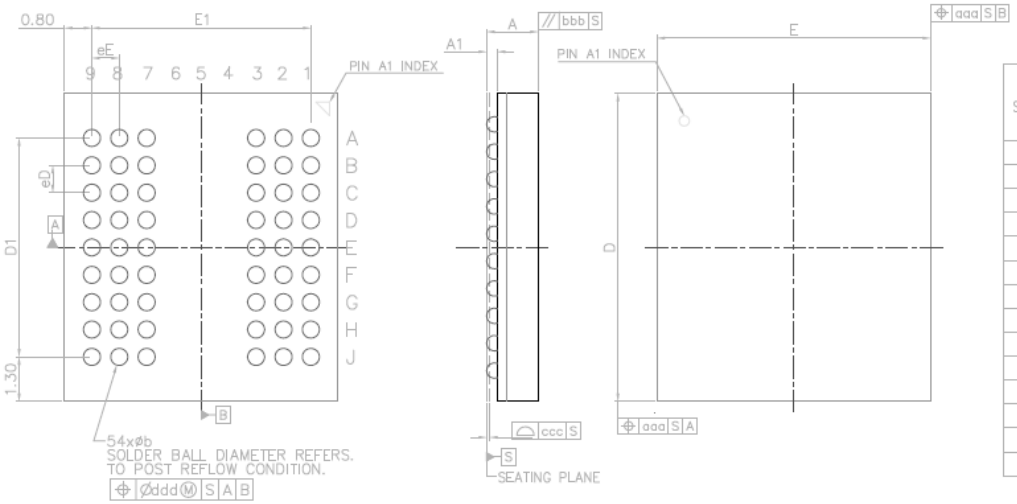
Pin Configuration – 54 balls BGA Package (x16)

< TOP View>

See the balls through the package

	1	2	3	4	5	6	7	8	9
A	Vss	DQ15	VssQ				VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ				VssQ	DQ2	DQ1
C	DQ12	DQ11	VssQ				VDDQ	DQ4	DQ3
D	DQ10	DQ9	VDDQ				VssQ	DQ6	DQ5
E	DQ8	A13	Vss				VDD	LDQM	DQ7
F	UDQM	CLK	CKE				CAS#	RAS#	WE#
G	A12	A11	A9				BA0	BA1	CS#
H	A8	A7	A6				A0	A1	A10
J	Vss	A5	A4				A3	A2	VDD

Package Dimensions (x16; 54 balls; 0.8mmx0.8mm Pitch; 8 x 9mm BGA Package)



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.86	0.93	1.00
A1	0.30	0.35	0.40
b	0.40	0.45	0.50
D	8.90	9.00	9.10
E	7.90	8.00	8.10
D1	6.40 BSC.		
E1	6.40 BSC.		
eE	0.80 BSC.		
eD	0.80 BSC.		
aaa	0.15		
bbb	---	---	0.100
ccc	---	---	0.100
ddd	---	---	0.080
N	54		

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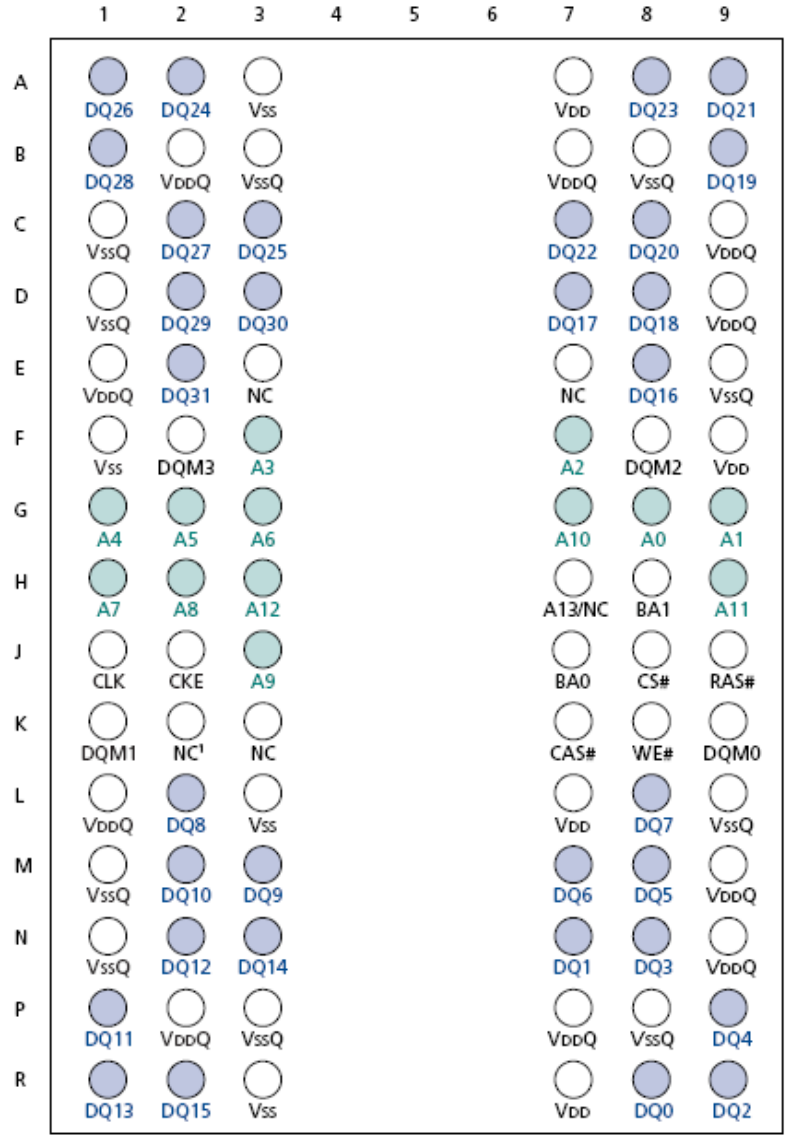
Pin Configuration – 90 balls BGA Package (x32)

< TOP View>

See the balls through the package



Notes:

1. The K2 pin must be connected to V_{SS}, V_{SSQ}, or left floating.

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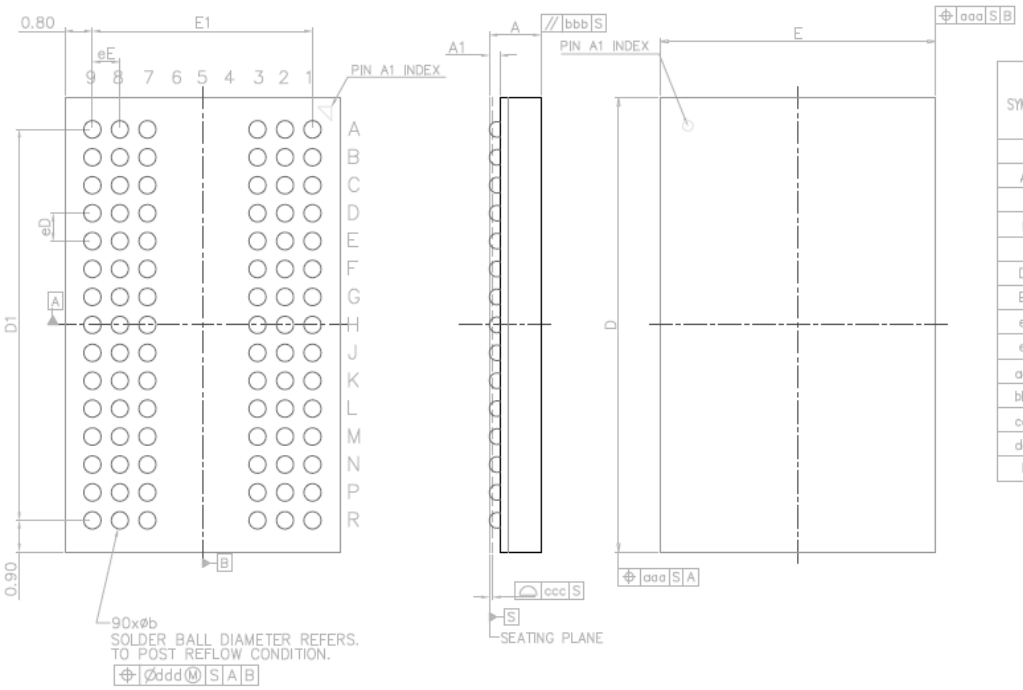
Package Dimensions (x32; 90 balls; 0.8mmx0.8mm Pitch; 8 x 13mm BGA Package)



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.86	0.93	1.00
A1	0.30	0.35	0.40
b	0.40	0.45	0.50
D	12.90	13.00	13.10
E	7.90	8.00	8.10
D1	11.2 BSC		
E1	6.40 BSC.		
eE	0.80 BSC.		
eD	0.80 BSC.		
aaa	0.15		
bbb	---	---	0.100
ccc	---	---	0.100
ddd	---	---	0.080
N	90		

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Input / Output Functional Description

Symbol	Type	Function
CLK	Input	**Clock:** Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides precharge powerdown and SELF REFRESH operation (all banks idle), active powerdown (row active in any bank), deep power-down (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power.
/CS	Input	**Chip Select:** /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/RAS, /CAS, /WE	Input	**Command Inputs:** /RAS, /CAS and /WE (along with /CS) define the command being entered.
DM For x16: LDQM, UDQM For x32: DQM0-DQM3	Input	**Input Data Mask:** DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) during a READ cycle. For x16 devices, LDQM corresponds to the data on DQ0-DQ7, UDQM corresponds to the data on DQ8-DQ15. For x32 devices, DQM0 corresponds to the data on DQ0-DQ7, DQM1 corresponds to the data on DQ8-DQ15, DQM2 corresponds to the data on DQ16-DQ23, and DQM3 corresponds to the data on DQ24-DQ31. DQM0-DQM3 (LDQM / UDQM if x16) are considered same state when referenced as DQM.
DQ For x16: DQ0-DQ15 For x32: DQ0-DQ31	Input/output	**Data Bus:** Bi-directional Input / Output data bus.
BA0, BA1	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 and BA1 become when registering an ALL BANK PRECHARGE (A10 HIGH).
A [13:0]	Input	**Address Inputs:** A[13:0] are sampled during the ACTIVE command (row-address A[13:0]) and READ/WRITE command [column-address A[8:0] (x32); column-address A[9:0] (x16); with A10 defining auto precharge] to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1. The address inputs also provide the op-code during a LOAD MODE REGISTER command.

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A13/NC	Input	**A13:** used for reduced page-size, option; otherwise, leave as NC.
NC	Input	**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** Isolated on the die for improved noise immunity.
V_{SSQ}	Supply	**DQ Ground:** Isolated on the die for improved noise immunity.
V_{DD}	Supply	**Power Supply**
V_{SS}	Supply	**Ground**

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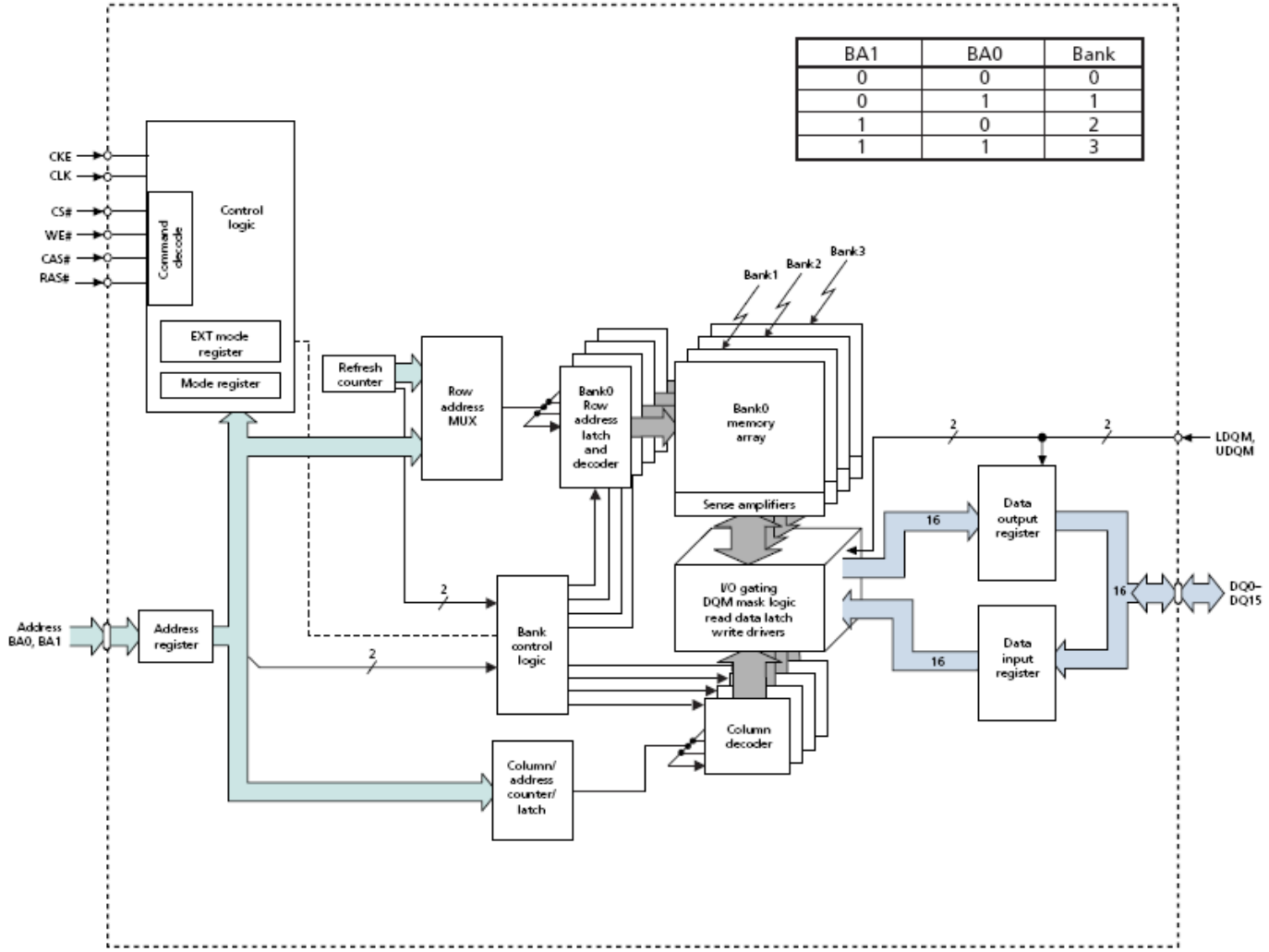
Functional Block Diagram – LPSDR 32Mx16



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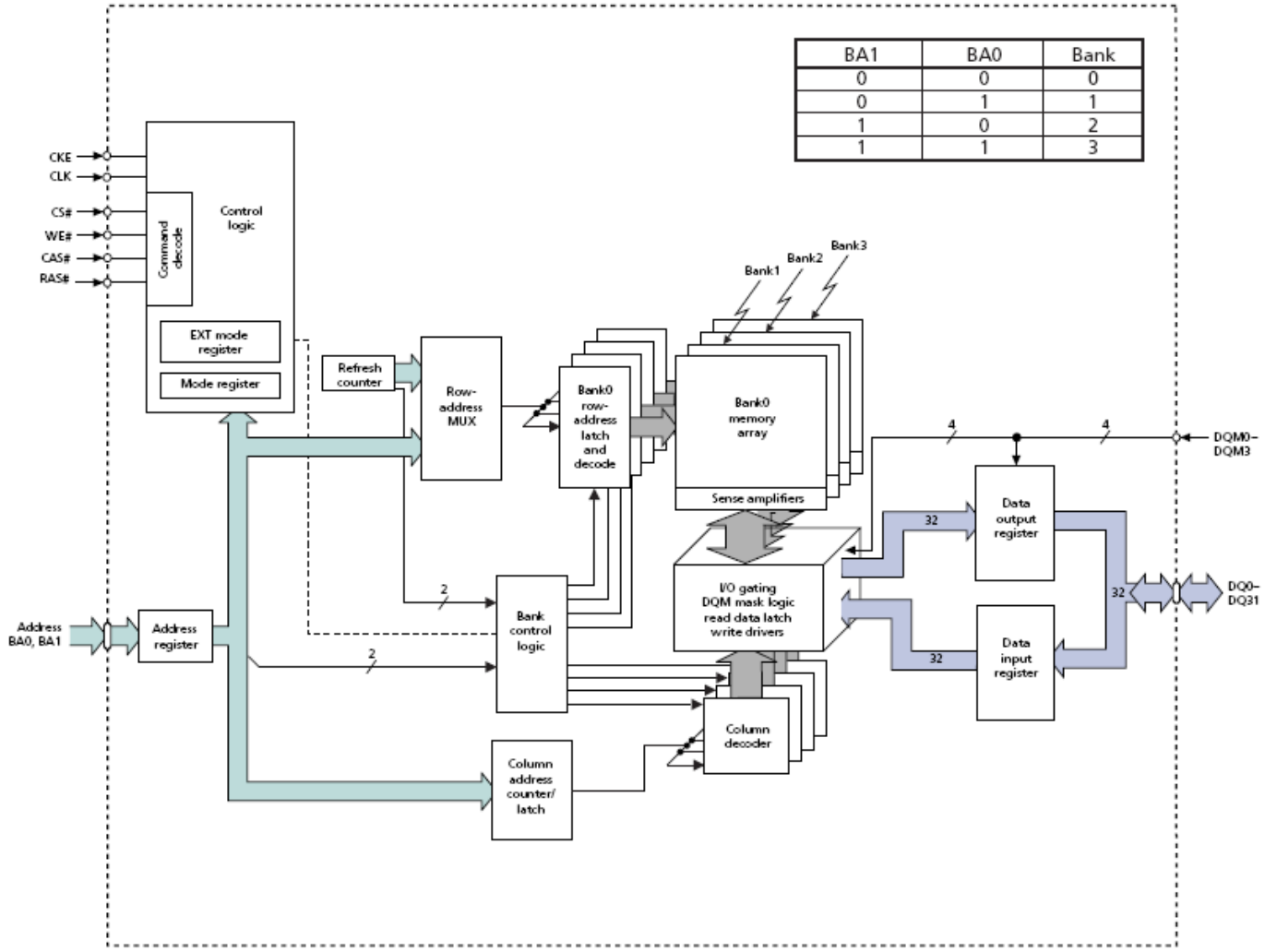
Functional Block Diagram – LPSDR 16Mx32



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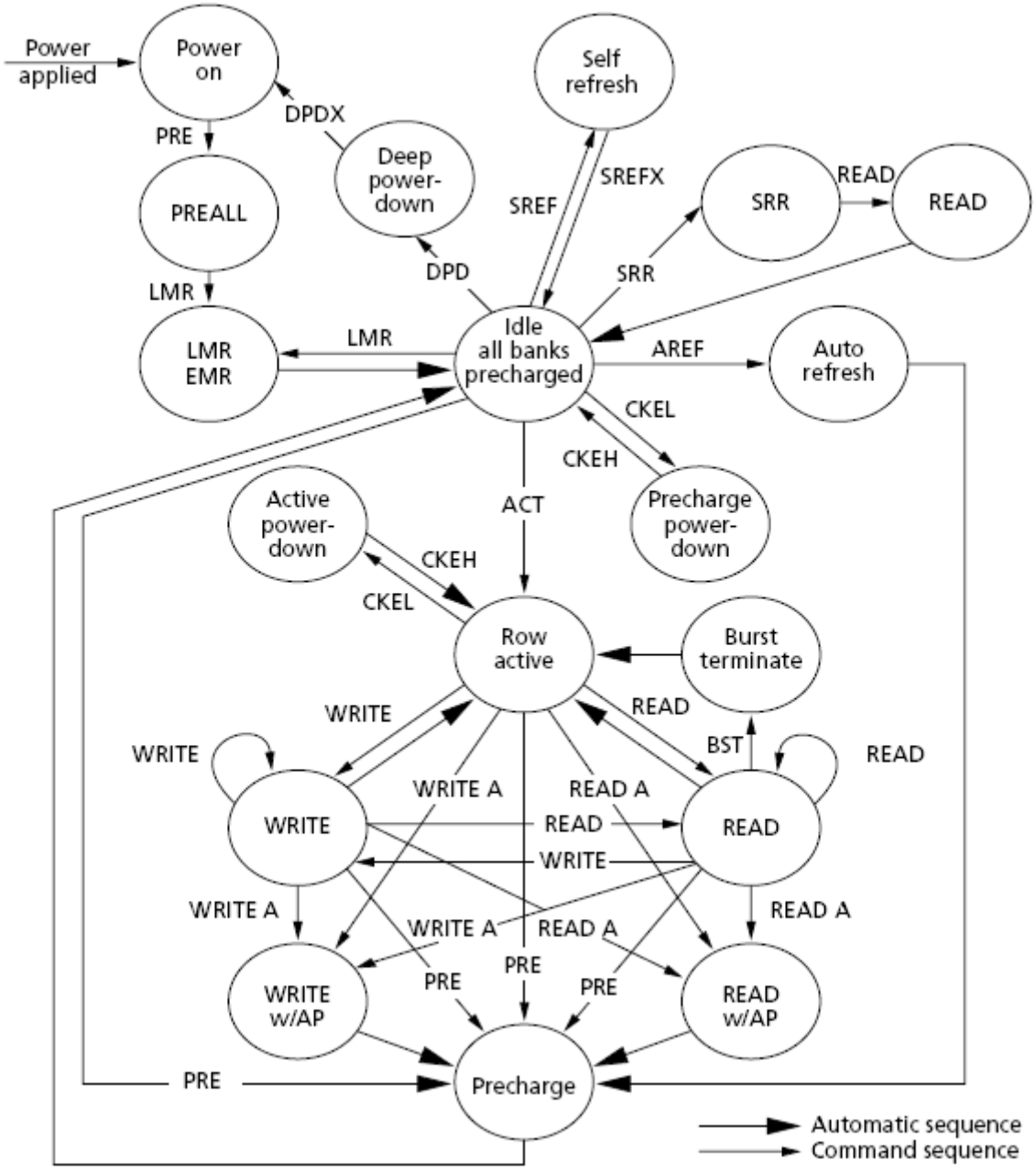
Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Active	LMR	Load mode register	PRE	Precharge
READ	Read (w/o Autoprecharge)	CKEH	Exit power-down	PREALL	Precharge all banks
READ A	Read (w/ Autoprecharge)	CKEL	Enter power-down	AREF	Auto Refresh
WRITE	Write (w/o Autoprecharge)	DPD	Enter Deep Power Down	SREF	Enter self refresh
WRITE A	Write (w/ Autoprecharge)	DPDX	Exit Deep Power Down	SREFX	Exit self refresh
EMR	Load extended mode registe	BST	Burst Terminate	SRR	Status Register Read

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Electrical Specifications

Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Units
V_{DD} / V_{DDQ}	V_{DD} / V_{DDQ} supply voltage relative to Vss	-0.5	+2.4	V
Vin	Voltage on any pin relative to Vss	-0.5	+2.4	V
Tstg	Storage Temperature (plastic)	-55	+150	°C

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Input / Output Capacitance (x16, x32)

Symbol	Parameter	Min	Max	Unit
CI1	Input capacitance: CLK	2.0	5.0	pF
CI2	Input capacitance: All other input-only balls	2.0	5.0	pF
CIO	Input/output capacitance: DQs	2.5	6.0	pF

Notes:

1. This parameter is sampled. V_{DD} /V_{DDQ} = +1.8V, T_A=25C; ball under test biased at 0.9V, f = 1MHz.

DC Electrical Characteristics and Operating Conditions

V_{DD} / V_{DDQ} = 1.70 ~ 1.95V

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply voltage	1.7	1.95	V	
V_{DDQ}	I/O Supply voltage	1.7	1.95	V	
Address and Command inputs					
V_{IH}	Input voltage high: Logic 1; All inputs	0.8 x V_{DDQ}	V_{DDQ} + 0.3	V	3
V_{IL}	Input voltage low : Logic 0 ; All inputs	-0.3	+0.3	V	3
Data outputs					
V_{OH}	Output high voltage	0.9 x V_{DDQ}	-	V	4
V_{OL}	Output low voltage	-	0.2	V	4
Leakage current					
I_I	Input leakage current:	-1.0	1.0	uA	

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	Any input 0 ≦ V_{IN} ≦ V_{DD}, (All other balls not under test = 0V)				
I_{OZ}	Output leakage current: DQs are disabled; 0 ≦ V_{OUT} ≦ V_{DDQ}	-1.5	1.5	uA	
Operating temperature					
T_A	Commercial	-25	+85	°C	
T_A	Industrial	-40	+85	°C	

Notes:

1. All voltage referenced to Vss.
2. A full initialization sequence is required before proper device operation is ensured.
3. V_{IH} overshoot: V_{IH} (MAX) = V_{DDQ} + 2V for a pulse width ≤ 3ns, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = –2V for a pulse width ≤ 3ns.
4. I_{OUT} = 4mA for full drive strength. Other drive strengths require appropriate scale..

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IDD Specifications and Measurement Conditions

32Mx16 IDD Specifications; V_{DD}/V_{DDQ} = 1.70~1.95V

Symbol	Parameter/Condition		Speed Grade		Unit	Notes
			S1(-6)	S2(-75)		
IDD1	**Operating current:** Active mode; Burst = 1; READ or WRITE; ^{t}RC=^{t}RC(min)		60	50	mA	2,3,4
IDD2P	**Standby current:** Power-down mode; All banks idle; CKE is LOW		300	300	uA	5
IDD2N	**Standby current:** Non-power-down; All banks idle; CKE is HIGH		10	10	mA	
IDD3P	**Standby current:** Active mode; CKE is LOW; /CS is HIGH; All banks active; No accesses in progress.		5	5	mA	3,4,6
IDD3N	**Standby current:** Active mode; CKE is HIGH; /CS is HIGH; All banks active after ^{t}RCD met; No accesses in progress.		20	20	mA	3,4,6
IDD4	**Operating current:** Burst mode; READ or WRITE; All banks active, half DQs toggling every cycle.		105	100	mA	2,3,4
IDD5	**Auto Refresh current:** CKE=HIGH; /CS is HIGH.	^{t}RFC = 110ns	95	95	mA	2,3,4,6
IDD5A		^{t}RFC = 7.8125us	3	3	mA	2,3,4,7
I_{ZZ}	**Deep power-down current:**		10	10	uA	5,8

16Mx32 IDD Specifications; V_{DD}/V_{DDQ} = 1.70~1.95V

Symbol	Parameter/Condition		Speed Grade		Unit	Notes
			S1(-6)	S2(-75)		
IDD1	**Operating current:** Active mode; Burst = 1; READ or WRITE; ^{t}RC=^{t}RC(min)		60	50	mA	2,3,4
IDD2P	**Standby current:** Power-down mode; All banks idle; CKE is LOW		300	300	uA	5
IDD2N	**Standby current:** Non-power-down; All banks idle; CKE is HIGH		10	10	mA	
IDD3P	**Standby current:** Active mode; CKE is LOW; /CS is HIGH; All banks active; No accesses in progress.		5	5	mA	3,4,6
IDD3N	**Standby current:** Active mode; CKE is HIGH; /CS is HIGH; All banks active after ^{t}RCD met; No accesses in progress.		20	20	mA	3,4,6
IDD4	**Operating current:** Burst mode; READ or WRITE; All banks active, half DQs toggling every cycle.		105	100	mA	2,3,4
IDD5	**Auto Refresh current:** CKE=HIGH; /CS is HIGH.	^{t}RFC = 110ns	95	95	mA	2,3,4,6
IDD5A		^{t}RFC = ^{t}REFI	3	3	mA	2,3,4,7
I_{ZZ}	**Deep power-down current:**		10	10	uA	5,8

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IDD6 Self-refresh current; V_{DD}/V_{DDQ} = 1.70~1.95V (x16 and x32)

Symbol	Parameter / Condition			Max	Unit	Notes
IDD6	**Self refresh current:** CKE=LOW; ^{t}CK=^{t}CK(min); Address and control inputs are stable; Data bus inputs are stable.	85°C	Full Array	600	uA	
			1/2 Array	480		
			1/4 Array	420		
			1/8 Array	420		
			1/16 Array	400		
		45°C	Full Array	300		
			1/2 Array	260		
			1/4 Array	250		
			1/8 Array	250		
			1/16 Array	250		

Notes:

1. A full initialization sequence is required before proper device operation is ensured.
2. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
3. The I_{DD} current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
4. Address transitions average one transition every two clocks.
5. Measurement is taken 500ms after entering into this operating mode to allow tester measuring unit settling time.
6. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid V_{IH} or V_{IL} levels.
7. CKE is HIGH during REFRESH command period ^{t}RFC else CKE is LOW.
8. Typical values at 25°C (not a maximum value).
9. Enables on-die refresh and address counters.
10. Values for IDD6 85°C full array and partial array are guaranteed for the entire temperature range. All other IDD6 values are estimated.

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Electrical Characteristics and Recommended AC Operating Conditions

V_{DD}/V_{DDQ} = 1.70~1.95V

Symbol	Parameter		S1(-6)		S2(-75)		Unit	Notes
			Min	Max	Min	Max		
Clock parameters								
^tAC	Access time from CLK (positive edge)	CL=3	-	5	-	5.4	ns	
		CL=2	-	8	-	8		
^tCK	Clock cycle time	CL=3	6	-	7.5	-	ns	6
		CL=2	9	-	9	-		
^tCH	CK high-level width		2.5	-	2.5	-	ns	
^tCL	CK low-level width		2.5	-	2.5	-	ns	
CKE input parameters								
^tCKH	CKE hold time		1	-	1	-	ns	
^tCKS	CKE setup time		1.5	-	1.5	-	ns	
Data parameters								
^tDH	Data-in hold time		1	-	1	-	ns	
^tDS	Data –in setup time		1.5	-	1.5	-	ns	
^tHZ	Data-out high-z time	CL=3	-	5	-	5.4	ns	7
		CL=2	-	8	-	8	ns	
^tLZ	Data-out Low-z time		1.0	-	1.0	-	ns	
^tOH	Data-out hold time (load)		2.5	-	2.5	-	ns	
^tOH_N	Data-out hold time (no load)		1.8	-	1.8	-	ns	
Command / Address Input parameters								
^tAH	Address hold time		1	-	1	-	ns	
^tAS	Address setup time		1.5	-	1.5	-	ns	
^tCMH	/CS, /RAS, /CAS, /WE, DQM hold time		0.5	-	0.5	-	ns	
^tCMS	/CS, /RAS, /CAS, /WE, DQM setup time		1.5	-	1.5	-	ns	
SDRAM core parameters								
^tRAS	ACTIVE to PRECHARGE command		42	120,000	45	120,000	ns	

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Symbol	Parameter		S1(-6)		S2(-75)		Unit	Notes
			Min	Max	Min	Max		
tRC	ACTIVE to ACTIVE command period		60	-	67.5	-	ns	
tRCD	ACTIVE to READ or WRITE delay		18	-	19.2	-	ns	
tRP	PRECHARGE command period		18	-	19.2	-	ns	
tRRD	ACTIVE *bank-a* to ACTIVE *bank-b* command		2	-	2	-	tCK	
tWR	Write recovery time		15	-	15	-	ns	10
tT	Transition time		0.3	1.2	0.3	1.2	ns	9
tXSR	Exit SELF REFRESH to first valid command		112.5	-	112.5	-	ns	11
tREF	Refresh period		-	64	-	64	ms	
tREFI	Average periodic refresh interval (8,192 rows)		-	7.8125	-	7.8125	us	8
tRFC	Auto Refresh command period		97.5	-	97.5	-	ns	
Other parameters								
tBDL	Last data-in to burst STOP command		1		1		tCK	12
tCCD	READ/WRITE command to READ/WRITE command		1		1		tCK	12
tCDL	Last data-in to new READ/WRITE command		1		1		tCK	13
tCKED	CKE to clock disable or power-down entry mode		1		1		tCK	13
tDAL	Data-in to ACTIVE command		5		5		tCK	14,16
tDPL	Data-in to PRECHARGE command		2		2		tCK	15,16
tDQD	DQM to input data delay		0		0		tCK	12
tDQM	DQM to data mask during WRITEs		0		0		tCK	12
tDQZ	DQM to data High-Z during READs		2		2		tCK	12
tDWD	WRITE command to input data delay		0		0		tCK	12
tMRD	LOAD MODE REGISTER command to ACTIVE or REFRESH command		2		2		tCK	
tPED	CKE to clock enable or power-down exit mode		1		1		tCK	13
tRDL	Last data-in to PRECHARGE command		2		2		tCK	15,16
tROH	Data-out High-Z from PRECHARGE command	CL=3	3		3		tCK	12
		CL=2	2		2			

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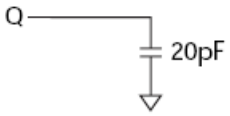
Notes:

1. A full initialization sequence is required before proper device operation is ensured.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ TA ≤ +70°C standard temperature and –40°C ≤ TA ≤ +85°C industrial temperature) is ensured.
3. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
4. Outputs measured for 1.8V at 0.9V with equivalent load:



Test loads with full DQ driver strength. Performance will vary with actual system DQ bus capacitive loading, termination, and programmed drive strength.

5. AC timing tests have VIL and Vih with timing referenced to VIH/2 = crossover point. If the input transition time is longer than tT (MAX), then the timing is referenced at VIL (MAX) and VIH (MIN) and no longer at the VIH/2 crossover point.
6. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) during access or precharge states (READ, WRITE, including tWR, and PRECHARGE commands). CKE may be used to reduce the data rate.
7. tHZ defines the time at which the output achieves the open circuit condition, it is not a reference to VOH or VOL. The last valid data element will meet tOH before going High-Z.
8. The 1Gb Mobile SDRAM requires 8,192 AUTO REFRESH cycles every 64ms (tREF). Providing a distributed AUTO REFRESH command every 7.8125µs meets the refresh requirement and ensures that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRFC), once every 64ms.
9. AC characteristics assume tT = 1ns.
10. Auto precharge mode only. The precharge timing budget (tRP) begins at *x* ns for -75 after the first clock delay and after the last WRITE is executed. May not exceed the limit set for precharge mode.
11. CLK must be toggled a minimum of two times during this period.
12. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
13. Timing is specified by tCKS. Clock(s) specified as a reference only at minimum cycle rate.
14. Timing is specified by tWR plus tRP. Clock(s) specified as a reference only at minimum cycle rate.
15. Timing is specified by tWR.
16. Based on tCK (MIN), CL = 3.

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Target Output Drive Characteristics (Full Strength)

Characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	2.8	18.53	–2.80	–18.53
0.20	5.6	26.8	–5.60	–26.80
0.30	8.4	32.8	–8.40	–32.80
0.40	11.2	37.05	–11.20	–37.05
0.50	14	40	–14.00	–40.00
0.60	16.8	42.5	–16.80	–42.50
0.70	19.6	44.57	–19.60	–44.57
0.80	22.4	46.5	–22.40	–46.50
0.85	23.8	47.48	–23.80	–47.48
0.90	23.8	48.5	–23.80	–48.50
0.95	23.8	49.4	–23.80	–49.40
1.00	23.8	50.05	–23.80	–50.05
1.10	23.8	51.35	–23.80	–51.35
1.20	23.8	52.65	–23.80	–52.65
1.30	23.8	53.95	–23.80	–53.95
1.40	23.8	55.25	–23.80	–55.25
1.50	23.8	56.55	–23.80	–56.55
1.60	23.8	57.85	–23.80	–57.85
1.70	23.8	59.15	–23.80	–59.15
1.80	–	60.45	–	–60.45
1.90	–	61.75	–	–61.75

Notes:

1. Table values based on nominal impedance of 25Ω (full-drive) at $V_{DDQ}/2$.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.

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Target Output Drive Characteristics (Three-Quarter Strength)

Characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.96	12.97	-1.96	-12.97
0.20	3.92	18.76	-3.92	-18.76
0.30	5.88	22.96	-5.88	-22.96
0.40	7.84	25.94	-7.84	-25.94
0.50	9.8	28	-9.8	-28
0.60	11.76	29.75	-11.76	-29.75
0.70	13.72	31.2	-13.72	-31.2
0.80	15.68	32.55	-15.68	-32.55
0.85	16.66	33.24	-16.66	-33.24
0.90	16.66	33.95	-16.66	-33.95
0.95	16.66	34.58	-16.66	-34.58
1.00	16.66	35.04	-16.66	-35.04
1.10	16.66	35.95	-16.66	-35.95
1.20	16.66	36.86	-16.66	-36.86
1.30	16.66	37.77	-16.66	-37.77
1.40	16.66	38.68	-16.66	-38.68
1.50	16.66	39.59	-16.66	-39.59
1.60	16.66	40.5	-16.66	-40.5
1.70	16.66	41.41	-16.66	-41.41
1.80	–	42.32	–	-42.32
1.90	–	43.23	–	-43.23

Notes:

1. Table values based on nominal impedance of 37Ω (three-quarter drive strength) at $V_{DDQ}/2$.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.
3. Contact factory for availability of three-quarter drive strength.

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Target Output Drive Characteristics (One-half Strength)

Characteristics are specified under best and worst process variation/conditions

Voltage (V)	Pull-Down Current (mA)		Pull-Up Current (mA)	
	Min	Max	Min	Max
0.00	0.00	0.00	0.00	0.00
0.10	1.27	8.42	–1.27	–8.42
0.20	2.55	12.3	–2.55	–12.30
0.30	3.82	14.95	–3.82	–14.95
0.40	5.09	16.84	–5.09	–16.84
0.50	6.36	18.2	–6.36	–18.20
0.60	7.64	19.3	–7.64	–19.30
0.70	8.91	20.3	–8.91	–20.30
0.80	10.16	21.2	–10.16	–21.20
0.85	10.8	21.6	–10.80	–21.60
0.90	10.8	22	–10.80	–22.00
0.95	10.8	22.45	–10.80	–22.45
1.00	10.8	22.73	–10.80	–22.73
1.10	10.8	23.21	–10.80	–23.21
1.20	10.8	23.67	–10.80	–23.67
1.30	10.8	24.14	–10.80	–24.14
1.40	10.8	24.61	–10.80	–24.61
1.50	10.8	25.08	–10.80	–25.08
1.60	10.8	25.54	–10.80	–25.54
1.70	10.8	26.01	–10.80	–26.01
1.80	–	26.48	–	–26.48
1.90	–	26.95	–	–26.95

Notes:

1. Table values based on nominal impedance of 55Ω (half-drive strength) at $V_{DDQ}/2$.
2. The full variation in drive current, from minimum to maximum—due to process, voltage, and temperature—will lie within the outer bounding lines of the I-V curves.
3. The I-V curve for one-quarter drive strength is approximately 50 percent of one-half drive strength.

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Basic Functionality

The 512Mb Mobile LPSDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a qual-bank DRAM.

The 512Mb chip is organized as 8Mbit x 4 banks x 16 I/O or 4Mbit x 4 banks x 32 I/O device. Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits. Each of the x32's 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits. In the reduced page-size option, each of the x32's 134,217,728-bit banks are organized as 16,384 rows by 256 columns by 32 bits. To achieve high-speed operation, our LPSDR SDRAM are quad-bank DRAM that operate at 1.8V, pipelined architecture and include a synchronous interface. The pipelined architecture enables changing the column address on every clock cycle to achieve a high-speed, fully random access. All signals are registered on the positive edge of the clock signal, CLK. Precharging one bank while accessing one of the other three banks will hide the precharge cycles and provides seamless high-speed, random access operation.

LPSDR SDRAM, Read and Write access are burst oriented. The address bits registered coincident with the ACTIVE command to select the row in the specific bank. And then the address bits registered with the READ or WRITE command to select the starting column location in the bank for the burst access. The burst length can be programmed as 1, 2, 4, 8 or 16. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of burst access.

LPSDR SDRAM with Auto Refresh mode, and the Power-down mode for power saving. And the Deep Power Down Mode can achieve the maximum power reduction by removing the memory array power within Low Power DDR SDRAM. With this feature, the system can cut off almost all DRAM power without adding the cost of a power switch and giving up month-board power-line layout flexibility. Self Refresh mode with Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR) options, which allow users to achieve additional power saving. The TCSR and PASR options can be programmed via the extended mode register. The two features may be combined to achieve even greater power saving.

All inputs are LVCMOS compatible. Devices will have a V_{DD} and V_{DDQ} supply of 1.8V (nominal).

Prior to normal operation, the LPSDR SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

LPSDR SDRAMs must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. And any interruption to the device power, the initialization routine should be followed to ensure proper functionality of the Mobile SDR SDRAM. After power is simultaneously applied to VDD and VDDQ and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

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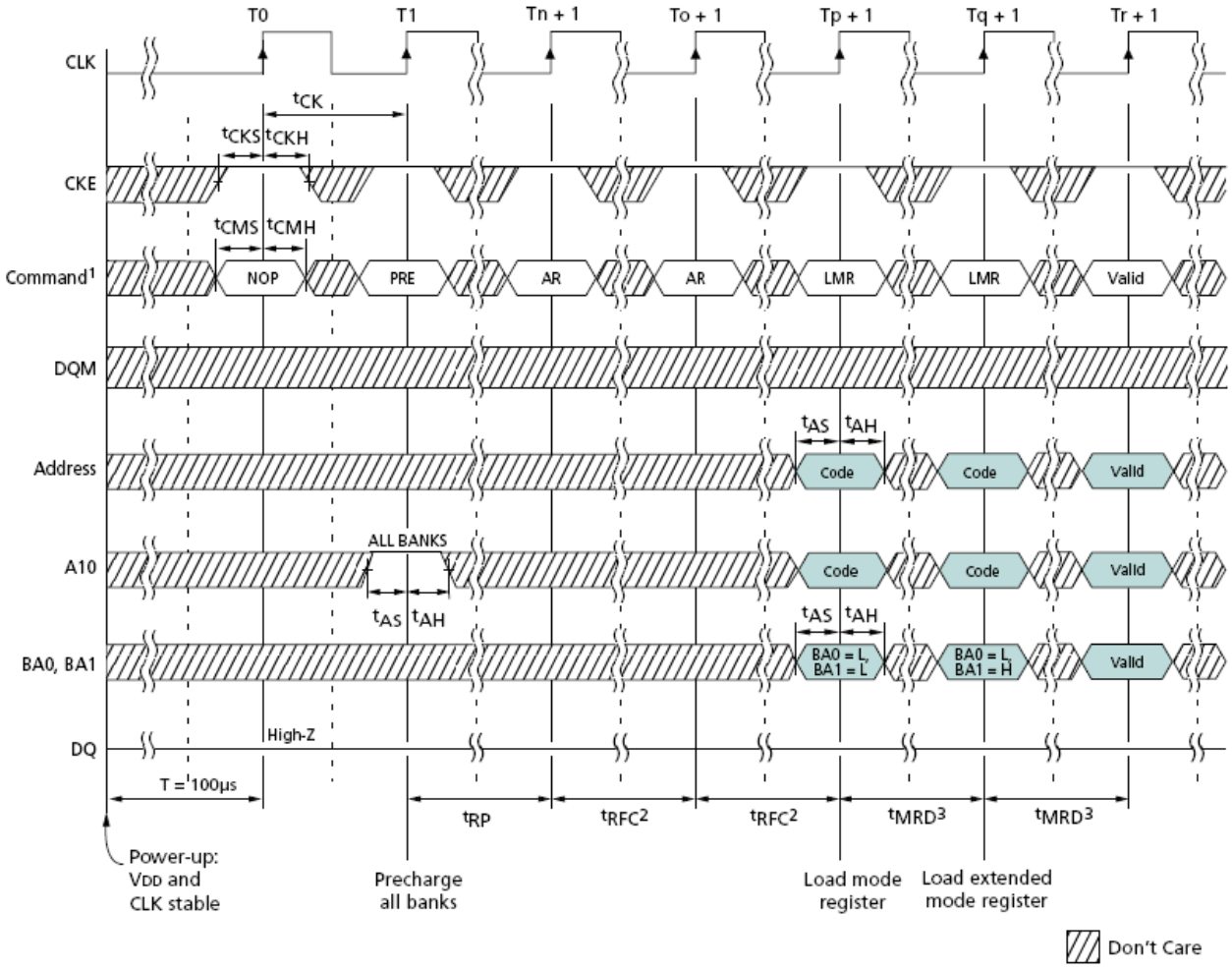
After the 100µs delay is satisfied by issuing at least one COMMAND INHIBIT or NOP command, a PRECHARGE command must be issued. All banks must then be precharged, which places the device in the all-banks-idle state. When in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the Mode registers powers up in an unknown state, it should be loaded prior to issuing any operational command.

Initialization and Load Mode Register Sequence



Notes:

1. PRE = PRECHARGE command; LMR = LOAD MODE REGISTER command; AR = AUTO REFRESH command.
2. NOPs or DESELECTs must only be provided during ^{t}RFC time.
3. NOPs or DESELECTs must only be provided during ^{t}MRD time.

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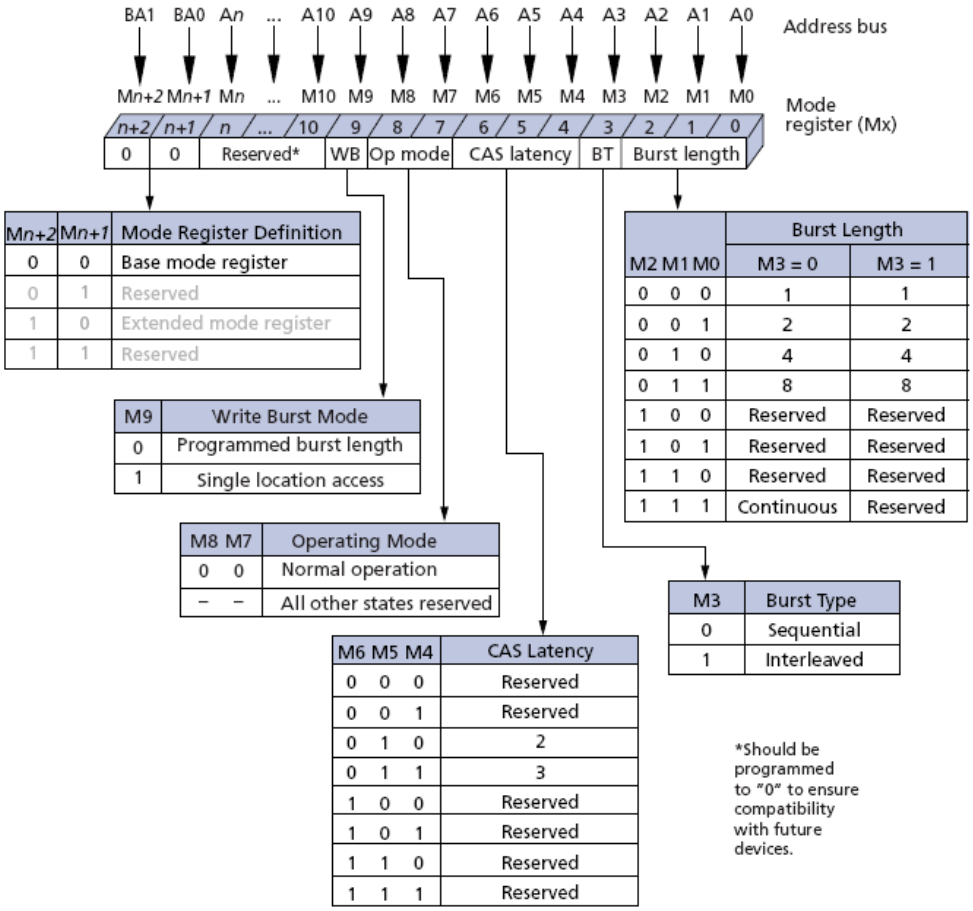
Register Definition

Mode Registers and Extended Mode Registers

The Mode Registers are used to define the specific mode of operation of the LPSDR SDRAM. This define includes the definition of a burst length, a burst type, a CAS latency, operating mode, and write burst mode. The default value of the mode register is not defined, therefore the mode register must be written after power up for proper operation. The Mode Register must be loaded when all banks are idle and no bursts are progress, and the controller must wait the specific time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. The MRS contents won't be changed until it is reprogrammed, the device goes into Deep Power-Down, or the device loses power.

The mode register is written by asserting low on /CS, /RAS, /CAS, /WE, BA0 and BA1, while controlling the state of address pins A0~A13. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on the functionality. Burst length is defined by M0~M2 with options of 1, 2, 4, 8 and continuous bit burst length. Burst address sequence type is defined by M3 and CAS latency is defined by M4~M6. M7~M8 specify the operating mode. M9 specifies the write burst mode, and M10~M*n* must be set to low to ensure future compatibility. M*n*+1~M*n*+2 should be set to zero to prevent the extended mode register from being programmed.

Standard Mode Register definition



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Burst Length, Type, and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit M3 as above figure. The ordering of access within a burst is determined by the burst length, burst type, and the starting column address. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. The burst length is defined by bits M0-M2. Burst length options include 1, 2, 4, 8 or continuous locations are available for both the sequential and the interleaved burst types. The continuous page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary BLs. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the BL is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap when a boundary is reached. The block is uniquely selected by A1–Ai when BL = 2, by A2–Ai when BL = 4, and by A3–Ai when BL = 8, where Ai is the most significant column address bit for a given configuration. The remaining (least significant) address bits are used to specify the starting location within the block. The programmed BL applies to both READ and WRITE bursts. Accesses within a given burst may be programmed to be either sequential or interleaved via the standard mode register, and the burst type is selected via bit M3.

Burst Type and Burst Order

Burst Length	Starting Column Address (A2,A1,A0)	Burst type = Sequential M3 = 0	Burst type = Interleaved M3 = 1
2	000	0,1	0,1
	001	1,0	1,0
4	000	0,1,2,3	0,1,2,3
	001	1,2,3,0	1,0,3,2
	010	2,3,0,1	2,3,0,1
	011	3,0,1,2	3,2,1,0
8	000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
	010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
	100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
	110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0
Continuous	n = A0~An/9/8 (location 0-y)	Cn, Cn+1, Cn+2, …, Cn-1, Cn…	Not supported

CAS Latency (CL)

The CAS Latency, or READ latency is the delay, in clock cycles, between the registration of a Read command and the availability of the first bit of output data. The latency can be set to two or three clocks. CAS Latency is defined by bit A6~A4 in the standard mode register. If a READ command is registered at a clock edge n, and the CAS latency is m clocks, the first data element will be valid by clock edge n+m. The DQ start driving as a result of the clock edge one cycle earlier (n + m - 1), and provided that the relevant access times are met, the data is valid by clock edge n + m. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

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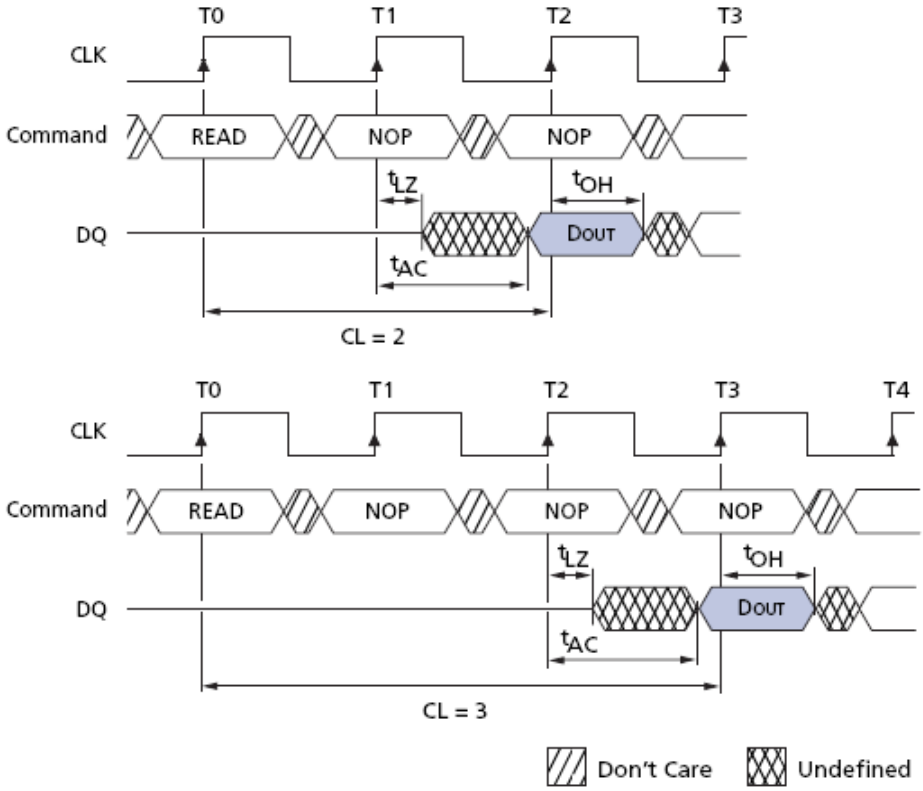

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use. Reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

When M9 = 0, the BL programmed via M[2:0] applies to both READ and WRITE bursts; when M9 = 1, the programmed BL applies to READ bursts, but write accesses are single location (nonburst) accesses.

Extended Mode Register definition

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include output drive strength selection, Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR). TCSR and PASR are effective in Self Refresh mode only. The extended mode register is programmed via the LMR (LOAD MODE REGISTER) command with BA0=0 and BA1=1, and the information won't be changed until it is reprogrammed, the device goes into deep power-down mode, or the device loses power. The EMRS must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time ^{t}MRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation. Address bits A0-A2 specify PASR, A3-A4 the TCSR, A5-A6 the Drive Strength. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.

Temperature Compensated Self Refresh (TCSR)

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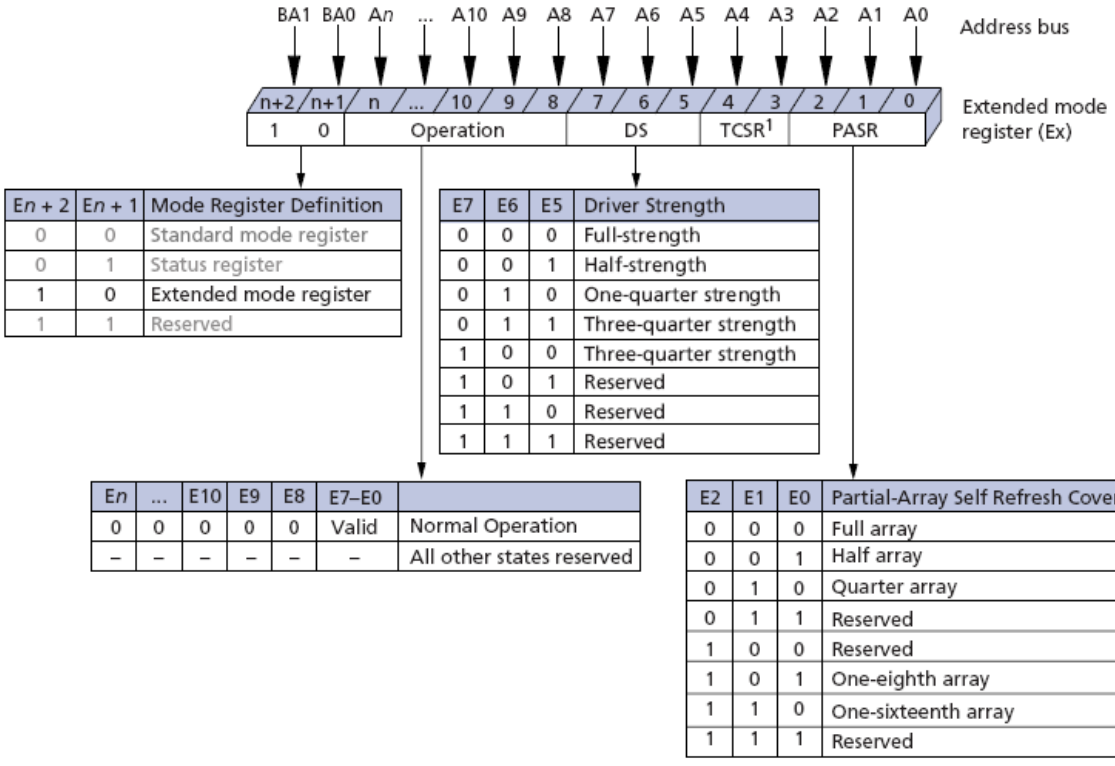
On this version of the LPSDR SDRAM, the internal temperature sensor is implemented to adjust the self refresh oscillator automatically base on the case temperature. To maintain backward compatibility, the programming of TCSR bits no effect on the device. The self refresh oscillator will continue refresh at the optimal factory-programmed rate for the device temperature. The address bits, A3 and A4 are ignore (don't care) during EMRS programming.

Partial-Array Self Refresh (PASR)

For further power savings during self refresh, the PASR feature may allow the self refresh to be restricted to a variable portion of the total array. They are full array (default: banks 0, 1, 2, and 3), 1/2 array (banks 0 and 1), 1/4 array (bank 0), 1/8 array (bank 0 with row address MSB=0), and 1/16 array (bank 0 with row address MSB=0, and row address MSB-1=0). Data outside the defined area will be lost. Address bits A0 to A2 are used to set PASR. WRITE and READ commands can still be issued to any bank selected during standard operation, but only the selected banks or segments of a bank in PASR are refreshed during self refresh. It is important to note that data in unused banks or portions of banks is lost when PASR is used.

Output Drive Strength

LPSDR SDRAM provides the option to control the drive strength of the output buffers for the smaller systems or point-to-point environments. The value was selected based on the expected loading of the memory bus. Total four values provided, and they are 25 ohm, 37ohm, 55ohm, and 80ohm internal impedance. They are full, three-quarter, one-half, and one-quarter drive strengths, respectively.



En + 2	En + 1	Mode Register Definition
0	0	Standard mode register
0	1	Status register
1	0	Extended mode register
1	1	Reserved

E7	E6	E5	Driver Strength
0	0	0	Full-strength
0	0	1	Half-strength
0	1	0	One-quarter strength
0	1	1	Three-quarter strength
1	0	0	Three-quarter strength
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

En	...	E10	E9	E8	E7–E0	
0	0	0	0	0	Valid	Normal Operation
–	–	–	–	–	–	All other states reserved

E2	E1	E0	Partial-Array Self Refresh Coverage
0	0	0	Full array
0	0	1	Half array
0	1	0	Quarter array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	One-eighth array
1	1	0	One-sixteenth array
1	1	1	Reserved

Extended Mode Register

Notes: 1. On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.

LPSDR SDRAM Command Description and Operation

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Command Truth Table

NANE (Function)	Abbreviation	/CS	/RAS	/CAS	/WE	DQM	ADDR	DQ	NOTES
DESELECT	DESELECT	H	X	X	X	X	X	X	
NO OPERATION	NOP	L	H	H	H	X	X	X	
ACTIVE (select bank and active row)	ACT	L	L	H	H	X	Bank/Row	X	2
READ (select bank, column, and start read burst)	READ	L	H	L	H	L/H	Bank/Col	X	3
WRITE (select bank, column, and start write burst)	WRITE	L	H	L	L	L/H	Bank/Col	Valid	3
WRITE with AP (write burst with Auto Precharge)	WRITEA	L	H	L	L	Valid	H	Col	3
BURST TERMINATE or enter Deep Power-Down	BST	L	H	H	L	X	X	X	4,5
PRECHARGE (deactive row in selected bank)	PRE	L	L	H	L	X	Code	X	6
AUTO REFRESH or enter SELF REFRESH	REFA / REFS	L	L	L	H	X	X	X	7,8
LOAD MODE REGISTER	LMR	L	L	L	L	X	Op-code	X	9
Write enable/output enable		X	X	X	X	L	X	Active	10
Write inhibit/output High-Z		X	X	X	X	H	X	High-Z	10

Notes:

1. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.
2. A[0:n] provide row address (where An is the most significant address bit), BA0 and BA1 determine which bank is made active.
3. A[0:i] provide column address (where i = the most significant column address for a given device configuration). A10 HIGH enables the auto precharge feature (non-persistent), while A10 LOW disables the auto precharge feature. BA0 and BA1 determine which bank is being read from or written to.
4. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.
5. The purpose of the BURST TERMINATE command is to stop a data burst, thus the command could coincide with data on the bus. However, the DQ column reads a “Don’t Care” state to illustrate that the BURST TERMINATE command can occur when there is no data present.
6. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: all banks precharged and BA0, BA1 are “Don’t Care.”.
7. This command is AUTO REFRESH is CKE is High, and SELF REFRESH if CKE is Low.
8. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
9. A[11:0] define the op-code written to the mode register.
10. Activates or deactivates the DQ during WRITEs (zero-clock delay) and READs (two-clock delay).

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CKE Truth Table

Current State	CKE		Command (n) /RAS, /CAS, /WE, /CS	Action (n) -Result	Notes
	Previous Cycle (n-1)	Current Cycle (n)			
Power Down	L	L	X	Maintain Power Down	
Self Refresh	L	L	X	Maintain Self Refresh	
Clock suspend	L	L	X	Maintain clock suspend	
Deep Power Down	L	L	X	Maintain Deep Power Down	
Power Down	L	H	NOP or DESELECT	Exit Power Down	5
Self Refresh	L	H	NOP or DESELECT	Exit Self Refresh	6
Deep Power Down	L	H	X	Exit Deep Power Down	7
Clock suspend	L	H	X	Exit clock suspend	
All Banks Idle	H	L	NOP or DESELECT	Precharge Power Down Entry	
All Banks Idle	H	L	BURST TERMINATE	Deep Power Down Entry	8
All Banks Idle	H	L	AUTO REFRESH	Self Refresh Entry	
Reading or Writing	H	L	VALID	Clock suspend entry	
See the other Truth Tables	H	H	See the other Truth Tables		

Notes:

1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of the SDRAM immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is a result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. Exiting power-down at clock edge n will put the device in the all-banks-idle state in time for clock edge n + 1 (provided that ^{t}CKS is met).
6. Exiting self refresh at clock edge n will put the device in the all-banks-idle state after ^{t}XSR is met. COMMAND INHIBIT or NOP commands should be issued on any clock edges occurring during the ^{t}XSR period. A minimum of two NOP commands must be provided during the ^{t}XSR period.
7. After exiting clock suspend at clock edge n, the device will resume operation and recognize the next command at clock edge n + 1.
8. Deep power-down is a power-saving feature of this Mobile SDRAM device. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW..

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Current State Bank n Truth Table (command to Bank n)

Current State	Command					Action (n) -Result	Notes
	/CS	/RAS	/CAS	/WE	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous operation	
	L	H	H	H	NOP	Continue previous operation	
Idle	L	L	H	H	ACTIVE	Select and Active row	
	L	L	L	H	AUTO REFRESH	Auto refresh	7
	L	L	L	L	LMR	Load Mode register set	7
	L	L	H	L	PRE	Precharge	11
Row Active	L	H	L	H	READ	Select column & start read burst	10
	L	H	L	L	WRITE	Select column & start write burst	10
	L	L	H	L	PRECHARGE	Deactive row in bank or banks	8
READ (AP disable)	L	H	L	H	READ	Select column & start new read burst	10
	L	H	L	L	WRITE	Select column & start write burst	10
	L	L	H	L	PRECHARGE	Truncate read burst, start precharge	8
	L	H	H	L	BURST TERMINTE	Burst terminate	9,10
WRITE (AP disable)	L	H	L	H	READ	Select column & start read burst	10
	L	H	L	L	WRITE	Select column & start new write burst	10
	L	L	H	L	PRECHARGE	Truncate write burst, start precharge	8
	L	H	H	L	BURST TERMINTE	Truncate write burst, start precharge	9,10

Notes:

1. The Table applies when both CKEn-1 and CKE are HIGH, and after ^{t}XSR or ^{t}XP has been met if the previous state was self refresh or Power Down.
2. This table is bank-specific, except where noted; i.e., the current state is for a specific bank and the commands shown can be issued to that bank when in that state. Exceptions are covered in the notes below..
3. Current State Definitions:
   - Idle: The bank has been precharged, and the ^{t}RP has been met.
   - Row Active: A row in the bank has been activated, and ^{t}RCD had been met. No data bursts/accesses, register accesses in progress
   - Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   - Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or supported commands to the other bank, should be issued on any clock edge occurring during these states. Supported commands to any other bank are determined by that bank's current state.
   - Precharging: Starts with registration of a PRECHARGE command, ends when ^{t}RP is met. Then the bank will be in idle state.
   - Row Activating: Starts with registration of an AVTIVE command, ends when ^{t}RCD is met Then the bank will be in row active

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state

Read w/ AP enabled: Start with registration of a READ command with auto precharge enabled, ends when ^{t}RP has been met. Then the bank will be in the idle state.

Write w/ AP enabled: Start with registration of a WRITE command with auto precharge enabled, ends when ^{t}RP has been met. Then the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; DESELECT or NOP commands must be applied on each positive clock edge during these states.

   Refreshing: Starts with registration of an AUTO REFRESH command, ends when ^{t}RFC is met. Then all banks will be in idle state.

   Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command, ends when ^{t}MRD is met. Then all banks will be in idle state.

   Precharging All: Starts with registration of a PRECHARGE ALL command, ends when ^{t}RP is met. Then all banks will be in idle state

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. May or may not be bank specific; if all banks are to be precharged, each must be in a valid state for precharging.
9. This command is BURST TERMINATE when CKE is HIGH and DEEP POWER-DOWN when CKE is LOW.
10. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Does not affect the state of the bank and acts as a NOP to that bank.

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Current State Bank n Truth Table (command to Bank m)

Current State	Command					Action (n) -Result	Notes
	/CS	/RAS	/CAS	/WE	Description		
Any	H	X	X	X	DESELECT (NOP)	Continue previous operation	
	L	H	H	H	NOP	Continue previous operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	7
	L	H	L	L	WRITE	Select column & start write burst	7
	L	L	H	L	PRECHARGE	Precharge	
READ (AP disable)	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	7,10
	L	H	L	L	WRITE	Select column & start write burst	7,11
	L	L	H	L	PRECHARGE	Precharge	9
WRITE (AP disable)	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	7,12
	L	H	L	L	WRITE	Select column & start write burst	7,13
	L	L	H	L	PRECHARGE	Precharge	9
Read (AP enabled)	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	7,8,14
	L	H	L	L	WRITE	Select column & start write burst	7,8,15
	L	L	H	L	PRECHARGE	Precharge	9
Write (AP enabled)	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	7,8,16
	L	H	L	L	WRITE	Select column & start write burst	7,8,17
	L	L	H	L	PRECHARGE	Precharge	9

Notes:

1. The Table applies when both CKEn-1 and CKE are HIGH, and after ^{t}XSR or ^{t}XP has been met if the previous state was self refresh or Power Down.
2. This table describes alternate bank operation, except where noted; i.e., the current state is for bank n and the commands shown can be issued to bank m (assuming that bank m is in such a state that the given command is supported). Exceptions are covered in the notes below.
3. Current State Definitions:
   - Idle: The bank has been precharged, and the ^{t}RP has been met.
   - Row Active: A row in the bank has been activated, and ^{t}RCD had been met. No data bursts/accesses, register accesses in progress
   - Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

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Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

Read w/ AP: Starts with registration of a READ command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

Write w/ AP: Starts with registration of a WRITE command with auto precharge enabled and ends when ^{t}RP has been met. After ^{t}RP is met, the bank will be in the idle state.

4. AUTO REFRESH, SELF REFRESH, and LOAD MODE REGISTER commands may only be issued when all banks are idle.

5. A BURST TERMINATE command can not be issued to another bank; it applies to the bank represented by the current state only.

6. All states and sequences not shown are illegal or reserved.

7. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.

8. Concurrent auto precharge: Bank n will initiate the auto precharge command when its burst has been interrupted by bank m burst.

9. The burst in bank n continues as initiated.

10. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank m will interrupt the READ on bank n, CAS latency (CL) later.

11. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank m will interrupt the READ on bank n when registered. DQM should be used one clock prior to the WRITE command to prevent bus contention.

12. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank m will interrupt the WRITE on bank n when registered, with the data-out appearing CL later. The last valid WRITE to bank n will be data-in registered one clock prior to the READ to bank m.

13. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank m will interrupt the WRITE on bank n when registered. The last valid WRITE to bank n will be data-in registered one clock prior to READ to bank m.

14. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank m will interrupt the READ on bank n, CL later. The PRECHARGE to bank n will begin when the READ to bank m is registered.

15. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank m will interrupt the READ on bank n when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank n will begin when the WRITE to bank m is registered.

16. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank m will interrupt the WRITE on bank n when registered, with the data-out appearing CL later. The PRECHARGE to bank n will begin after tWR is met, where tWR begins when the READ to bank m is registered. The last valid WRITE bank n will be data-in registered one clock prior to the READ to bank m.

17. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank m will interrupt the WRITE on bank n when registered. The PRECHARGE to bank n will begin after ^{t}WR is met, where ^{t}WR begins when the WRITE to bank m is registered. The last valid WRITE to bank n will be data registered one clock to the WRITE to bank m.

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COMMAND

NO OPERATION (NOP)

The No operation (NOP) command is used to instruct the selected LPSDR SDRAM to perform a NOP. This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

DESELECT

The Deselect function (/CS=HIGH) prevents new commands from being executed by the LPSDR SDRAM. Operations already in progress are not affected.

LOAD MODE REGISTER (LMR)

The mode registers are loaded via the address inputs and can only be issued when all banks are idle, no bursts are in progress. The subsequent executable command can not be issued until ^{t}MRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 inputs selects the bank, and the address provided selects the row. This row remains activate (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the READ burst; if auto precharge is not selected, the row remains open for subsequent accesses. Read data appears on the DQ subject to the logic level on the DQM inputs two clocks earlier. If a given DQM signal was registered HIGH, the corresponding DQ will be High-Z two clocks later; if the DQM signal was registered LOW, the DQ will provide valid data.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The values on the BA0 and BA1 inputs select the bank; the address provided selects the starting column location. The value on input A10 determines whether auto precharge is used. If auto precharge is selected, the row being accessed is precharged at the end of the write burst; if auto precharge is not selected, the row remains open for subsequent accesses. Input data appearing on the DQ is written to the memory array subject to the DQM input logic level appearing coincident with the data. If a given DQM signal is registered LOW, the corresponding data is written to memory; if the DQM signal is registered HIGH, the corresponding data inputs are ignored and a WRITE is not executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (^{t}RP) after the precharge command is issued. Input A10 determines whether

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one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0 and BA1 select the bank. Otherwise BA0 and BA1 are treated as “Don’t Care.” After a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function, but without requiring an explicit command. This is accomplished by using A10 (A10=High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst.

BURST TERMINATE

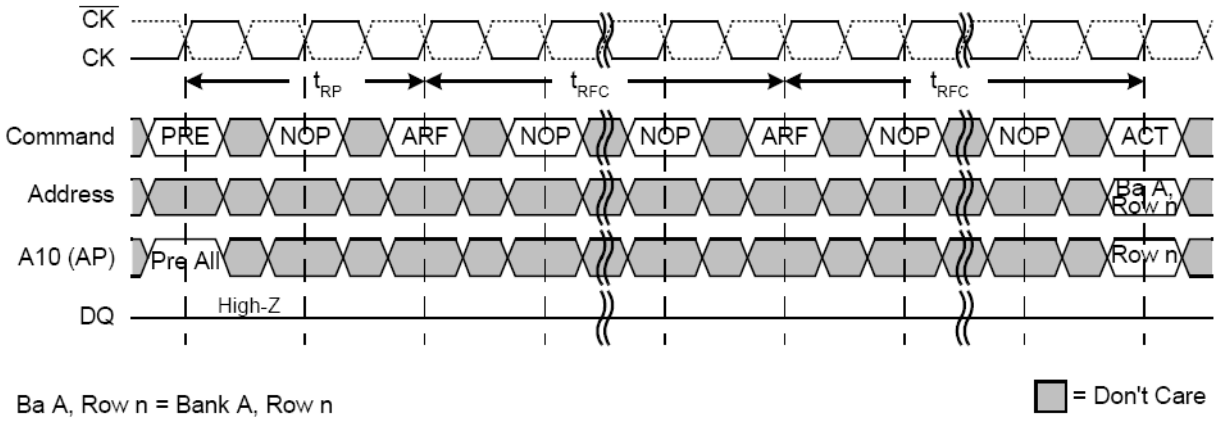
The BURST TERMINATE command is used to truncate either fixed-length or continuous page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated.

REFRESH

LPSDR SDRAM devices require a refresh of all rows in any rolling 64ms interval. Each refresh is generated in one of two ways: by an explicit AUTO REFRESH command, or by an internally timed event in SELF REFRESH mode:

- AUTO REFRESH

AUTO REFRESH command is used during normal operation of the LPSDR SDRAM, and it’s non-persistent, so it must be issued each time a refresh is required. The refresh addressing is generated by the internal refresh controller. The address bits become “Don’t Care” during AUTO REFRESH. The LPSDR SDRAM requires AUTO REFRESH commands at an average periodic interval of ^{t}REFI. To provide improved efficiency in scheduling and switching between tasks, some flexibility in the absolute interval is provided. The auto refresh period begins when the AUTO REFRESH command is registered and ends ^{t}RFC later.



- SELF REFRESH

SELF REFRESH command can be used to retain data in the LPSDR SDRAM, even if the rest of the system is powered down. When in the self refresh mode, the LPSDR SDRAM retains data without external clocking. The LPSDR SDRAM device has a built-in timer to accommodate Self Refresh operation. The SELF REFRESH command is initiated like an AUTO REFRESH

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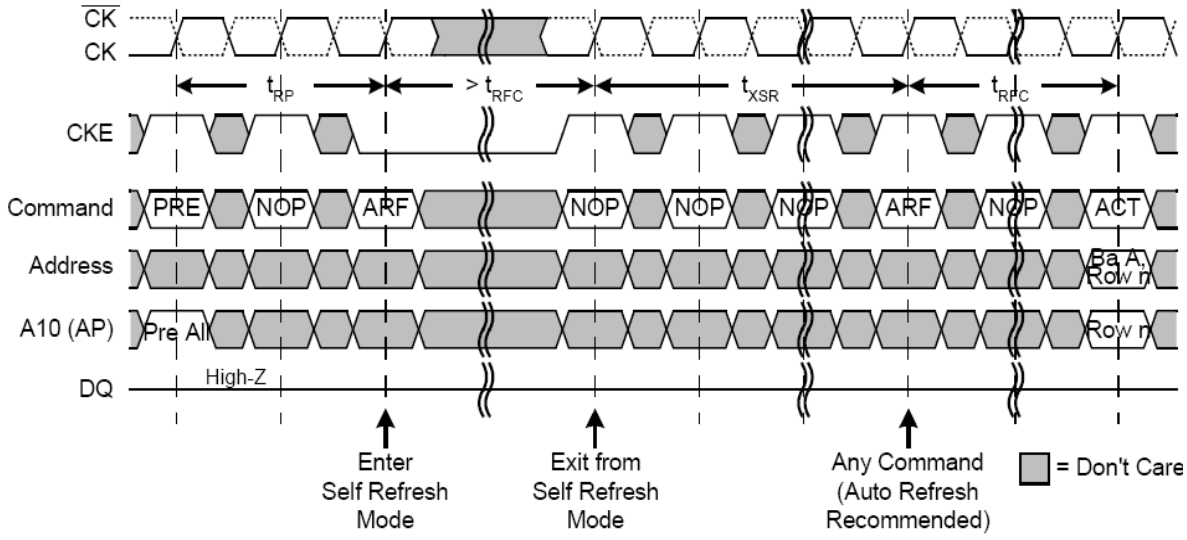
command, except CKE is LOW. Input signals except CKE are “Don’t Care” during Self Refresh. Once the SELF REFRESH command is registered, the external clock can be halted after one clock later. CKE must be held low to keep the device in Self Refresh mode, and internal clock also disabled to save power. The minimum time that the device must remain in Self Refresh mode is ^{t}RFC.

In the Self Refresh mode, two additional power-saving options exist: Temperature Compensated Self Refresh and Partial Array Self Refresh. During this mode, the device is refreshed as identified in the extended mode register. An internal temperature sensor will adjust the refresh rate to optimize device power consumption while ensuring data integrity. During SELF REFRESH operation, refresh intervals are scheduled internally and may vary. These refresh intervals may be different then the specified ^{t}REFI time. For this reason, the SELF REFRESH command must not be used as a substitute for the AUTO REFRESH command.

The procedure for exiting SELF REFRESH requires a sequence of commands. First, CK must be stable prior to CKE going back HIGH. When CKE is HIGH, the LPDDR SDRAM must have NOP commands issued for ^{t}XSR time.



Power-Down

Power-down is entered when CKE is registered Low (no accesses can be in progress). If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Power-down mode deactivates the input and output buffers, excluding CK, /CK and CKE. CKE keep Low to maintain device in the power-down mode, and all other inputs signals are “Don’t Care”. The minimum power-down duration is specified by ^{t}CKE. The device can not stay in this mode for longer than the refresh requirements of the device, without losing data. The power-down state is synchronously existed when CKE is registered High (along with a NOP or DESELECT command). A valid command can be issued after ^{t}XP after exist from power-down.

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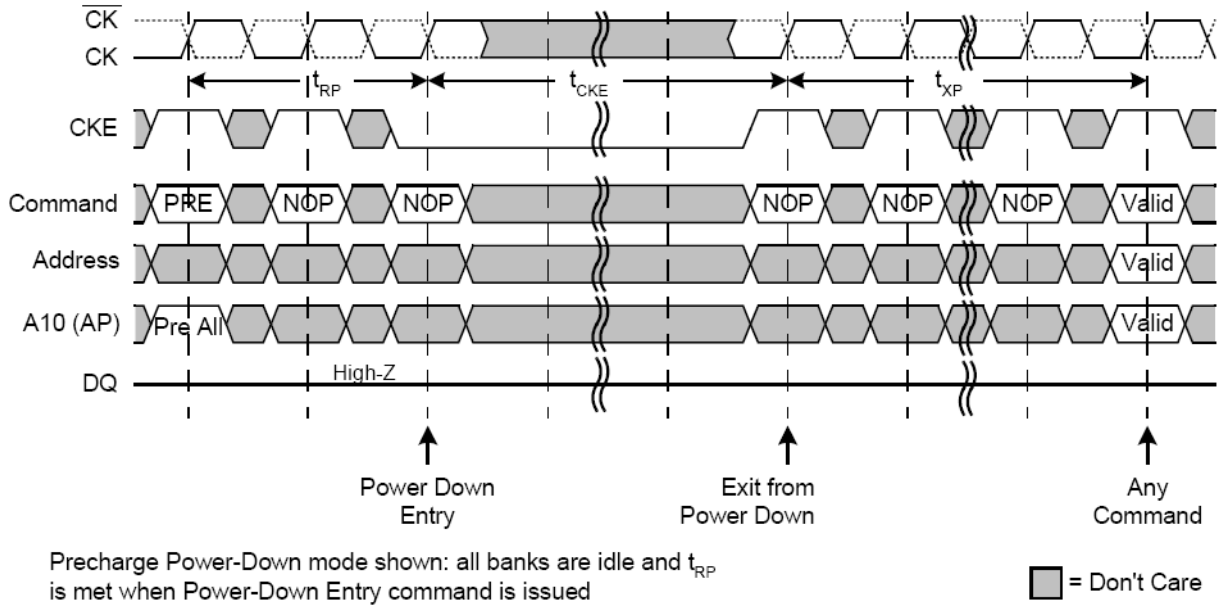
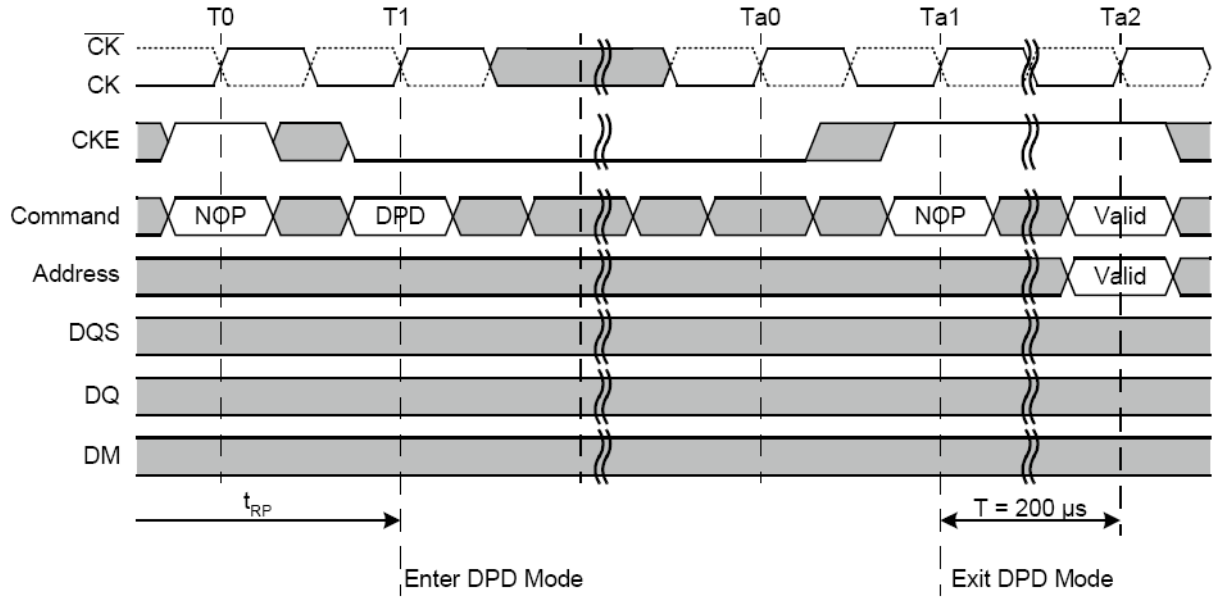


Precharge Power-Down mode shown: all banks are idle and t_{RP} is met when Power-Down Entry command is issued

Deep-Power-Down

The Deep Power-Down (DPD) mode enables very low standby currents. All internal voltage generators inside the LPSDR SDRAM are stopped and all memory data, MRS and EMRS information is lost in this mode. The DPD command is the same as a BURST TERMINATE command with CKE LOW. All banks must be in idle state with no activity on the data bus prior to entering the DPD mode. While in this mode, CKE must be held in a constant Low state. To exit the DPD mode, CKE is taken high after the clock is stable and NOP commands must be maintained for at least 200us. After 200us a complete re-initialization is required.



1) Clock must be stable before exiting Deep Power-Down mode. That is, the clock must be cycling within specifications by Ta0
2) Device must be in the all banks idle state prior to entering Deep Power-Down mode
3) 200µs is required before any command can be applied upon exiting Deep Power-Down mode
4) Upon exiting Deep Power-Down mode a PRECHARGE ALL command must be issued, followed by two AUTO REFRESH commands and a load mode register sequence

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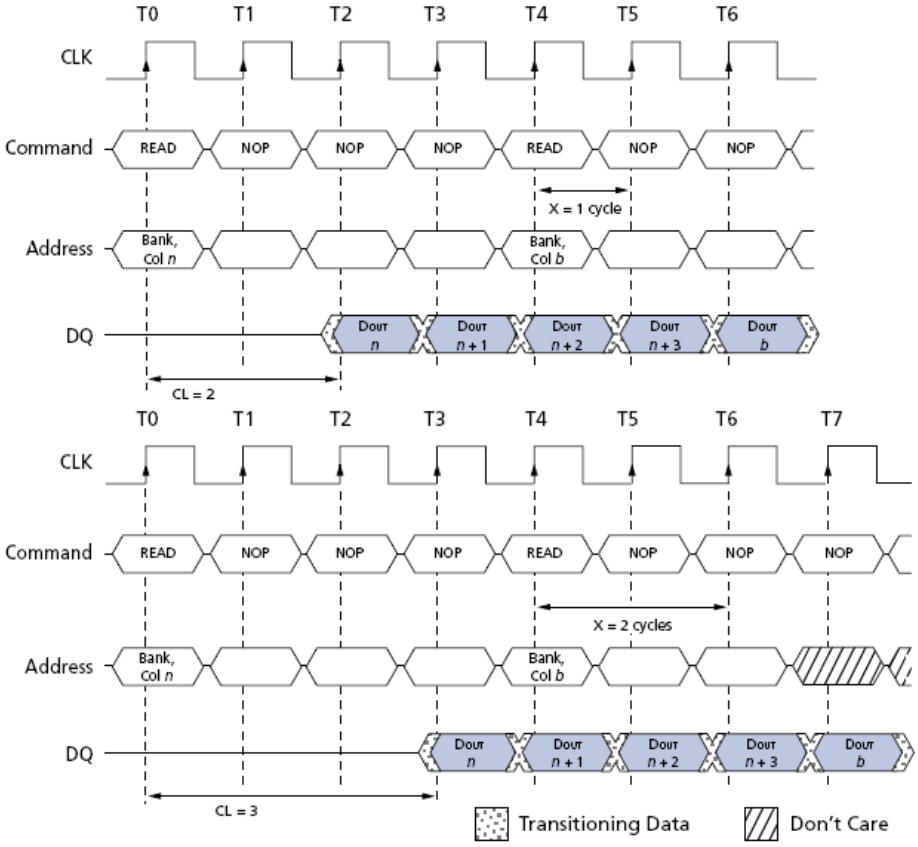
Timing Diagrams

READs

READ burst operations are initiated with a READ command. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. The first data-out element is edge aligned with the first rising edge of DQS and the successive data-out elements are edge aligned to successive edges of DQS. DQS is driven by LPSDR SDRAM along with output data. Upon completion of a read burst, assuming no other READ command has been initiated, the DQ will go to High-Z.

READ to READ

Data from any READ burst can be truncated with a subsequent READ command, and data from a fixed-length READ burst can be followed immediately by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst either follows the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued x cycles before the clock edge at which the last desired data element is valid, where x = CL - 1. LPSDR SDRAM devices use a pipelined architecture and therefore do not require the 2n rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, or each subsequent READ can be performed to a different bank.



Consecutive Read Bursts (CL=2 and CL=3)

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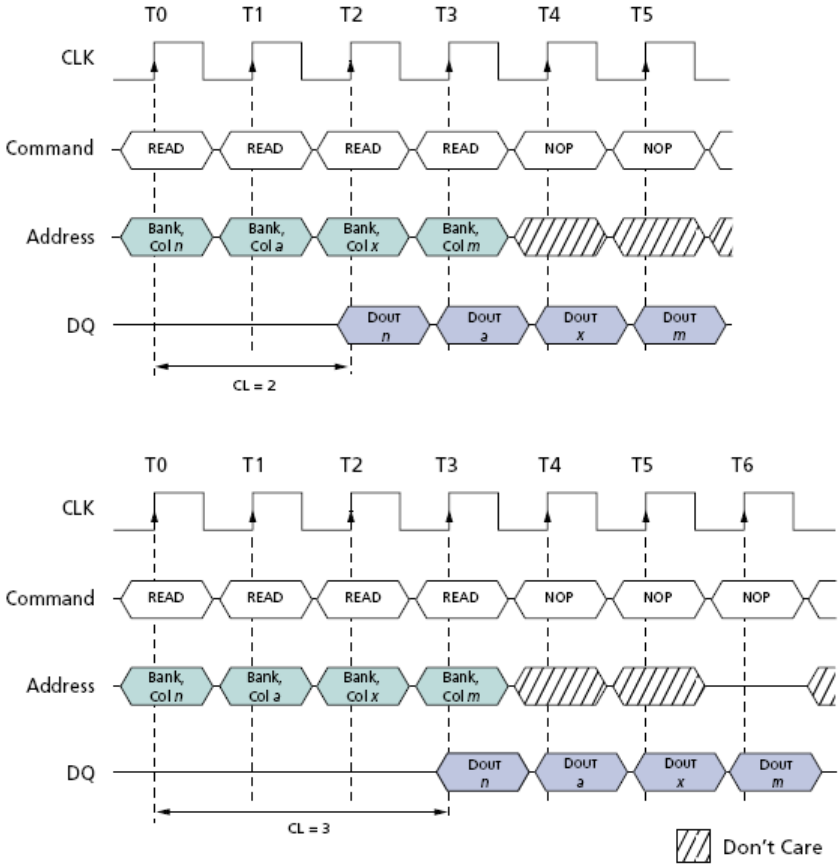
Notes:

1. Each READ command can be to any bank. DQM is LOW.



Random Read Access (CL=2 and CL=3)

Notes:

1. Each READ command can be to any bank. DQM is LOW.

READ to WRITE

Data from any READ burst can be truncated with a subsequent WRITE command, and data from a fixed-length READ burst can be followed immediately by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst can be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there is a possibility that the device driving the input data will go Low-Z before the SDRAM DQ go to High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

The DQM input is used to avoid I/O contention. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data out from the READ. After the WRITE command is registered, the DQ will go to High-Z (or remain at High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

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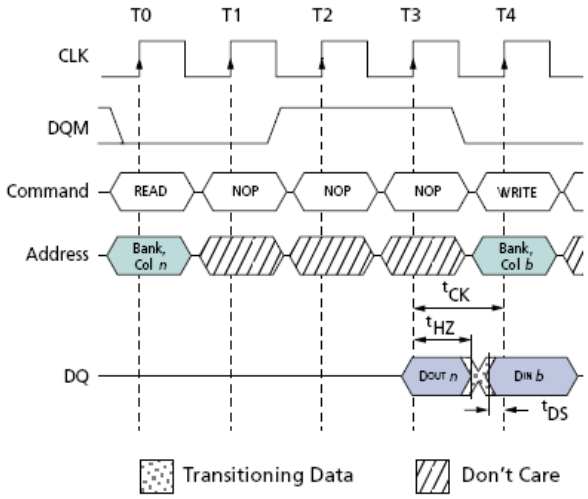
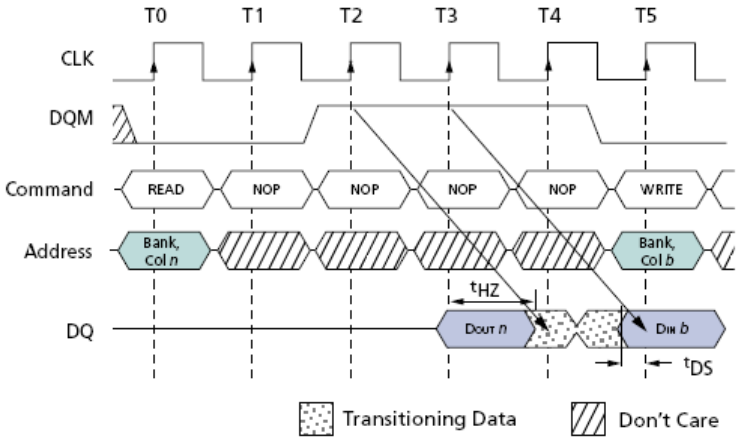


Read to Write (CL=3)

Notes:

1. CL=3. The READ command can be to any bank, and the WRITE command can be to any bank. If a burst of one is used, DQM is not required.



Read to Write with Extra Clock Cycle (CL=3)

Notes:

1. CL=3. The READ command can be to any bank, and the WRITE command can be to any bank.

READ to Precharge

A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated). The PRECHARGE command should be issued x cycles before the clock edge at which the last desired data element is valid, where x = CL - 1. The data element n + 3 is either the last of a burst of four or the last desired data element of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command. However, the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or continuous page

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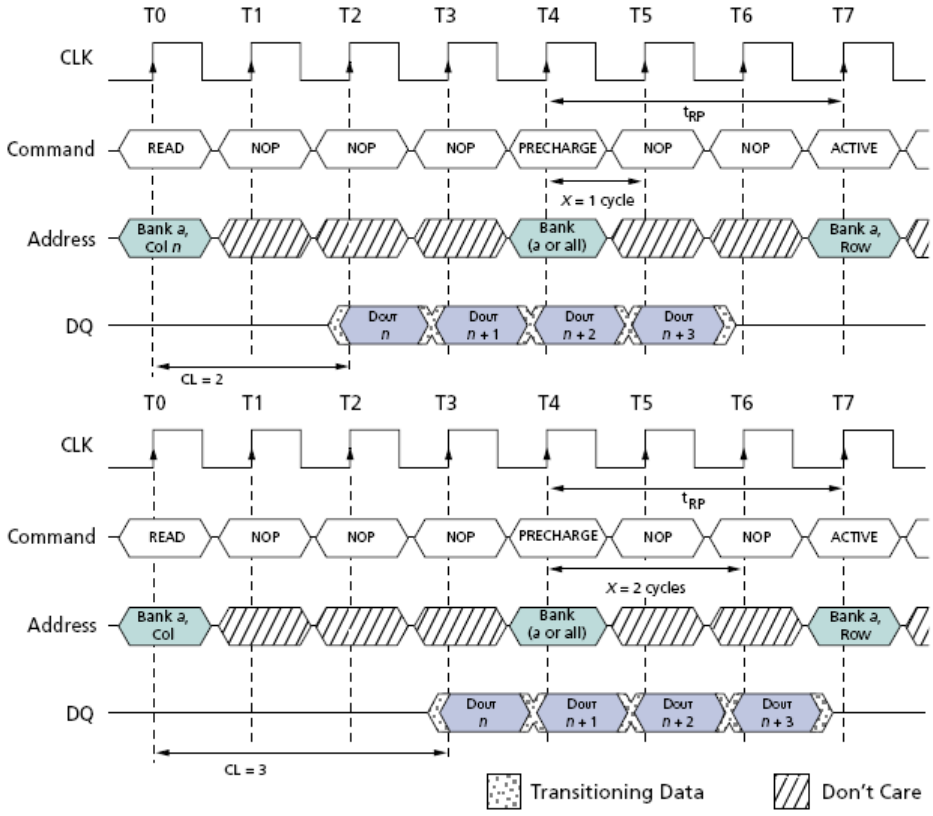
bursts.



Read to Precharge (CL=2 and CL=3)

Notes:

1. DQM is LOW.

READ BURST TERMINATE

Continuous-page READ bursts can be truncated with a BURST TERMINATE command and fixed-length READ bursts can be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued x cycles before the clock edge at which the last desired data element is valid, where x = CL - 1. The data element n + 3 is the last desired data element of a longer burst.

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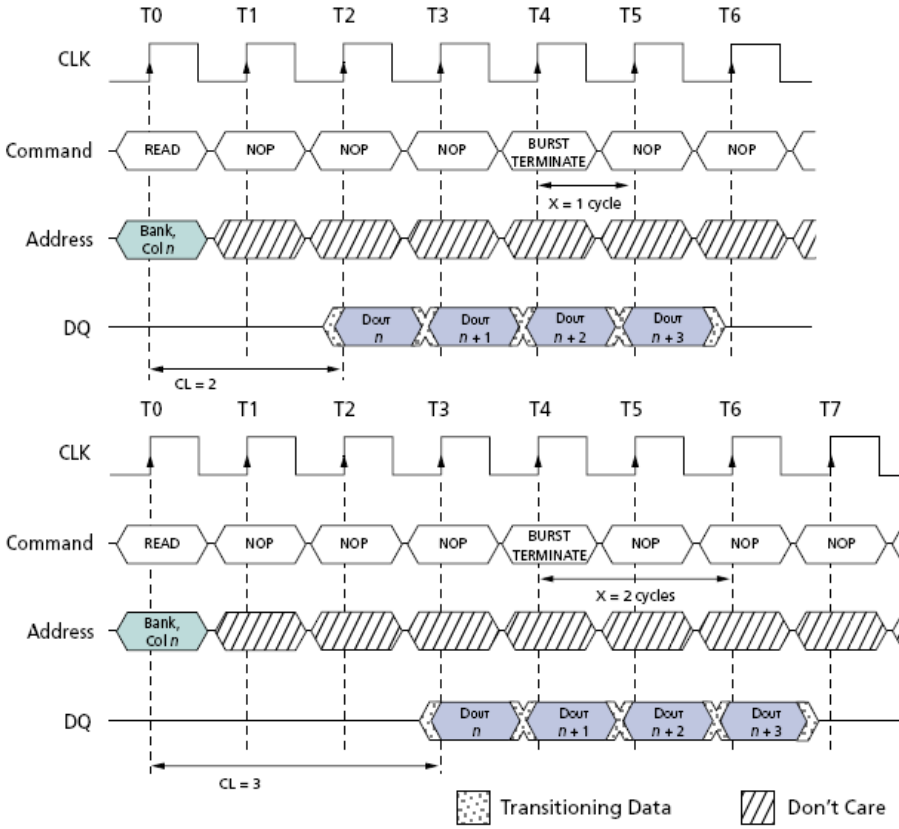
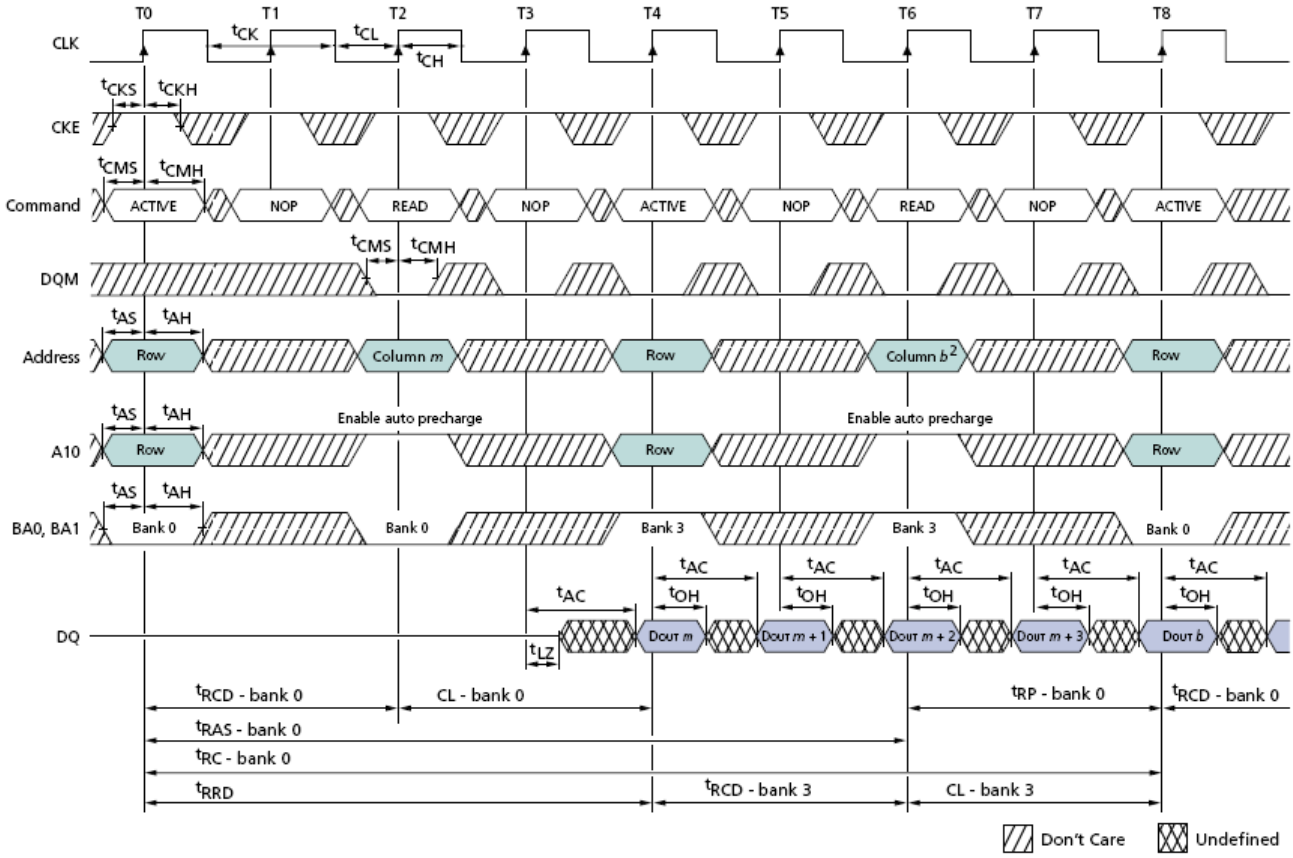


Terminating a Read Bursts (CL=2 and CL=3)

Notes: 1. DQM is LOW.



Alternating Bank Read Accesses (CL=2, and BL=4)

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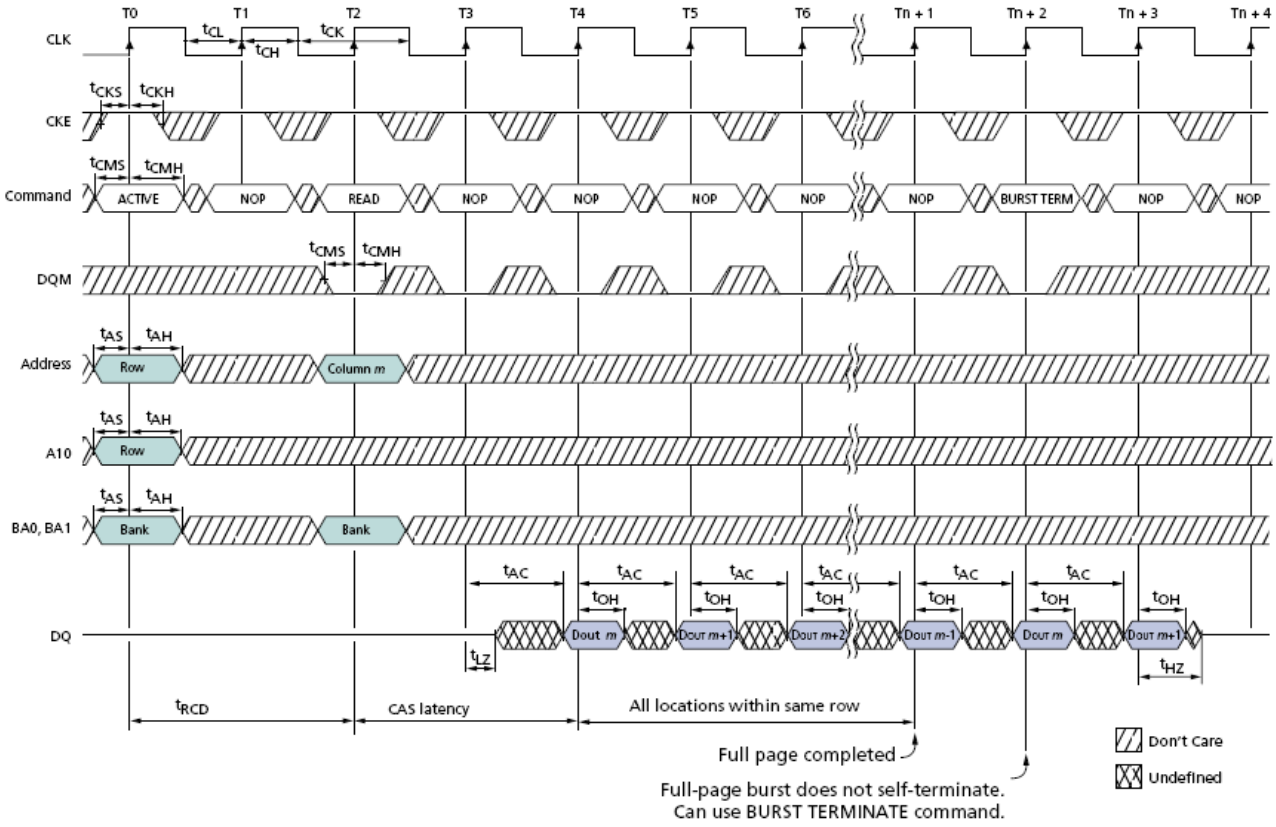
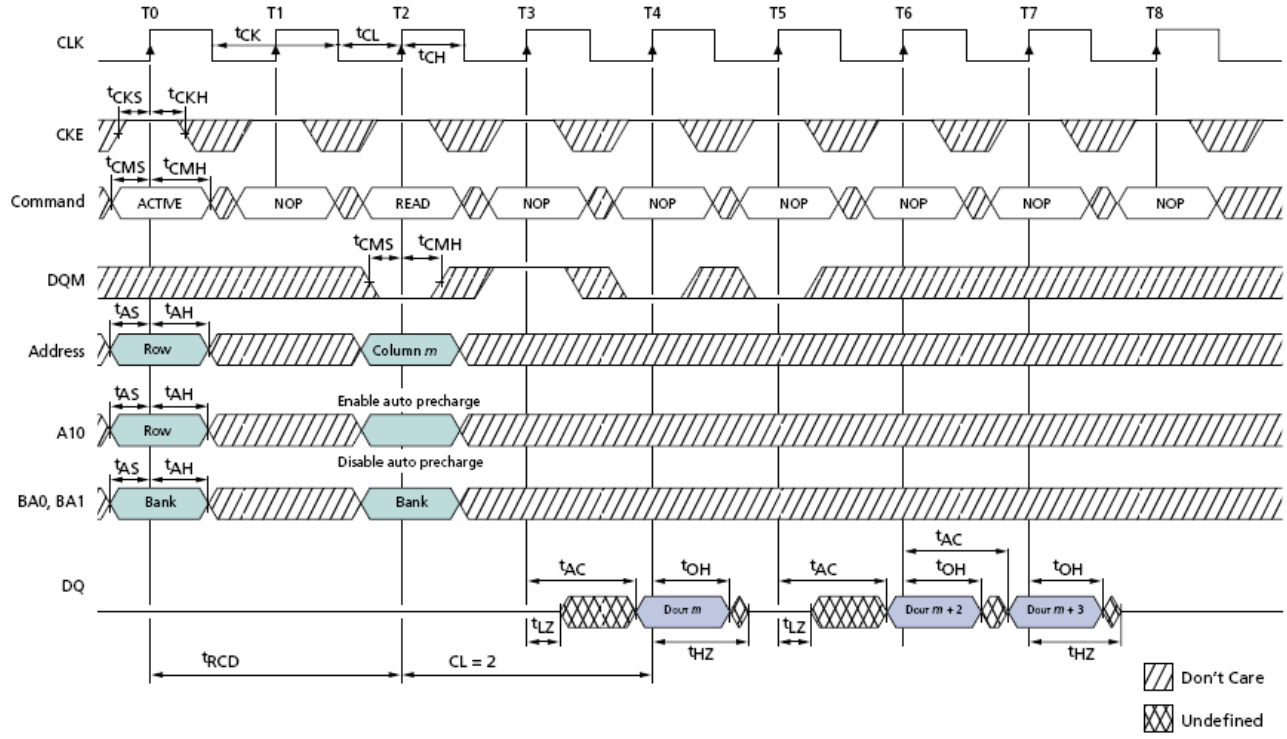


Read Continuous Page Burst (CL=2)



Read – DQM Operation (CL=2, and BL=4)

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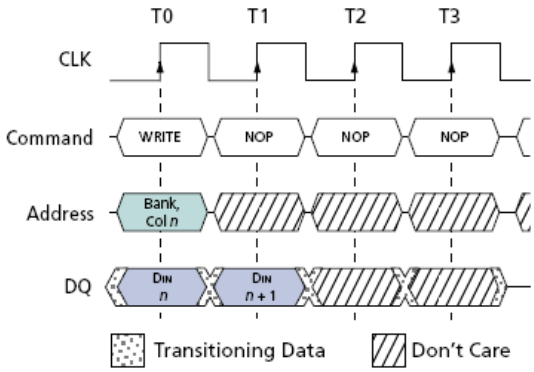
WRITEs

WRITE bursts are initiated with a WRITE command, the starting column and bank addresses are provided with the WRITE command and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

WRITE Burst

During WRITE bursts, the first valid data-in element is registered coincident with the WRITE command. Subsequent data elements are registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQ will remain at High-Z and any additional input data will be ignored. A continuous page burst continues until terminated; at the end of the page, it wraps to column 0 and continues.



Write Burst (BL=2)

Notes:

1. DQM is LOW.

WRITE to WRITE

Data for any WRITE burst can be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst can be followed immediately by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command. Data n + 1 is either the last of a burst of two or the last desired data element of a longer burst. LPSDR SDRAM uses a pipelined architecture and therefore does not require the 2n rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, or each subsequent WRITE can be performed to a different bank.

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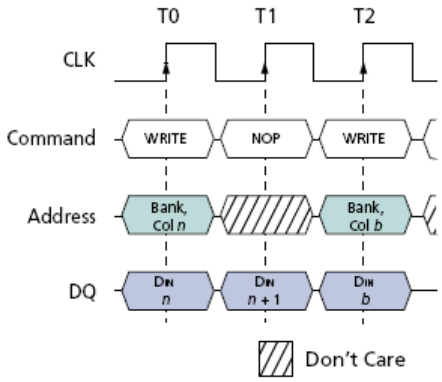
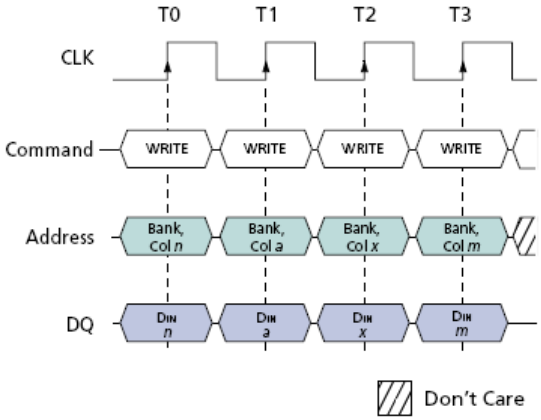


WRITE-to-WRITE

Notes:

1. DQM is LOW. Each WRITE command may be to any bank.



Random WRITE Cycles

Notes:

1. DQM is LOW. Each WRITE command may be to any bank.

WRITE to READ

Data for any WRITE burst can be truncated with a subsequent READ command, and data for a fixed-length WRITE burst can be followed immediately by a READ command. After the READ command is registered, data input is ignored and WRITEs will not be executed. Data n + 1 is either the last of a burst of two or the last desired data element of a longer burst.

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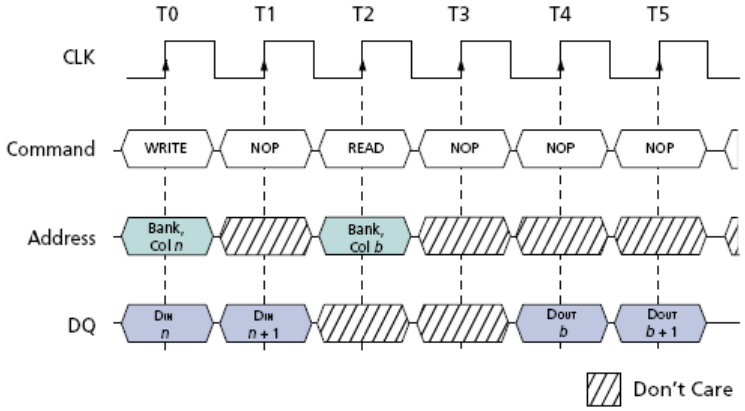

Write-to-Read (CL=2)

Notes:

1. The Write command can be to ant bank, and the READ command can be to any bank. DQM is LOW.

WRITE to PRECHARGE

Data for a fixed-length WRITE burst can be followed by or truncated with a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a continuous-page WRITE burst can be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued ^{t}WR after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a ^{t}WR of at least one clock with time to complete, regardless of frequency.

In addition, when truncating a WRITE burst at high clock frequencies (^{t}CK < 15ns), the DQM signal must be used to mask input data for the clock edge prior to and the clock edge coincident with the PRECHARGE command. Data n + 1 is either the last of a burst of two or the last desired data element of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until ^{t}RP is met.

In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length bursts or continuous page bursts.

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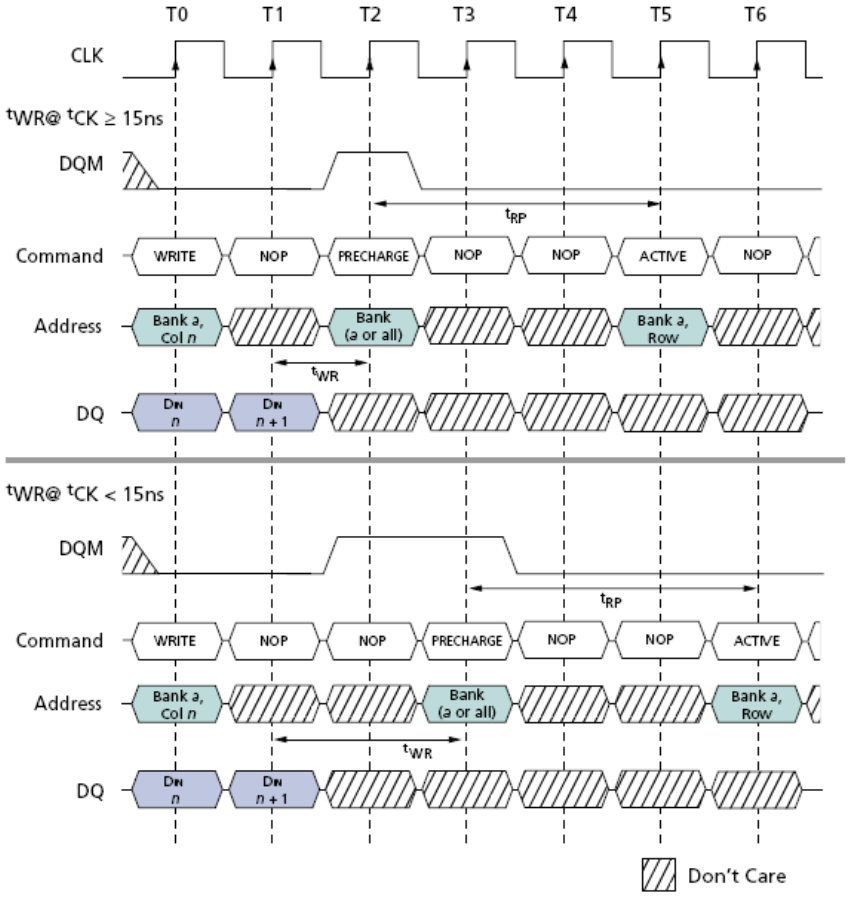


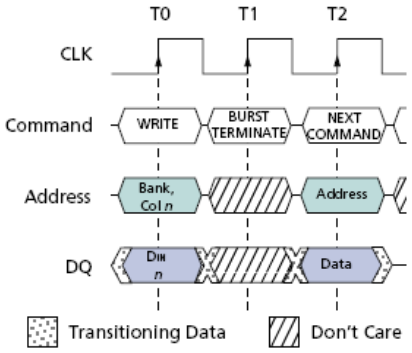
Write-to-Precharge

Notes:

1. In this example, DQM could remain LOW if the WRITE burst is a fixed length of two.

Terminating a WRITE Burst

Fixed-length WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command is ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command.



Terminating a WRITE Burst Notes: 1. DQM is LOW.

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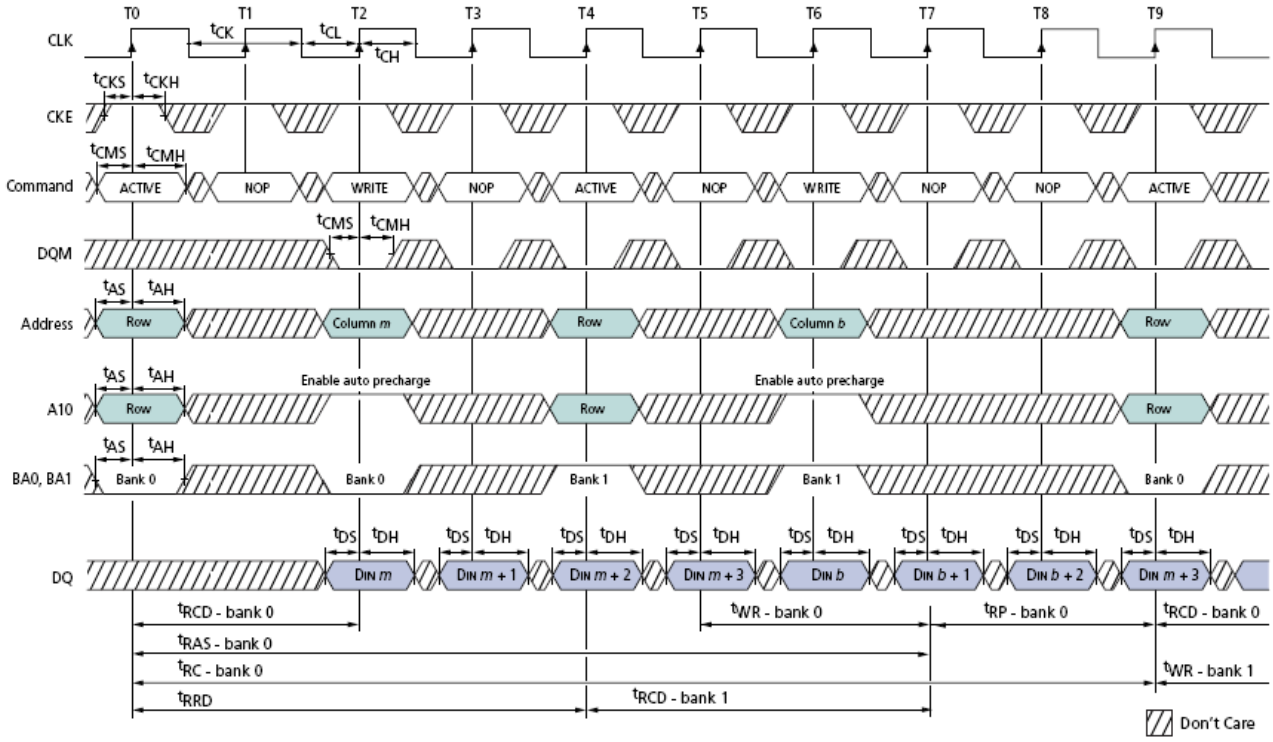
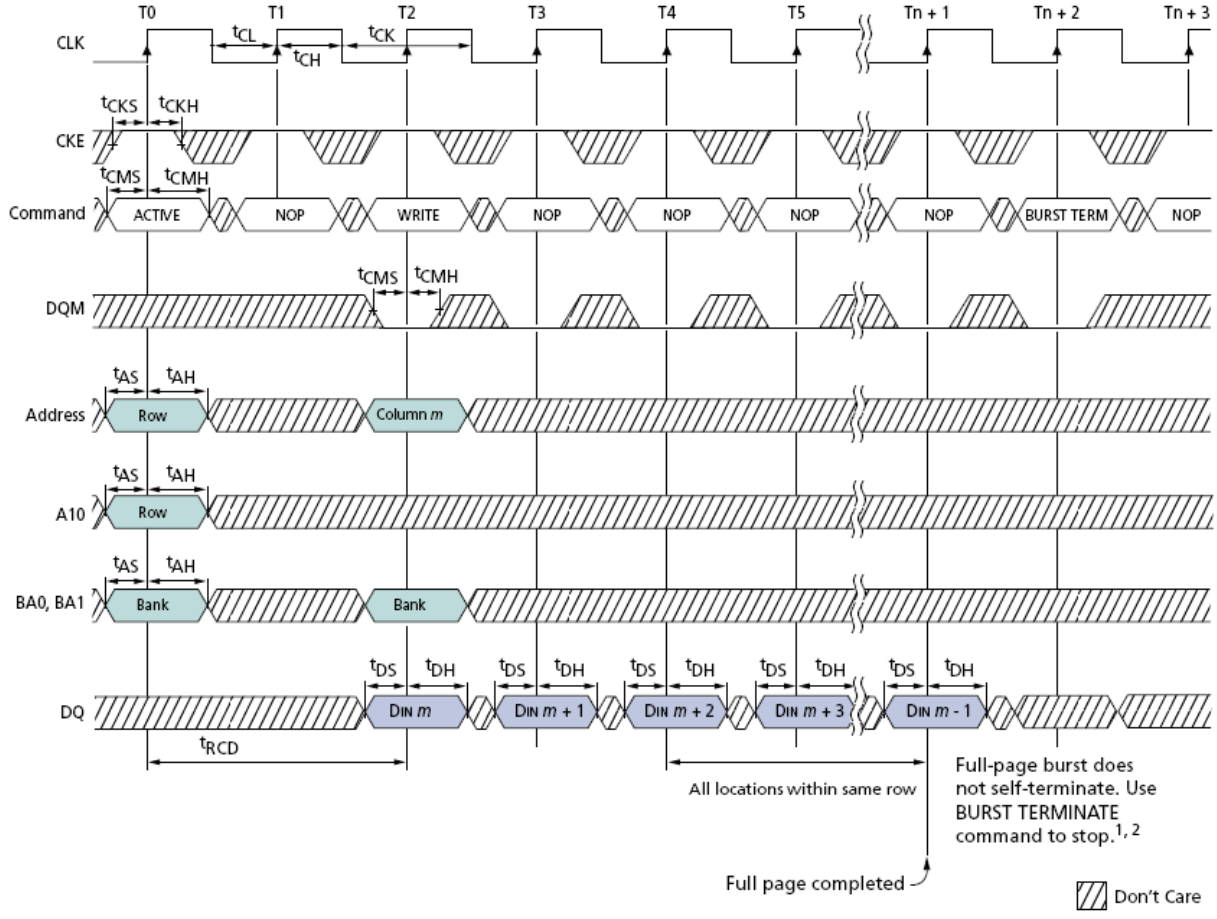


Alternating Bank Write Accesses (BL=4)



WRITE – Continuous Page Burst

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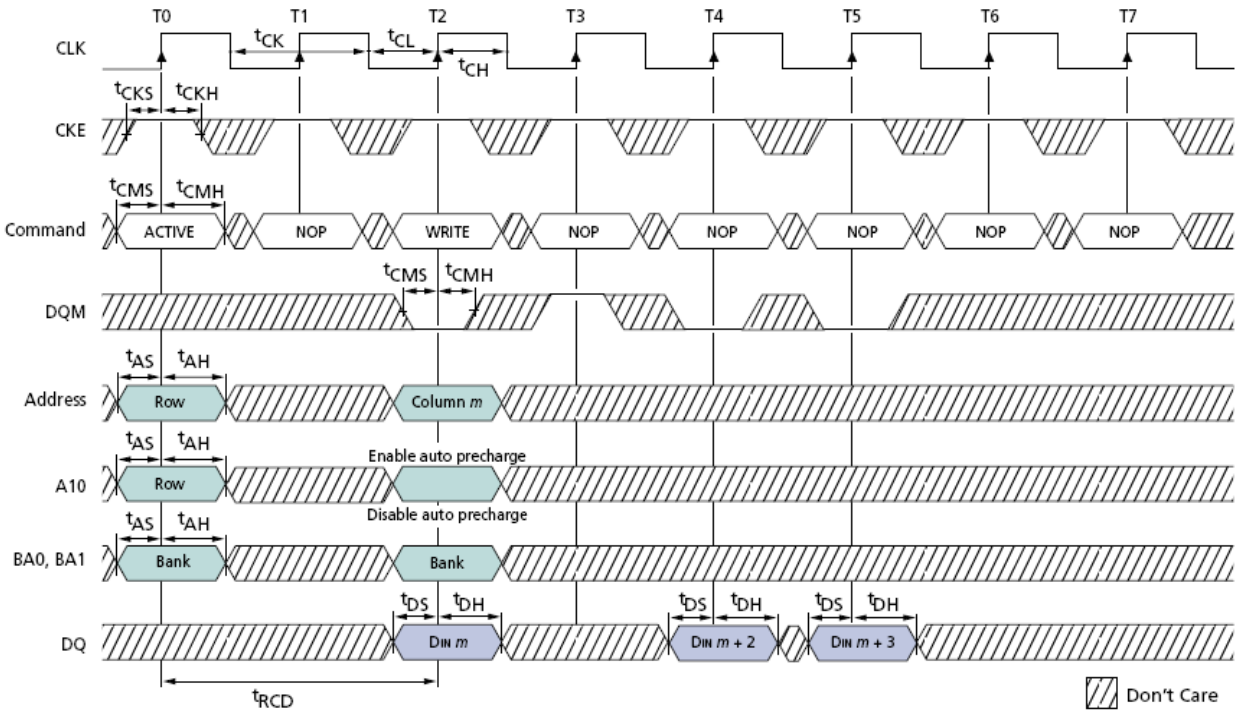
Notes:

1. ^{t}WR must be satisfied prior to issuing a PRECHARGE command.
2. Page left open; no ^{t}RP.



WRITE – DQM Operation (BL=4)

Burst Read/Single Write

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a "1." In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed BL. READ commands access columns according to the programmed BL and sequence, just as in the normal mode of operation (M9 = 0).

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PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (^{t}RP) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged. In case where only one bank is to be precharged (A10=LOW), inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care”. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command will be treated as a NOP if there is no open row in that bank (idle state), or if the previously open row is already in the process of precharging.

AUTO PRECHARGE

Auto Precharge is a feature which performs the same individual bank precharge function described previously, but without requiring an explicit command. This is accomplished by using A10 (A10=High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto precharge is non-persistent in that it is either enabled or disabled for each individual READ or WRITE command. Auto precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The “earliest valid stage” is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating ^{t}RAS(min). The READ with auto precharge enabled or WRITE with auto precharge enabled states can each be broken into two parts: the access period and the precharge period. The access period starts with registration of the command and ends where the precharge period (or ^{t}RP) begins. For READ with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For WRITE with auto precharge, the precharge period begins when ^{t}WR ends, with ^{t}WR measured as if auto precharge was disabled. In addition, during a WRITE with auto precharge, at least one clockis required during ^{t}WR time. During the prechare period, the user must not issue another command to the same bank until ^{t}RP is satisfied. This device supports ^{t}RAS lock-out. In the case of a single READ with auto-precharge or a single WRITE with auto-precharge issued at ^{t}RCD(min), the internal precharge will be delayed until ^{t}RAS(min) has been satisfied.

Concurrent AUTO PRECHARGE

This device supports concurrent auto precharge such that when a READ with auto precharge is enabled or a WRITE with auto precharge is enabled, any command to another bank is supported, as long as that command does not interrupt the read or write data transfer already in process. This feature enables the precharge to complete in the bank in which the READ or WRITE with auto precharge was executed, without requiring an explicit PREACHRGE command, thus freeing the command bus for operations in other banks. During the access period of a READ or a WRITE with auto precharge, only ACTIVE and PRECHARGE commands may be applied to other banks. During the precharge period, ACTIVE, PRECHARGE, READ, and WRITE commands may be applied to other banks. In either situation, all other related limitations apply.

READ with AUTO PRECHARGE

1. Interrupted by a READ (with or without auto precharge): A READ to bank m will interrupt a READ on bank n following the programmed CL. The precharge to bank n begins when the READ to bank m is registered.

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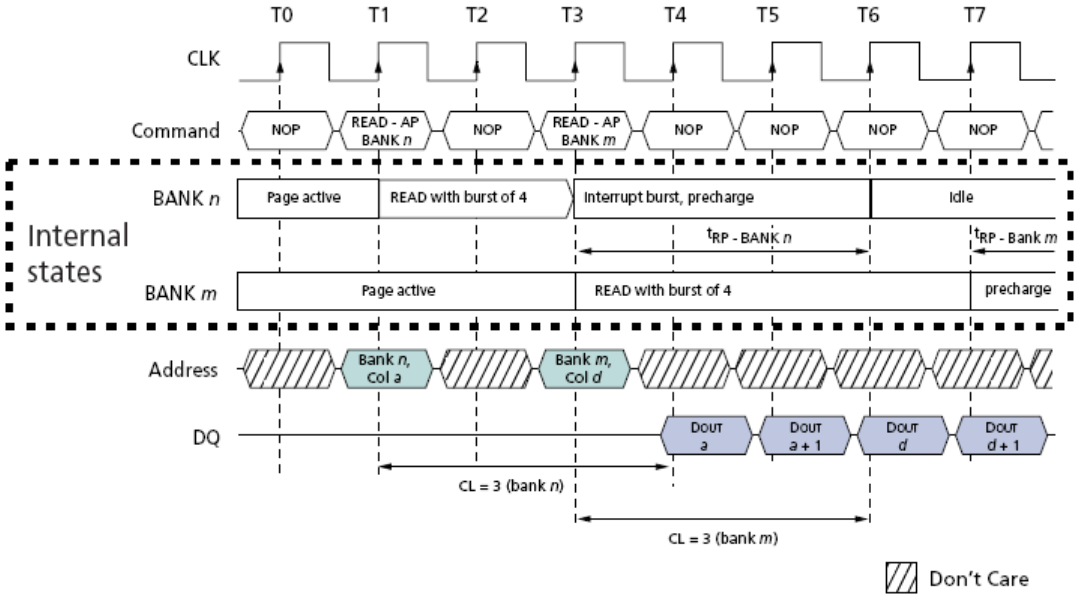
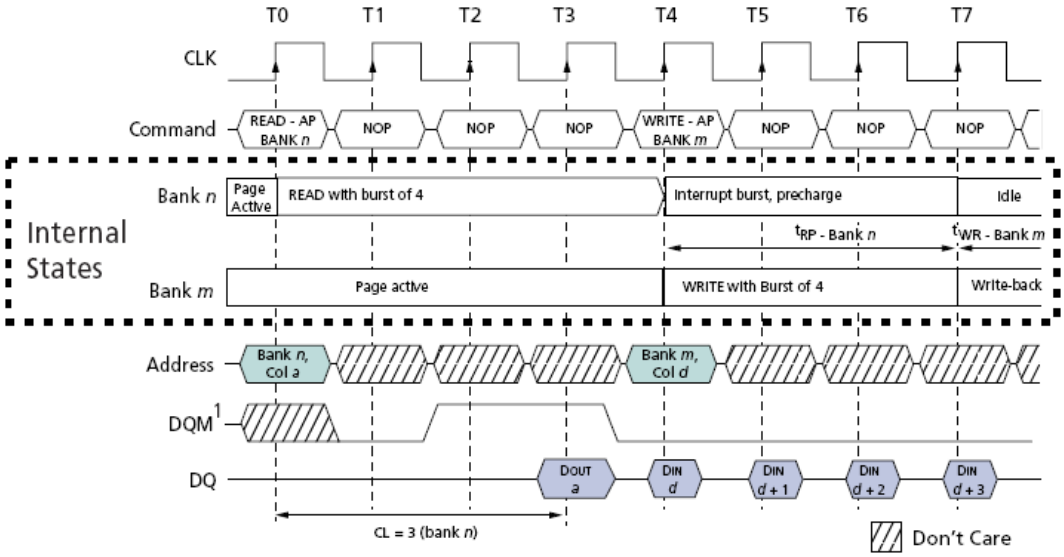
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank m will interrupt a READ on bank n when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The precharge to bank n begins when the WRITE to bank m is registered.



READ with Auto Precharge Interrupted by a READ

Notes:

1. DQM is LOW.



READ with Auto Precharge Interrupted by a WRITE

Notes:

1. DQM is HIGH at T2 to prevent Dout a+1 from contending with Din d at T4.

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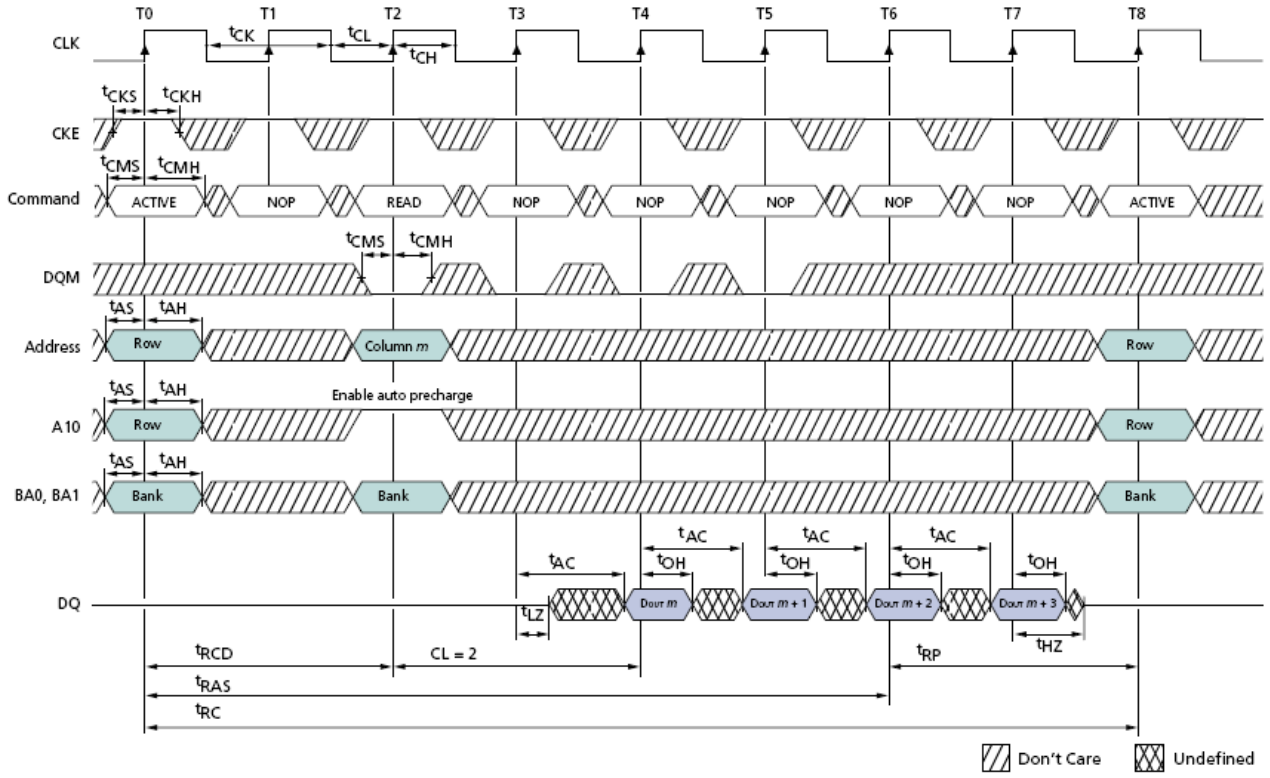
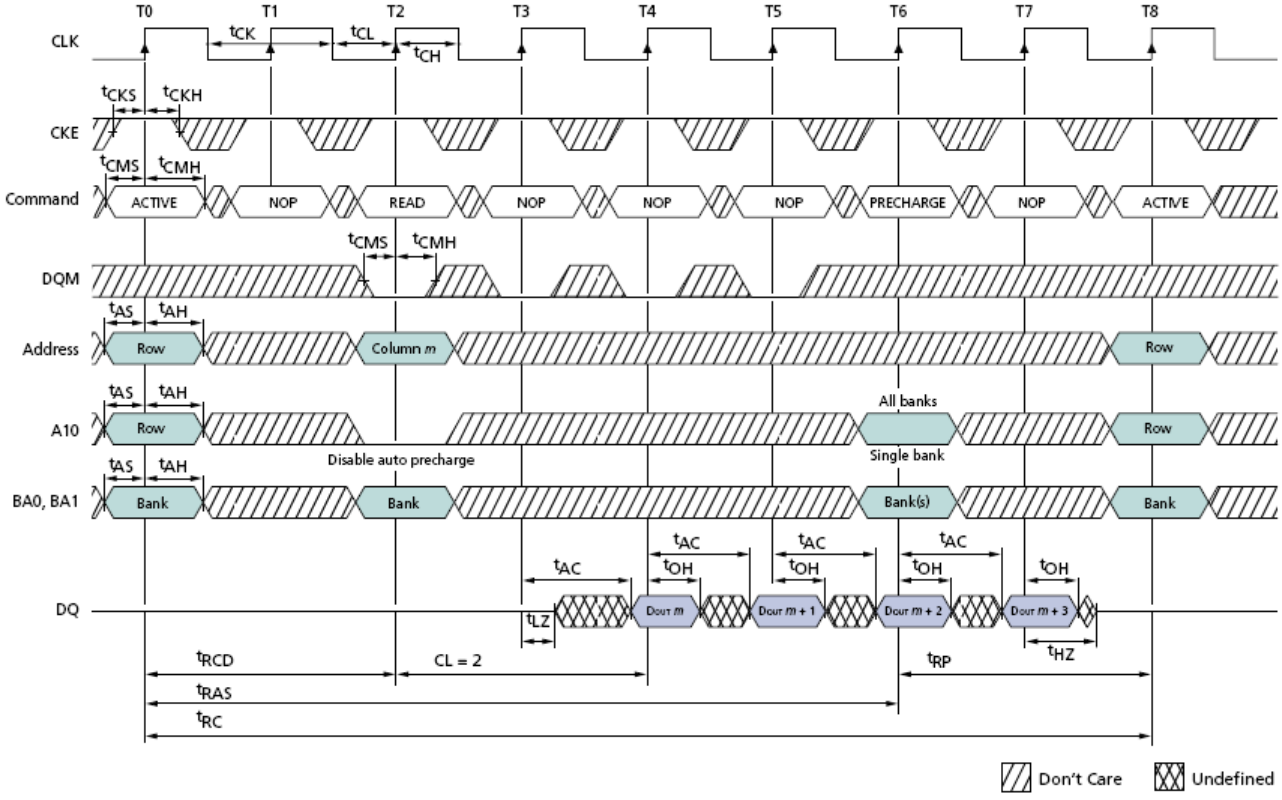


READ with Auto Precharge (BL=4 and CL=2)



READ without Auto Precharge (BL=4 and CL=2)

Notes: 1. The READ burst is followed by a manual PRECHARGE.

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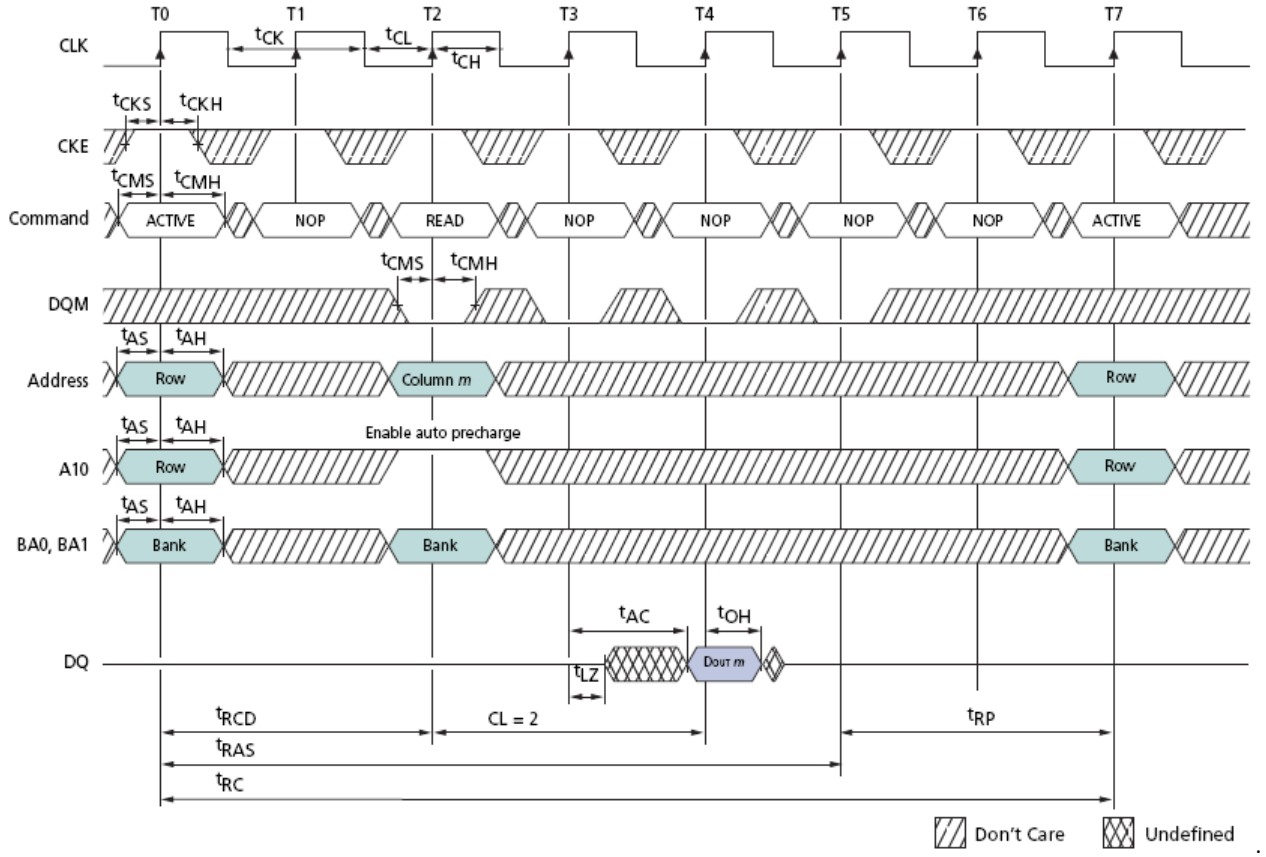
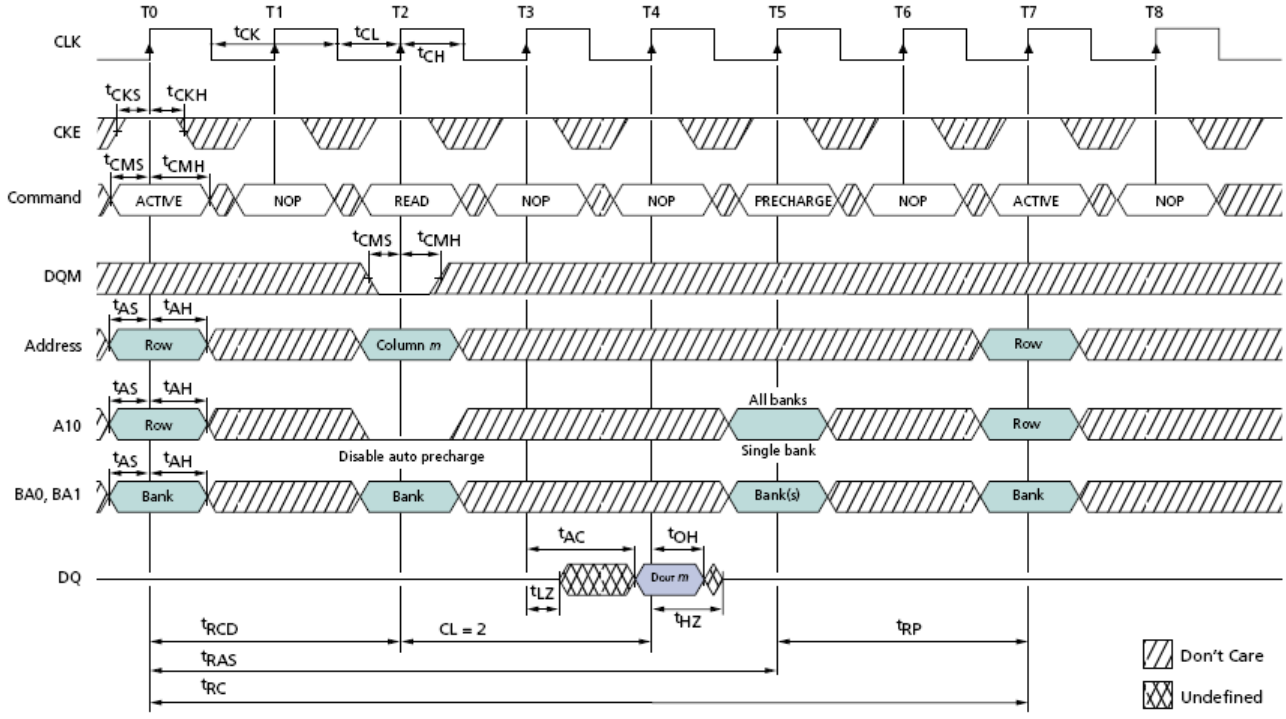


Single READ with Auto Precharge (BL=1 and CL=2)



Single READ without Auto Precharge (BL=1 and CL=2)

Notes: 1. The READ burst is followed by a manual PRECHARGE.

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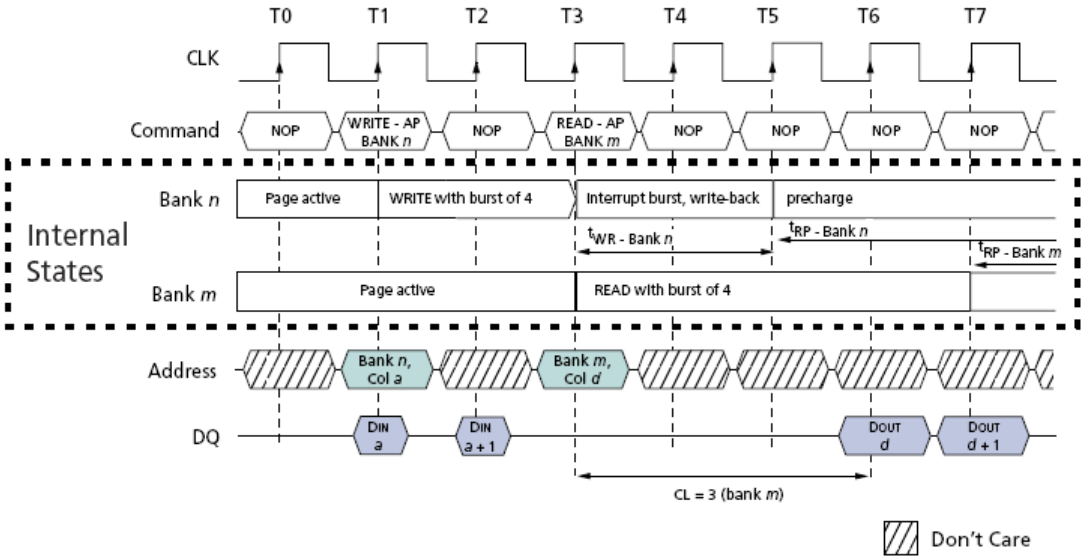
WRITE with AUTO PRECHARGE

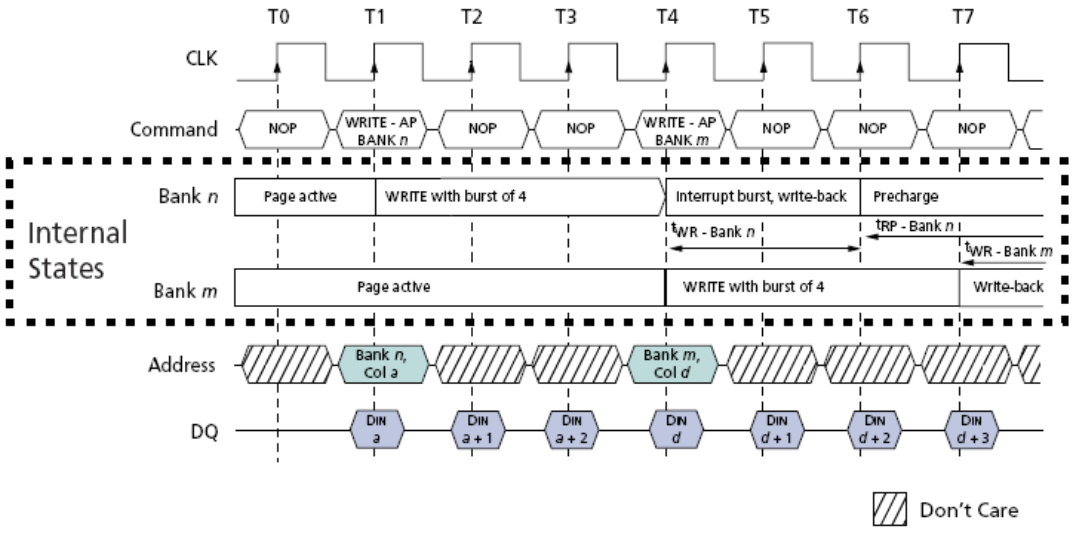
1. Interrupted by a READ (with or without auto precharge): A READ to bank m will interrupt a WRITE on bank n when registered, with the data-out appearing CL later. The precharge to bank n will begin after tWR is met, where tWR begins when the READ to bank m is registered. The last valid WRITE to bank n will be data-in registered one clock prior to the READ to bank m.

2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank m will interrupt a WRITE on bank n when registered. The precharge to bank n will begin after tWR is met, where tWR begins when the WRITE to bank m is registered. The last valid data WRITE to bank n will be data registered one clock prior to a WRITE to bank m.



WRITE with Auto Precharge Interrupted by a READ

Notes: 1. DQM is LOW.



WRITE with Auto Precharge Interrupted by a WRITE

Notes: 1. DQM is LOW.

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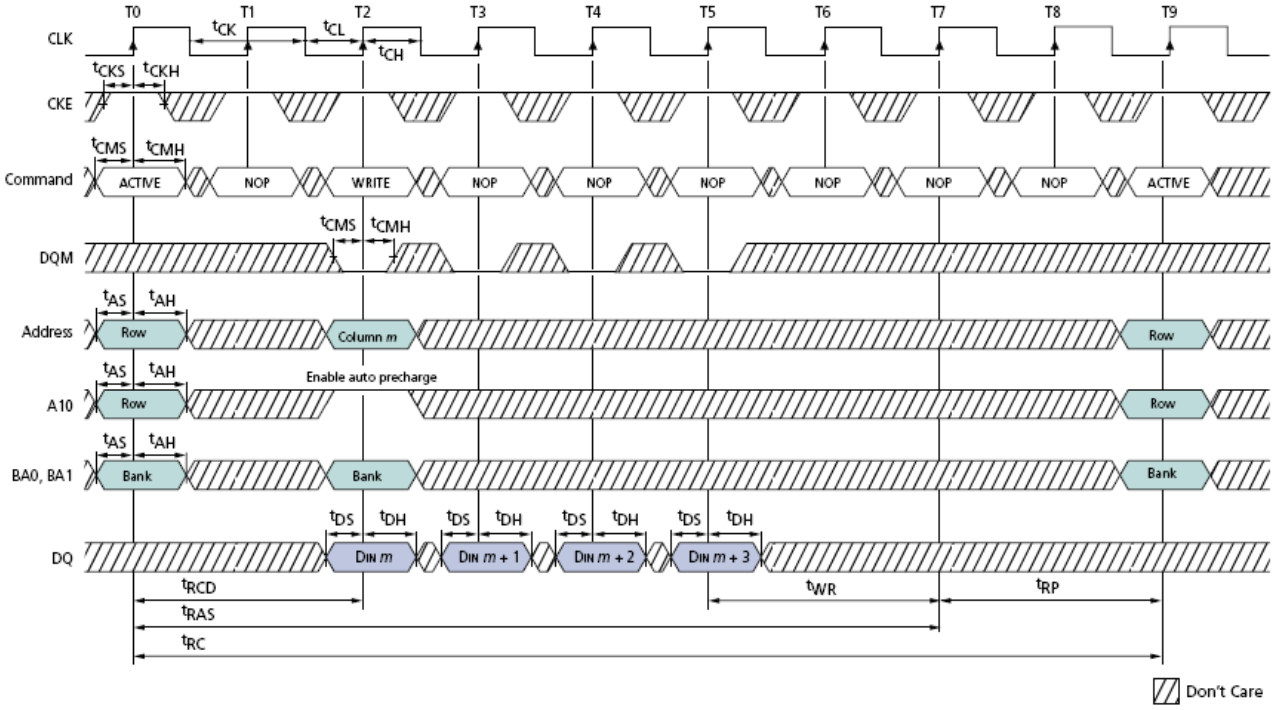
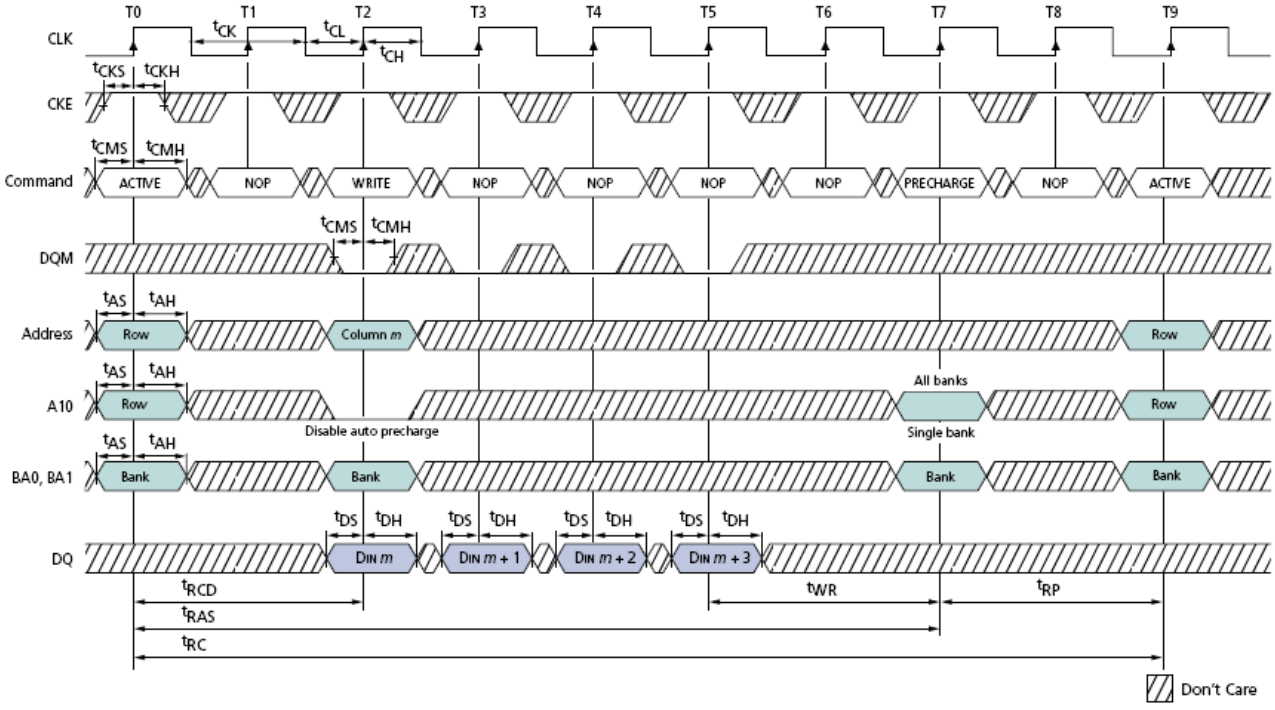


WRITE with Auto Precharge (BL=4)



WRITE without Auto Precharge (BL=4)

Notes: 1. The WRITE burst is followed by a manual PRECHARGE.

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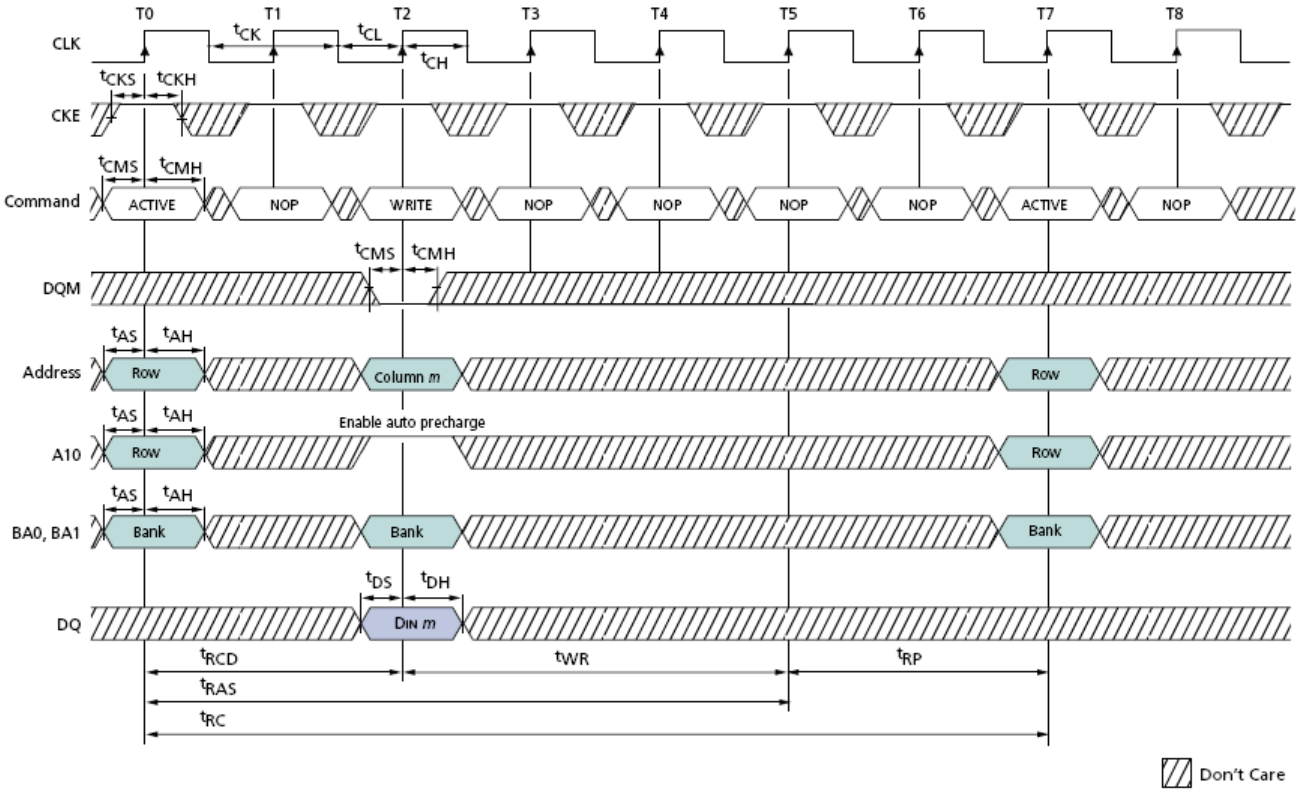
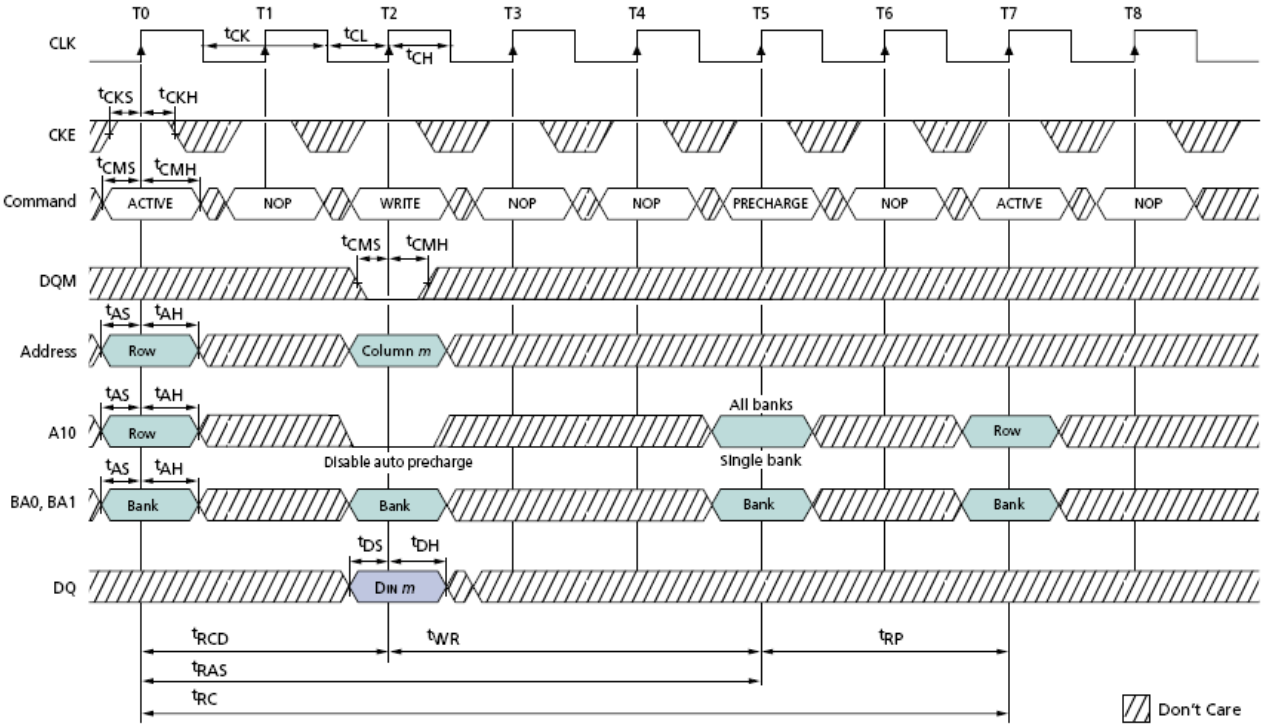


Single WRITE wit Auto Precharge (BL=1)



Single WRITE without Auto Precharge (BL=1)

Notes: 1. The WRITE burst is followed by a manual PRECHARGE.

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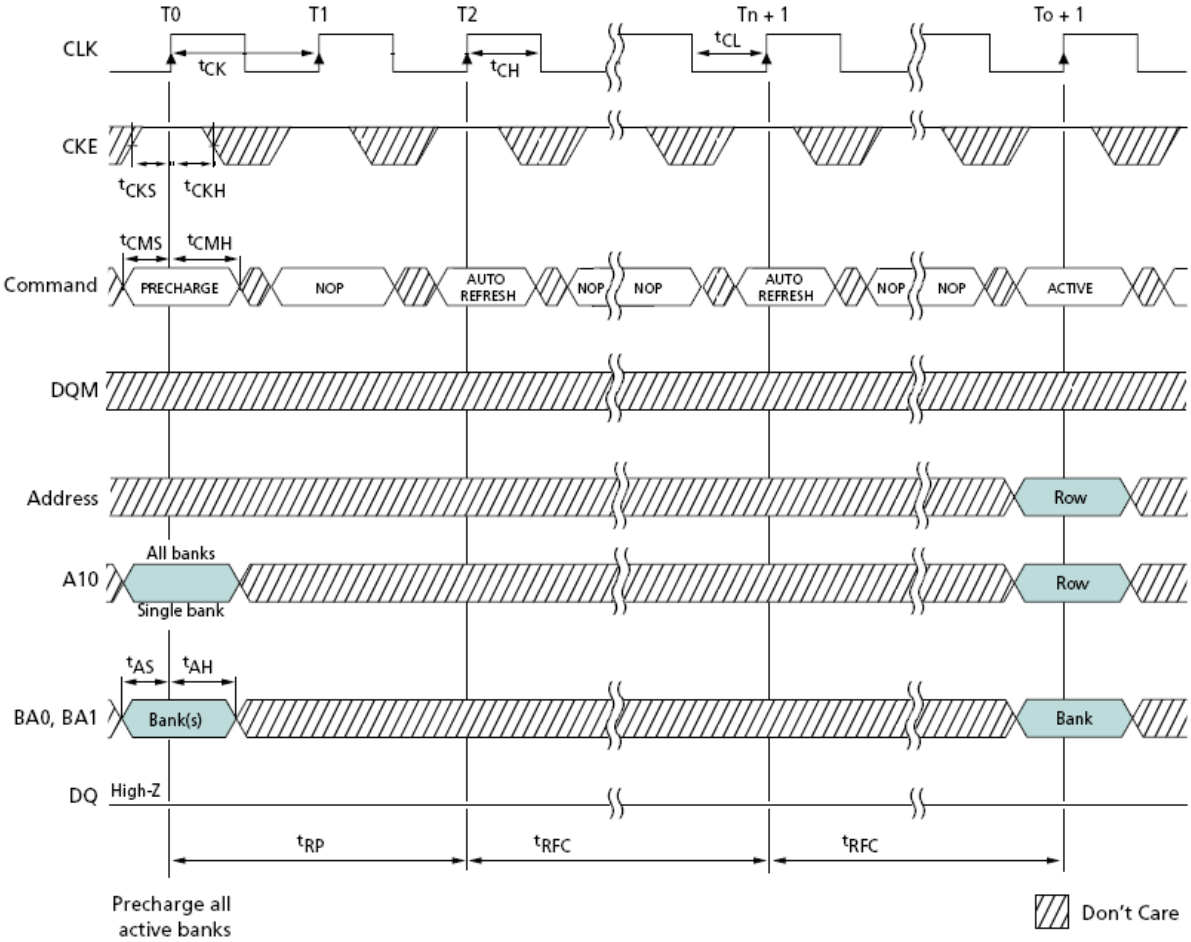
AUTO REFRESH

The AUTO REFRESH command is used during normal operation of the SDRAM to refresh the contents of the SDRAM array. This command is non persistent, so it must be issued each time a refresh is required. All active banks must be precharged prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum ^{t}RP is met following the PRECHARGE command. Addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an AUTO REFRESH command.

After the AUTO REFRESH command is initiated, it must not be interrupted by any executable command until ^{t}RFC has been met. During ^{t}RFC time, COMMAND INHIBIT or NOP commands must be issued on each positive edge of the clock. The SDRAM requires that every row be refreshed each ^{t}REF period. Providing a distributed AUTO REFRESH command—calculated by dividing the refresh period (^{t}REF) by the number of rows to be refreshed—meets the timing requirement and ensures that each row is refreshed. Alternatively, a burst refresh can be employed after every ^{t}REF period—by issuing consecutive AUTO REFRESH commands for the number of rows to be refreshed at the minimum cycle rate (^{t}RFC)—to satisfy the refresh requirement.



Auto Refresh Mode

Notes: 1. Back-to-Back AUTO REFRESH commands are not required.

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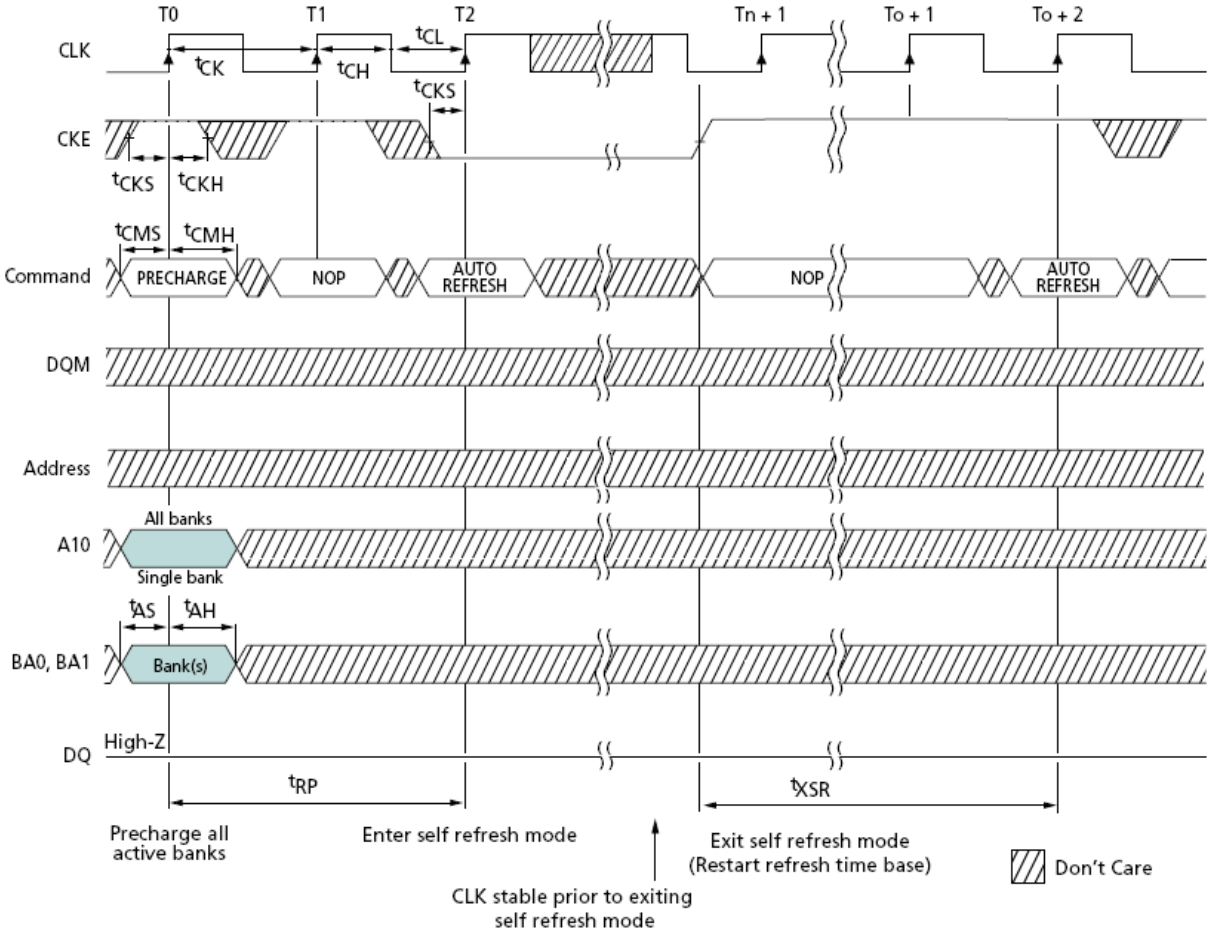
SELF REFRESH

The self refresh mode can be used to retain data in the SDRAM, even if the rest of the system is powered down. When in self refresh mode, the SDRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command, except CKE is disabled (LOW). After the SELF REFRESH command is registered, all the inputs to the SDRAM become "Don't Care" with the exception of CKE, which must remain LOW.

After self refresh mode is engaged, the SDRAM provides its own internal clocking, enabling it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to ^{t}RAS and remains in self refresh mode for an indefinite period beyond that.

The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) prior to CKE going back HIGH. After CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for ^{t}XSR because time is required for the completion of any internal refresh in progress.

Upon exiting the self refresh mode, AUTO REFRESH commands must be issued according to the distributed refresh rate (^{t}REF/refresh row count) as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.



Self Refresh Mode

Notes: 1. Each AUTO REFRESH command performs a REFRESH cycle. Back-to-Back commands are not required.

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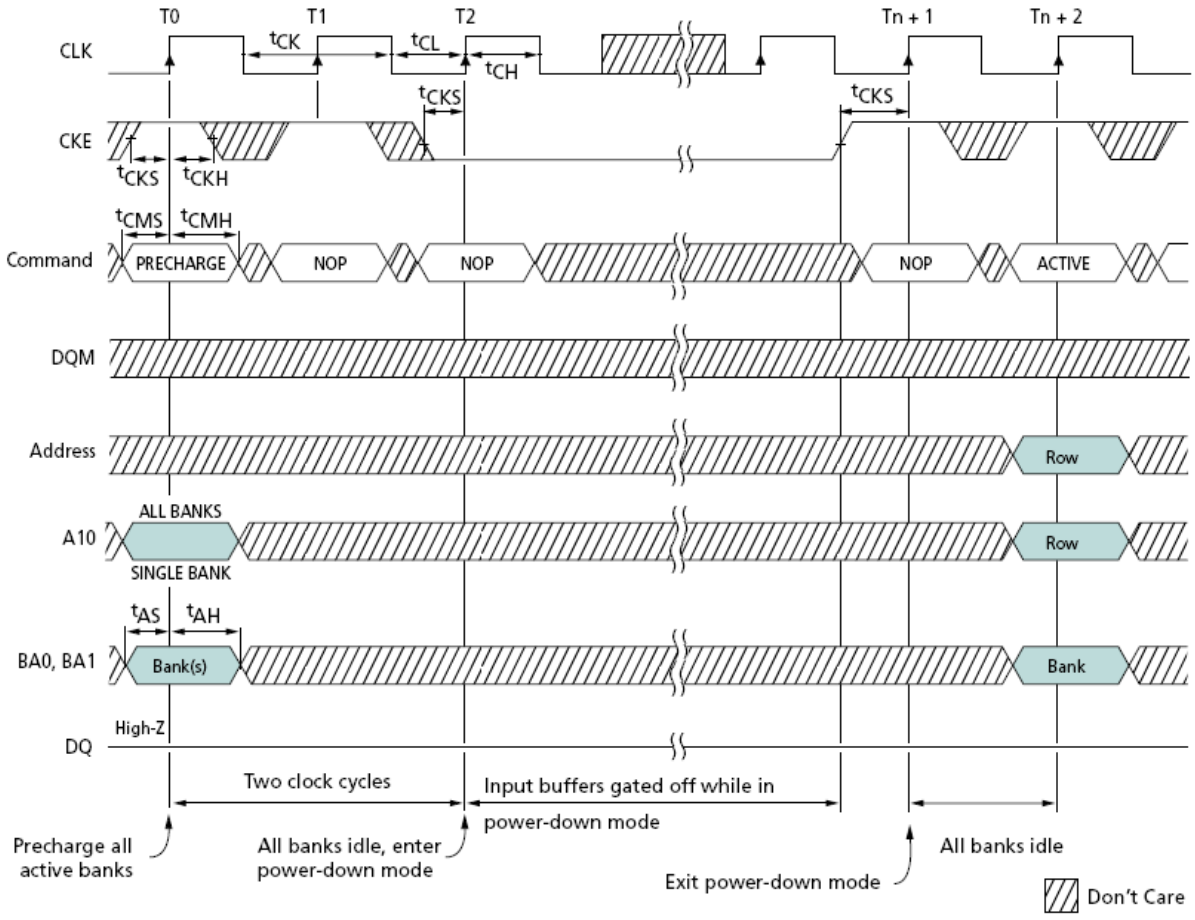
Power-Down

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device cannot remain in the power-down state longer than the refresh period (64ms) as no REFRESH operations are performed in this mode. The power-down state is exited by registering a NOP or COMMAND INHIBIT with CKE HIGH at the desired clock edge (meeting ^{t}CKS).



Power-Down Mode

Notes: 1. Violating refresh requirements during power-down may result in a loss of data.

Deep-Power-Down

Deep power-down mode is a maximum power-saving feature achieved by shutting off the power to the entire device memory array. Data on the memory array will not be retained after deep power-down mode is executed. Deep power-down mode is entered by having all banks idle, with CS# and WE# held LOW with RAS# and CAS# HIGH at the rising edge of the clock, while CKE is LOW. CKE must be held LOW during deep power down.

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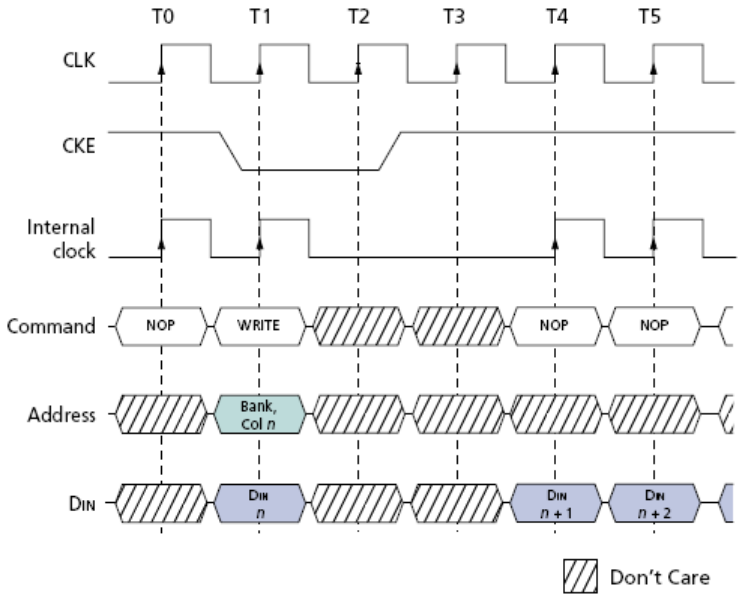
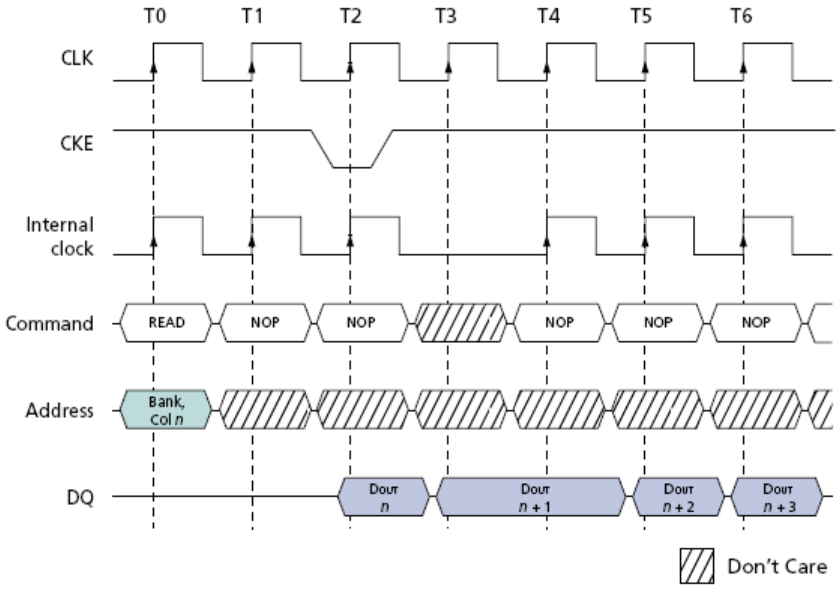
Clock Suspend

The clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, “freezing” the synchronous logic. For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input balls when an internal clock edge is suspended will be ignored; any data present on the DQ balls remains driven; and burst counters are not incremented, as long as the clock is suspended. Exit clock suspend mode by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.



Clock Suspend during WRITE Burst (BL=4 or greater)

Notes: 1. DQM is LOW.



Clock Suspend during READ Burst (CL=2, BL=4 or greater)

Notes: 1. DQM is LOW.

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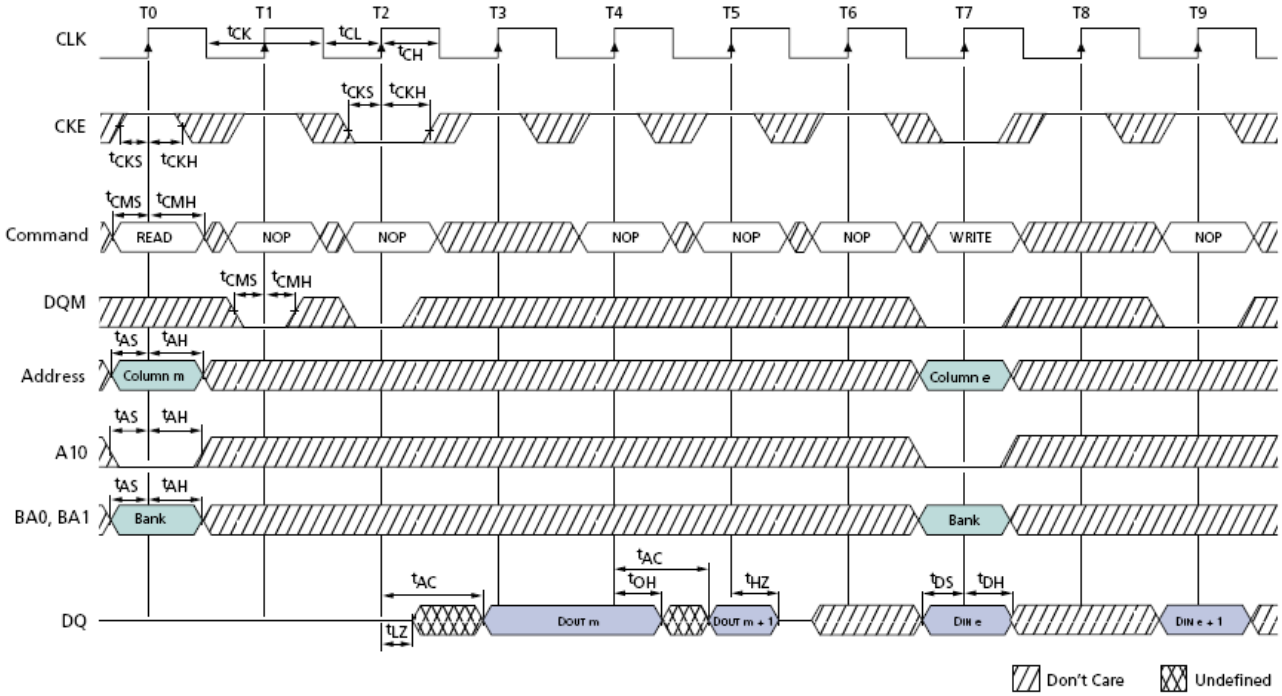

Clock Suspend Mode (CL=3, and BL=2)

Notes: 1. The Auto Precharge is disable..

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Revision Log

Rev	Date	Modification
0.1	11/2009	Preliminary Release
0.2	11/2010	Update the AC/DC data base on real silicon characterization performance
0.21	7/11/2012	Update ordering information and part number guide
0.3	10/31/2012	IDD Specifications correction

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