EiceDRIVER™

1ED020I12-S

Single IGBT Driver IC

Power Management & Drives

Never stop thinking.

Revision History:	**2006-11-13**	Version 1.2
Previous Version:	Target Datasheet 1.1	

Page	Subjects (major changes since last revision)
7	Update Functional Description
16	Update VDE 0884-10 (Draft) Isolation Characteristics
19	Update Package Outlines

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Single IGBT Driver IC

Product Highlights

- **Coreless transformer isolated driver**
- **Galvanic isolation**
- **Integrated protection features**
- **Suitable for operation at high ambient temperature**
- **Cost effective technology**

Features

- Single channel isolated IGBT Driver
- For 600V/1200V IGBTs
- 2A rail-to-rail output
- Vcesat-detection
- Two-level-turn-off
- Active Miller Clamp

Typical Application

- AC-Drives
- UPS-Systems
- Welding

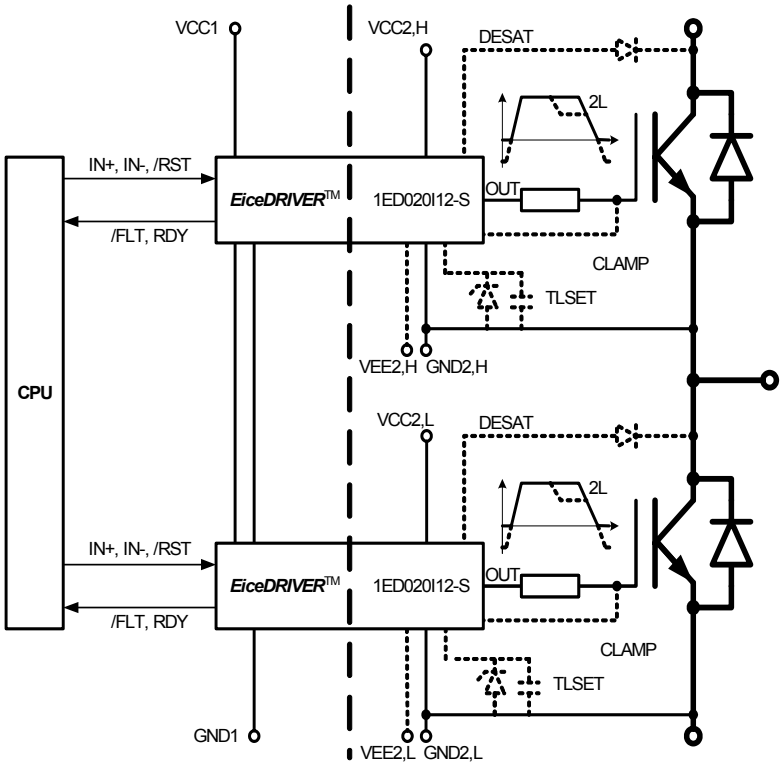

Figure 1: Typical Application

Type	Ordering Code	Gate drive current	Package
1ED020I12-S	t.b.d	+/- 2A	PG-DSO-16-15

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1 Blockdiagram and Application

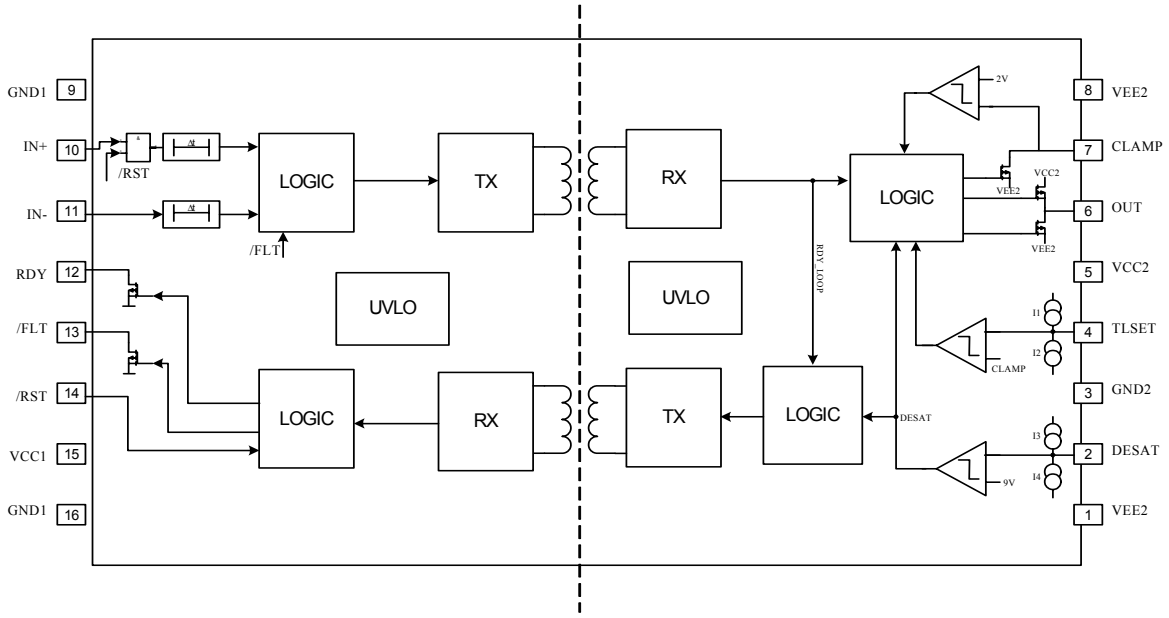


Figure 2: Blockdiagram 1ED020I12-S

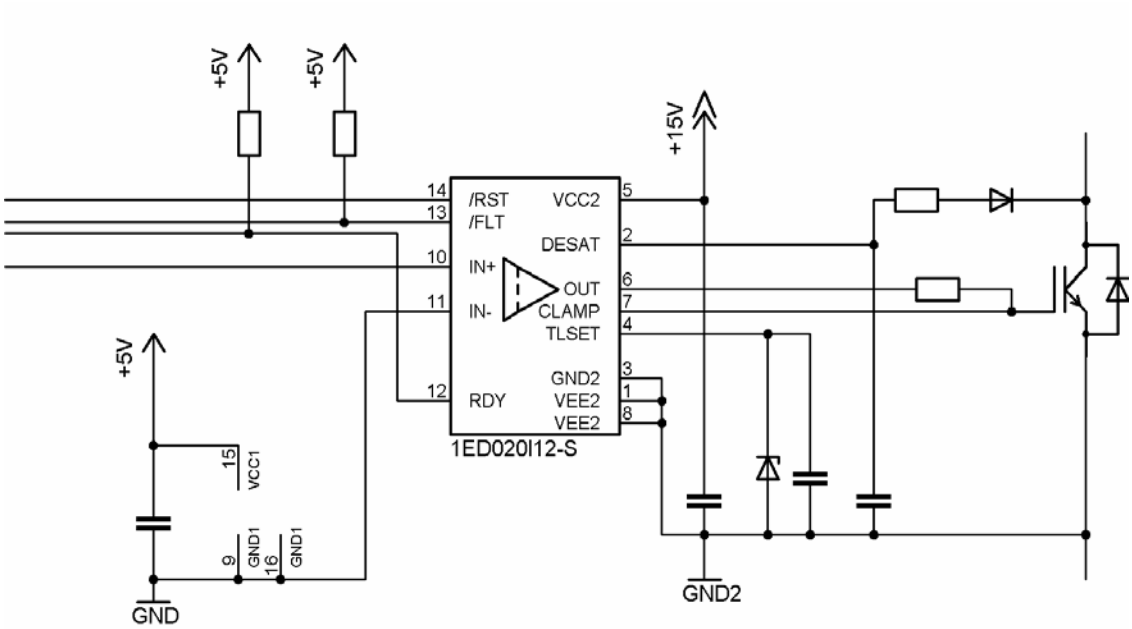


Figure 3: Application example

2 Functional Description

2.1 Introduction

The 1ED020I12-S is an advanced IGBT gate driver that can be also used for driving power MOS. Control and protection functions are included to make possible the design of high reliability systems.

The device consists of two galvanic separated parts. The input chip can be directly connected to a standard 5V DSP or microcontroller with CMOS in/output and the output chip is connected to the high voltage side.

An effective active Miller clamp function avoids the need of negative gate driving in most applications and allows the use of a simple bootstrap supply for the high side driver.

A rail-to-rail driver output enables the user to provide easy clamping of the IGBTs gate voltage during short circuit of the IGBT. So an increase of short circuit current due to the feedback via the Miller capacitance can be avoided. Further, a rail-to-rail output reduces power dissipation.

The device also includes an IGBT desaturation protection with a FAULT status output.

A two-level turn-off feature with adjustable delay protects against excessive overvoltage at turn-off in case of overcurrent or short-circuit condition. The same delay is applied at turn-on to prevent pulse width distortion.

A READY status output reports if the device is supplied and operates correctly.

2.2 Internal Protection Features

2.2.1 Undervoltage Lockout (UVLO)

To ensure correct switching of IGBTs the device is equipped with an undervoltage lockout for both chips.

If the powersupply voltage V_{VCC1} of the input chip drops below V_{UVLOL1} a turn-off signal is sent to the output chip before power-down. The IGBT is switched off and the signals at IN+ and IN- are ignored as long as V_{VCC1} reaches the power-up voltage V_{UVLOH1} .

If the power supply voltage V_{VCC2} of the output chip goes down below V_{UVLOL2} the IGBT is switched off and signals from the input chip are ignored as long as V_{VCC2} reaches the power-up voltage V_{UVLOH2} .

2.2.2 READY status output

The READY output shows the status of three internal protection features.

- UVLO of the input chip
- UVLO of the output chip after a short delay
- Internal signal transmission

It is not necessary to reset the READY signal since its state only depends on the status of the former protection signals.

2.2.3 Watchdog Timer

During normal operation the internal signal transmission is monitored by a watchdog timer. If the transmission fails for a given time, the IGBT is switched off and the READY output reports an internal error.

2.2.4 Active Shut-Down

The Active Shut-Down feature ensures a safe IGBT off-state if the output chip is not connected to the power supply.

2.3 Non-Inverting and Inverting Inputs

There are two possible input modes to control the IGBT. At non-inverting mode IN+ controls the driver output while IN- is set to low. At inverting mode IN- controls the driver output while IN+ is set to high. A minimum input pulse width is defined to filter occasional glitches.

2.4 Driver Output

The output driver section uses only Mosfets to provide a rail-to-rail output. Due to this feature tight control of gate voltage during on-state and short circuit can be maintained as long as the drivers supply is stable. Due to the low internal voltage drop switching behaviour of the IGBT is predominantly governed by the gate resistor. Furthermore, this reduces the power to be dissipated by the driver.

2.5 Two-Level Turn-Off

The two-level turn-off optimizes the switching of the IGBT. During turn-off, the gate voltage can be reduced to a programmable level in order to reduce the IGBT current (at overcurrent). This action avoids a dangerous overvoltage across the IGBT, especially at short circuit turn-off.

The turn-off (Ta) delay is programmable through an external zener diode and a capacitor for accurate timing.

The turn-off delay (Ta) is also used to delay the input signal to prevent distortion of the input pulse width.

2.6 External Protection Features

2.6.1 Desaturation Protection

A desaturation protection ensures the protection of the IGBT at short-circuit. When the DESAT voltage goes up and reaches 9V, the output is driven low (with 2-level turn-off if applicable). Further, the FAULT output is activated. A programmable blanking time is used to allow enough time for IGBT saturation. Blanking time is provided by a highly precise internal current source and an external capacitor.

2.6.2 Active Miller Clamping

A Miller clamp allows sinking the Miller current during a high dV/dt situation. Therefore, the use of a negative supply voltage can be avoided in many applications. During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2V (related to VEE2). The clamp is designed for a Miller current up to 1A.

2.6.3 Short-Circuit Clamping

During short circuit the IGBTs gate voltage tends to rise because of the feedback via the Miller capacitance. An additional protection circuit connected to OUT and CLAMP limits this voltage to a value slightly higher than the supply voltage. A current of maximum 500 mA for 10us may be fed back to the supply through one of this paths. If higher currents are expected or a tighter clamping is desired external Schottky diodes may be added.

2.7 RESET

The reset input has two functions.

Firstly, /RST is in charge of setting back the FAULT output. If /RST is low longer than a given time , /FLT will be reseted; otherwise, it will remain unchanged. Moreover, it works as enable/shutdown of the input logic.

3 Pin Configuration and Functionality

3.1 Pin Configuration

Pin	Symbol	Function
1	VEE2	Negative power supply output side
2	DESAT	Desaturation protection
3	GND2	Signal ground output side
4	TLSET	Timing and reference level for two-level turn-off
5	VCC2	Positive power supply output side
6	OUT	Driver output
7	CLAMP	Miller clamping
8	VEE2	Negative power supply output side
9	GND1	Signal ground input side
10	IN+	Non inverted driver input
11	IN-	Inverted driver input
12	RDY.	Ready output
13	$\overline{\text{FLT}}$	Fault output
14	$\overline{\text{RST}}$	Reset input
15	VCC1	Positive power supply input side
16	GND1	Signal ground input side

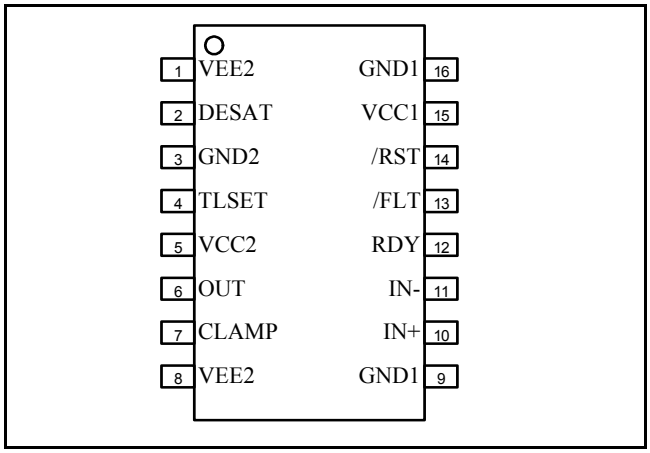


Figure 4: PG-DSO-16-15

3.2 Pin Functionality

GND1
Ground connection of the input side.

IN+ Non inverting driver input
In+ control signal for the driver output if IN- is set to low. (The IGBT is on if IN+ = high and IN- = low)
A minimum pulse width is defined to make the IC robust against glitches at IN+. An internal Pull-Down-Resistor ensures IGBT Off-State.

IN- Inverting driver input
IN- control signal for driver output if IN+ is set to high. (IGBT is on if IN- = low and IN+ = high)
A minimum pulse width is defined to make the IC robust against glitches at IN-. An internal Pull-Up-Resistor ensures IGBT Off-State.

/RST (Reset) input
Function 1: Enable/shutdown of the input chip. (The IGBT is off if /RST = low). A minimum pulse width is defined to make the IC robust against glitches at IN-.
Function 2: Resets the DESAT-FAULT-state of the chip if /RST is low for a time $T_{MINRST2}$. An internal Pull-Up-Resistor is used to ensure FLT status output.

/FLT (Fault output)
Open-drain output to report a desaturation error of the IGBT (FLT is low if desaturation occurs)

RDY (Ready status)
Open-drain output to report the correct operation of the device. (RDY = high if both chips are above the UVLO level and the internal chip transmission is faultless)

VCC1
5V power supply of the input chip

VEE2
Negative power supply pins of the output chip. If no negative supply voltage is available, both pins have to be connected to GND2.

TLSET (Two-Level turn-off)
Setting up the timing and voltage reference for the two-level shutdown (external components needed).
The two-level shutdown is deactivated if TLSET is connected to GND2.

DESAT (Desaturation)
Monitoring of the IGBT saturation voltage (V_{CE}) to detect desaturation caused by short-circuits. If OUT is high, V_{CE} is above a defined value and a certain blanking time has expired, the desaturation protection is activated and the IGBT is switched off. The blanking time is adjustable by an external capacitor.

CLAMP (Clamping)
Ties the gate voltage to ground after the IGBT has been switched off at a defined voltage to avoid a parasitic switch-on of the IGBT.During turn-off, the gate voltage is monitored and the clamp output is activated when the gate voltage goes below 2V (related to VEE2). Additionally, this pin is used to sense the gate voltage for two-level turn-off.

GND2
Reference ground of the output chip.

OUT (Driver output)
Output pin to drive an IGBT. The voltage is switched between VEE2 and VCC2. In normal operating mode Vout is controlled by IN+, IN- and /RST. During error mode (UVLO, internal error or DESAT) Vout is set to VEE2 independent of the input control signals.

VCC2
Positive power supply pin of the output side.

4 Electrical Parameters

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. Unless otherwise noted all parameters refer to GND1.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Positive power supply output side	V_{VCC2}	-0.3	20	V	1)
Negative power supply output side	V_{VEE2}	-12	0.3	V	1)
Maximum power supply voltage output side (V_{VCC2}-V_{VEE2})	V_{max2}	—	28	V	
Gate driver output	V_{OUT}	-0.3	V_{max2}+0.3	V	2)
Gate driver high output maximal current	I_{OUT}	tbd	tbd	A	t = tbd
Gate driver low output maximal current	I_{OUT}	tbd	tbd	A	t = tbd
Maximal short-circuit clamping time	t_{CLP}	—	10	us	$I_{CLAMP/OUT}$ = 500mA
Positive power supply input side	V_{VCC1}	-0.3	6.5	V	
Logic input voltages (IN+,IN-,$\overline{RST}$)	$V_{LogicIN}$	-0.3	6.5	V	
Opendrain Logic output voltage ($\overline{FLT}$)	$V_{\overline{FLT}}$	-0.3	6.5	V	
Opendrain Logic output voltage (RDY)	V_{RDYc}	-0.3	6.5	V	
Opendrain Logic output current ($\overline{FAULT}$)	$I_{\overline{FLT}}$	—	10	mA	
Opendrain Logic output current (RDY)	I_{RDYc}	—	10	mA	
Pin DESAT voltage	V_{DESAT}	-0.3	20		1))V_{VEE2} = -8V
Pin CLAMP voltage	V_{CLAMP}	-0.3	20		1))V_{VEE2} = -8V
Pin TLSET voltage	V_{TLSET}	-0.3	20		1))V_{VEE2} = -8V
Junction temperature	T_J	-40	150	°C	
Storage temperature	T_S	-55	150	°C	
Package power dissipation @TA = 25°C	P_D	—	tbd	mW	
Thermal resistance (both chips active)	R_{THJA}	—	tbd	K/W	
ESD Capability	V_{ESD}	—	2	kV	Human Body Model3)

1) With respect to GND2.

2) With respect to VEE2.

3) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor).

4.2 Operating Parameters

Note: Within the operating range the IC operates as described in the functional description. Unless otherwise noted all parameters refer to GND1.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Positive power supply output side	V_{VCC2}	13	20	V	1)
Negative power supply output side	V_{VEE2}	-12	0	V	1)
Maximum power supply voltage output side (V_{VCC2}-V_{VEE2})	V_{max2}	—	28	V	
Positive power supply input side	V_{VCC1}	4.5	5.5	V	
Logic input voltages (IN+,IN-,$\overline{RST}$)	$V_{LogicIN}$	-0.3	5.5	V	
Pin CLAMP voltage	V_{CLAMP}	-0.3	V_{CC2}	V	
Pin DESAT voltage	V_{DESAT}	-0.3	V_{CC2}	V	
Pin TLSET voltage	V_{TLSET}	-0.3	V_{CC2}	V	1)
Ambient temperature	T_A	-40	105	°C	

1) With respect to GND2.

4.3 Recommended Operating Parameters

Note: Unless otherwise noted all parameters refer to GND1.

Parameter	Symbol	Values	Unit	Remarks
Positive power supply output side	V_{VCC2}	15	V	1)
Negative power supply output side	V_{VEE2}	-8	V	1)
Positive power supply input side	V_{VCC1}	5	V	

1) With respect to GND2.

4.4 Electrical Characteristics

Note: The electrical characteristics involve the spread of values for the supply voltages, load and junction temperatures given below. Typical values represent the median values, which are related to production processes at T = 25°C. Unless otherwise noted all voltages are given with respect to GND.Unless otherwise noted the dynamic characteristics are given without two-level turn-off

4.4.1 Voltage Supply.

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
UVLO Threshold Input Chip	V_{UVLOH1}	—	tbd	4,3	V	
	V_{UVLOL1}	3,5	tbd	—	V	
UVLO Hysteresis Input Chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS1}	0,2	tbd	—	V	
UVLO Threshold Output Chip	V_{UVLOH2}	—	tbd	12,6	V	
	V_{UVLOL2}	10,4	tbd	—	V	
UVLO Hysteresis Output Chip (V_{UVLOH1} - V_{UVLOL1})	V_{HYS2}	0,7	tbd	—	V	
Quiescent Current Input Chip	I_{Q1}	—	tbd	9	mA	V_{VCC1} =5V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High
Quiescent Current Output Chip	I_{Q2}	—	tbd	5	mA	V_{VCC2} =15V V_{VEE2} =-8V IN+ = High, IN- = Low =>OUT = High, RDY = High, /FLT = High

4.4.2 Logic Input and Output

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
IN+,IN-, $\overline{RST}$ Low Input Voltage	V_{IN+L},V_{IN-L},$V_{\overline{RST}L}$	—	—	1.5	V	
IN+,IN-, $\overline{RST}$ High Input Voltage	V_{IN+H},$V_{IN-H}$$V_{\overline{RST}H}$	3.5	—	—	V	
IN-, $\overline{RST}$ Input Current	I_{IN-},$I_{\overline{RST}}$	—	100	400	uA	V_{IN-}=GND1 $V_{\overline{RST}}$=GND1
IN+ Input Current	I_{IN+},	—	100	400	uA	V_{IN+}=VCC1
Minimum Pulse Width IN+, IN-	T_{MININ+}, T_{MININ-}	tbd	40	tbd	ns	
Minimum Pulse Width $\overline{RST}$ for ENABLE/SHUTDOWN	$T_{MINRST1}$	tbd	40	tbd	ns	
Minimum Pulse Width $\overline{RST}$ for Reseting $\overline{FLT}$	$T_{MINRST2}$	tbd	500	tbd	ns	
$\overline{FLT}$ Low Voltage @ I_{SINK}=5mA	V_{FLTL}	—	—	300	mV	
RDY Low Voltage @ I_{SINK}=5mA	V_{RDYL}	—	—	300	mV	

4.4.3 Gate Driver

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
High Level Output Voltage	V_{OUTH1}	tbd	V_{CC2}-0,3	tbd	V	I_{OUTH} = -20mA
	V_{OUTH2}	tbd	V_{CC2}-1,5	tbd	V	I_{OUTH} = -200mA
	V_{OUTH3}	tbd	V_{CC2}-6,0	tbd	V	I_{OUTH} = -2A
High Level Output Peak Current	I_{OUTH}	—	-2	tbd	A	IN+ = High, IN- = Low; OUT = High
Low Level Output Voltage	V_{OUTL1}	tbd	V_{EE2}+0,03	tbd	V	I_{OUTL} = 20mA
	V_{OUTL2}	tbd	V_{EE2}+0,3	tbd	V	I_{OUTL} = 200mA
	V_{OUTL3}	tbd	V_{EE2}+3	tbd	V	I_{OUTL} = 2A
Low Level Output Peak Current	I_{OUTL}	—	2	tbd	A	IN+ = Low, IN- = Low; OUT = Low

4.4.4 Active Miller Clamp

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Low Level Clamp Voltage	$V_{CLAMPL1}$	tbd	V_{EE2}+0,03	tbd	V	I_{OUTL} = 20mA
	$V_{CLAMPL2}$	tbd	V_{EE2}+0,3	tbd	V	I_{OUTL} = 200mA
	$V_{CLAMPL3}$	tbd	V_{EE2}+1.5	tbd	V	I_{OUTL} = 1A
Low Level Clamp Current	I_{CLAMPL}	2	—	—	A	
Clamp Reference Voltage	V_{CLAMP}	—	2	—	V	

4.4.5 Short-Circuit Clamping

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Clamping voltage (OUT)	V_{CLPout}	—	tbd	—	V	IN+=High, IN-=Low, OUT=High I_{OUT} = 500mA (pulse test,t_{CLPmax}=10us)
Clamping voltage (CLAMP)	$V_{CLPclamp}$	—	tbd	—	V	IN+=High, IN-=Low, OUT=High I_{CLAMP} = 500mA (pulse test,t_{CLPmax}=10us)

4.4.6 Dynamic Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Input to output propagation delay[1)]	T_{PDELAY}	tbd	200	tbd	ns	V_{VCC2} =15V,V_{VEE2} =-8V C_{LOAD}= 100pF V_{IN+}=50%, V_{OUT}=50%
Input to output propagation delay with two-level turn-off	$T_{PDELAY2}$	—	T_{PDELAY} + 500	—	ns	V_{VCC2} =15V,V_{VEE2} =-8V C_{LOAD} = 100pF C_{TLSET} < tbd V_{IN+}=50%, V_{OUT}=50%

Input to output propagation distortion[1)]	T_{PDISTO}	—	15	tbd	ns	V_{VCC2} =15V,V_{VEE2} =-8V C_{LOAD}= 100pF V_{IN+}=50%, V_{OUT}=50%
Rise Time[1)]	T_{RISE}	—	60	—	ns	V_{VCC2} =15V,V_{VEE2} =-8V C_{LOAD}= 1nF VL 10% ,VH 90%
		—	400	—	ns	V_{VCC2} =15V,V_{VEE2} =-8V C_{LOAD}= 34nF VL 10% ,VH 90%
Fall Time[1)]	T_{FALL}	—	60	—	ns	V_{VCC2} =15V,V_{VEE2} =-8V C_{LOAD}= 1nF VL 10% ,VH 90%
		—	600	—	ns	V_{VCC2} =15V,V_{VEE2} =-8V C_{LOAD}= 34nF VL 10% ,VH 90%

1) without two-level shutdown

4.4.7 Desaturation protection

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Blanking Capacitor Charge Current	I_{DESATC}	225	250	275	uA	
Blanking Capacitor Discharge Current	I_{DESATD}	—	tbd	—	mA	
Desaturation Reference Level	V_{DESAT}	8,5	9	9,5	V	
Desaturation Sense to OUT Low Delay without Two-Level Turn-Off	$T_{DESATOUT}$	—	—	tbd	ns	V_{OUT} =90%
Desaturation Sense to FLT Low Delay	$T_{DESATFLT}$	—	tbd	1,8	us	$V_{\overline{FLT}}$ =10%; $I_{\overline{FLT}}$ =5mA

4.4.8 Two-level turn-off

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Maximum external Reference Voltage (Zener-Diode)	V_{Zdiode}	—	—	V_{CC2}-1,5	V	
Reference Voltage for setting two-level delay time	V_{TLSET}	—	7	—	V	
Current for setting two-level delay time	I_{TLSET}	—	500	—	uA	
Delaytime of Two-Level Turn-Off	T_{TLSET}	—	2	—	us	C_{TLSET}=100pF V_{Zdiode} = 11.7V

4.4.9 Active Shut Down

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Active Shut Down Voltage	V_{ACTSD} [1)]	—	—	3	V	I_{OUT}=-200mA, V_{CC2} open

1) With reference to V_{EE2}

5 VDE 0884-10 (Draft) Isolation Characteristics

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 150 V_{RMS} for rated mains voltage ≤ 300 V_{RMS} for rated mains voltage ≤ 600 V_{RMS}		 I-IV I-III I-II	
Climatic Classification		55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	
Maximum Working Insulation Voltage	V_{IORM}	891	V_{PEAK}
Input to Output Test Voltage, Method b[1)] V_{IORM} * 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5pC	V_{PR}	1670	V_{PEAK}
Input to Output Test Voltage, Method a[1)] V_{IORM} * 1.5 = V_{PR}, Type and sample Test, t_m = 60 sec, Partial Discharge < 5pC	V_{PR}	1336	V_{PEAK}
Highest Allowable Overvoltage[1)] (Transient Overvoltage t_{ini} = 10 sec)	V_{IOTM}	6000	V_{PEAK}
Safety-limiting values - maximum values allowed in the event of a failure Case Temperature Input Power Output Power	 T_s $P_{S,INPUT}$ $P_{S,OUTPUT}$	 175 400 1200	 °C mW mW
Insulation Resistance at T_s, V_{IO} = 500 V	R_S	$>10^9$	Ω

1) VDE 0884 for a detailed description of Method a and Method b partial discharge test profiles.

6 Timing Diagrams

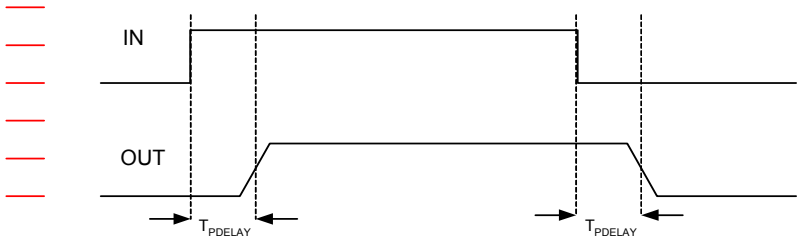
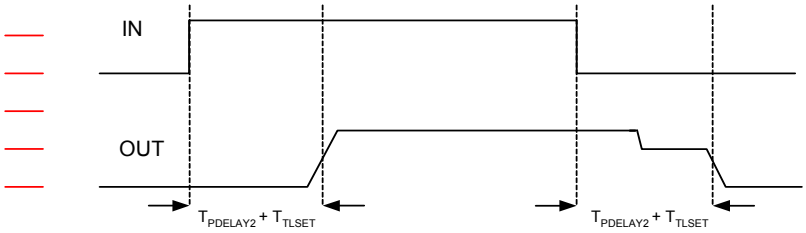


Figure 5: propagation delay without two-level turn-off



$$T_{TLSET} = \frac{C_{TLSET}(external) * V_{TLSET}}{I_{TLSET}}$$

Figure 6: propagation delay with two-level turn-off

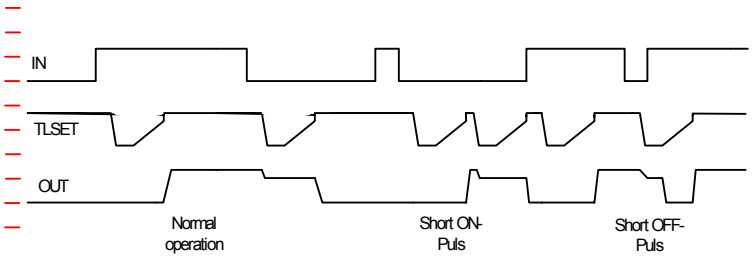


Figure 7: two-level turn-off

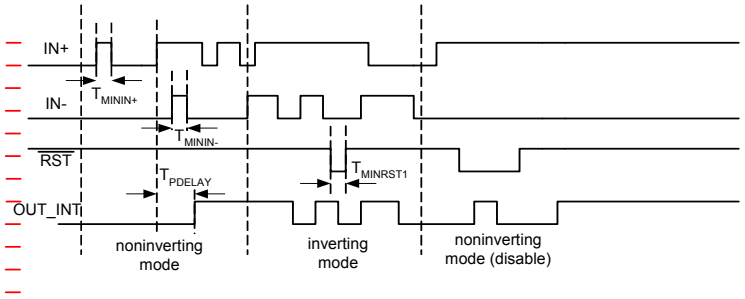


Figure 8: turn-on and turn-off

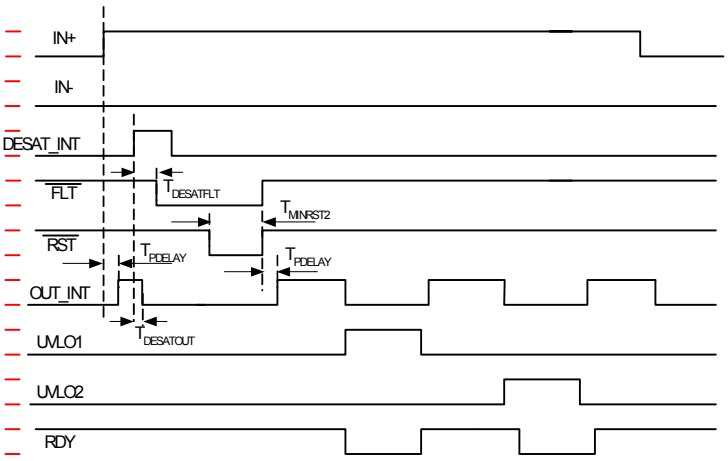
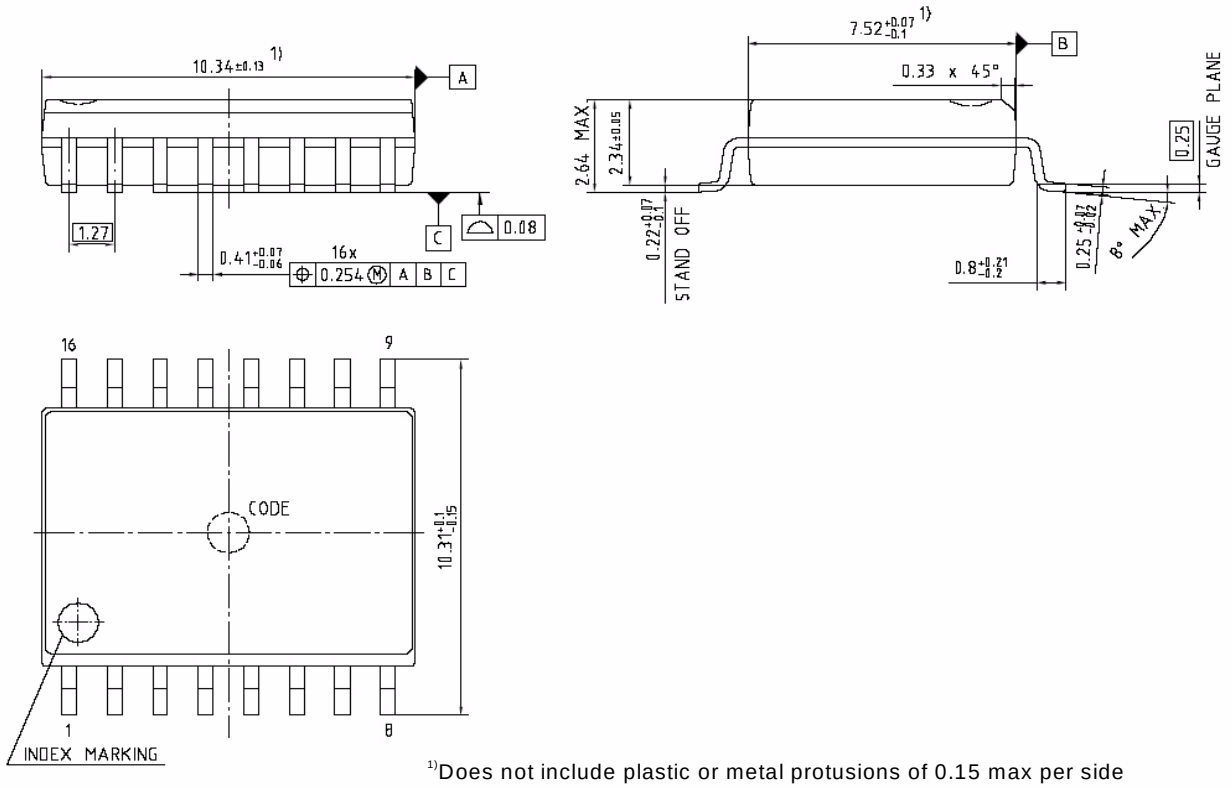


Figure 9: desaturation fault and UVLO

7 Package Outlines

PG-DSO-16-15

(Plastic Dual Small Outline Package)



[1] Does not include plastic or metal protusions of 0.15 max per side

Figure 10: PG-DSO-16-15

Total Quality Management

Qualität hat für uns eine umfassende Bedeutung. Wir wollen allen Ihren Ansprüchen in der bestmöglichen Weise gerecht werden. Es geht uns also nicht nur um die Produktqualität – unsere Anstrengungen gelten gleichermaßen der Lieferqualität und Logistik, dem Service und Support sowie allen sonstigen Beratungs- und Betreuungsleistungen.

Dazu gehört eine bestimmte Geisteshaltung unserer Mitarbeiter. Total Quality im Denken und Handeln gegenüber Kollegen, Lieferanten und Ihnen, unserem Kunden. Unsere Leitlinie ist jede Aufgabe mit „Null Fehlern“ zu lösen – in offener Sichtweise auch über den eigenen Arbeitsplatz hinaus – und uns ständig zu verbessern.

Unternehmensweit orientieren wir uns dabei auch an „top“ (Time Optimized Processes), um Ihnen durch größere Schnelligkeit den entscheidenden Wettbewerbsvorsprung zu verschaffen.

Geben Sie uns die Chance, hohe Leistung durch umfassende Qualität zu beweisen.

Wir werden Sie überzeugen.

Quality takes on an allencompassing significance at Semiconductor Group. For us it means living up to each and every one of your demands in the best possible way. So we are not only concerned with product quality. We direct our efforts equally at quality of supply and logistics, service and support, as well as all the other ways in which we advise and attend to you.

Part of this is the very special attitude of our staff. Total Quality in thought and deed, towards co-workers, suppliers and you, our customer. Our guideline is “do everything with zero defects”, in an open manner that is demonstrated beyond your immediate workplace, and to constantly improve.

Throughout the corporation we also think in terms of Time Optimized Processes (top), greater speed on our part to give you that decisive competitive edge.

Give us the chance to prove the best of performance through the best of quality – you will be convinced.

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