PM8374A

DualPHY™ 1G

2 CHANNEL PHYSICAL LAYER TRANSCEIVER WITH GIGABIT ETHERNET PCS FOR 933 Mbit/s TO 1.25 Gbit/s INTERFACES

Data Sheet

Released

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Patents

Granted

The technology discussed in this document is protected by one or more of the following patent grants:

U.S. Patent No. 6,316,977B1, 6,552,619

Revision History

Issue No.	Issue Date	Details of Change
1	May 2004	Initial release.

Table of Contents

List of Registers

List of Figures

List of Tables

1 Definitions

The following table defines terms and abbreviations used in this document.

Table 1 Definitions

Term	Definition
ANSI	American National Standards Institute
ASIC	Application Specific Integrated Circuit
BIST	Built-in Self Test
CABGA	Chip Array Ball Grid Array
CMOS	Complementary Metal-oxide Silicon
COL	Collision Detect.
CRS	Carrier Sense
DDR	Dual Data Rate
FIFO	First In, First Out
GMII	Gigabit Medium-Independent Interface
IEEE	Institute of Electrical and Electronics Engineers
IPG	Interpacket Gap
JTAG	Joint Test Action Group
MDC/MDIO	Management Data Clock/Management Data Input/Output
PCS	Physical Coding Sublayer

2 Features

General

- Two 933 Mbit/s to 1.25 Gbit/s IEEE 802.3-2000 Gigabit Ethernet and Fibre Channel Physical Interfaces (FC-PI) System Compliant Transceivers
- Two secondary channels to support channel redundancy
- Integrated clock synthesis, clock recovery, serializer/deserializer, built-in self-test, 8B/10B codec and IEEE 802.3-2000 Gigabit Ethernet Physical Coding Sublayer (PCS) logic
- Rate matching via IDLE character insertion and deletion capable of compensating up to ±200 ppm of difference between the local REFCLK and the incoming data
- Pin-programmable or software-configurable operation using two-pin IEEE 802.3 MDC/MDIO serial management interface
- Ultra-low power operation using 0.18µ technology

Serial Interface

- High-speed outputs feature programmable output current to optimize drive distance and power - directly drives 50 Ω (100 Ω differential) systems
- Direct AC coupled interface to copper serial backplanes, optics and coaxial cable
- Low threshold receive differential input threshold

Parallel Interface

- SDR parallel interface with synchronous receive clock (clock forwarding)
- Half Rate Mode that supports Dual Data Rate
- Supports GMII and TBI (Ten-bit Interface) standards.
- Receive channel output clocks eliminate the need for PLLs in interface ASICs
- 1.8 V and 2.5 V interoperable; 3.3 V tolerant

Test Features

- IEEE 1149.1 JTAG Boundary Scan support
- Built-in self-test (BIST) via internal packet generator/checker
- Per-channel control of serial and parallel loopback
- 8B/10B error counters

Physical

- Thermally enhanced 289-pin, 19mm x 19mm CABGA Package

3 Applications

- High-speed serial backplanes
- IEEE 802.3-2000 Gigabit Ethernet dense line cards
- ANSI X3T11 Fibre Channel dense line cards
- Link Aggregation
- Intra-system and inter-system interconnect
- Chassis Extender

4 References

1. IEEE 802.3-2000 Gigabit Ethernet, 2000 Edition

2. Methodologies for Jitter and Signal Quality Specification (MJSQ) Rev. 4.0

3. Fibre Channel Physical Interfaces (FC-PI) Rev. 13

4. IEEE 1149.1-2001 Standard Test Access Port and Boundary Scan Architecture, 23 July 2001.

5. PMC-2012433, QuadPHY 1G Telecom Standard Product Data Sheet

6. PMC-2030175, Octal/QuadPHY 1G Board Level Design and Debug Tips

7. PMC-2012358, OctalPHY 1G/QuadPHY 1G Evaluation Board Design

8. PMC-2022181, OctalPHY/QuadPHY 1G Evaluation Kit User's Guide

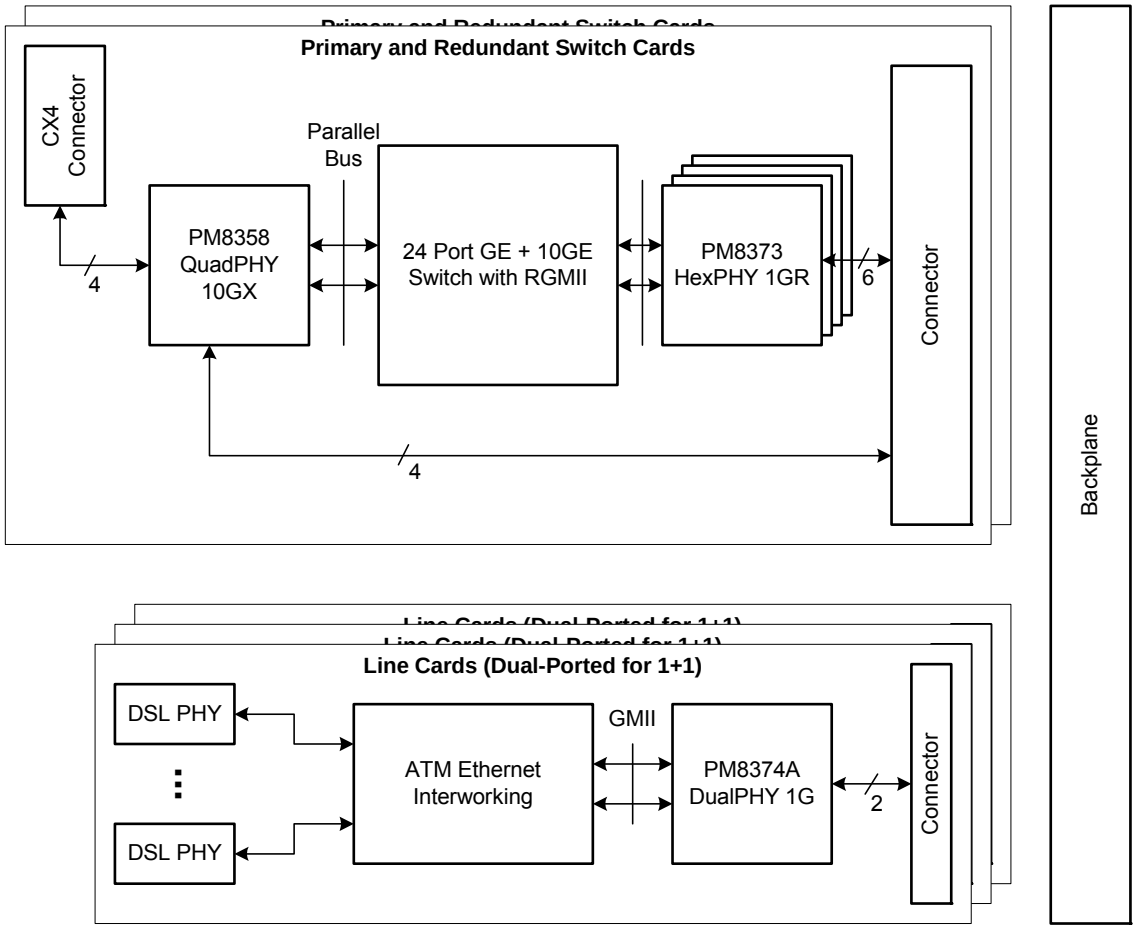
5 Application Examples

The DualPHY™ 1G device has numerous applications in networking, storage and computing systems requiring high-speed serial I/O technology. Typical applications include backplane interconnect, Gigabit Ethernet line cards and Fiber Channel line cards.

5.1 Next Generation IP-DSLAM Application

Figure 1 shows the DualPHY 1G device being used in a next-generation IP-DSLAM application. On the line cards, the DualPHY 1G provides a high-speed backplane interconnect.

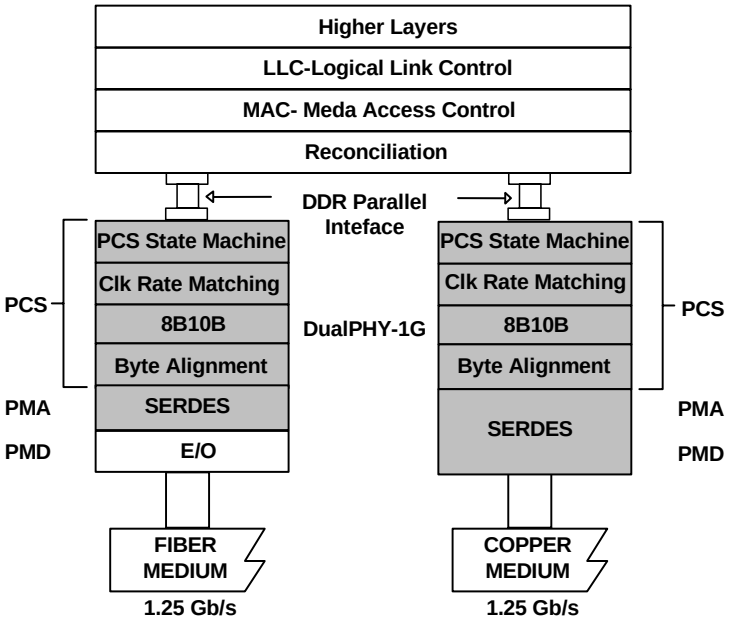
Figure 1 DualPHY 1G in Next Generation IP-DSLAM Applications



5.2 IEEE 802.3-2000 Gigabit Ethernet Transceiver

As a Gigabit Ethernet Transceiver, the DualPHY 1G device integrates the PCS layer down to the PMA layer for fiber mediums and down to the PMD layer for copper mediums. Figure 2 shows in gray shade, the supported functions of the device. The DualPHY 1G device may be configured to enable or disable certain layers.

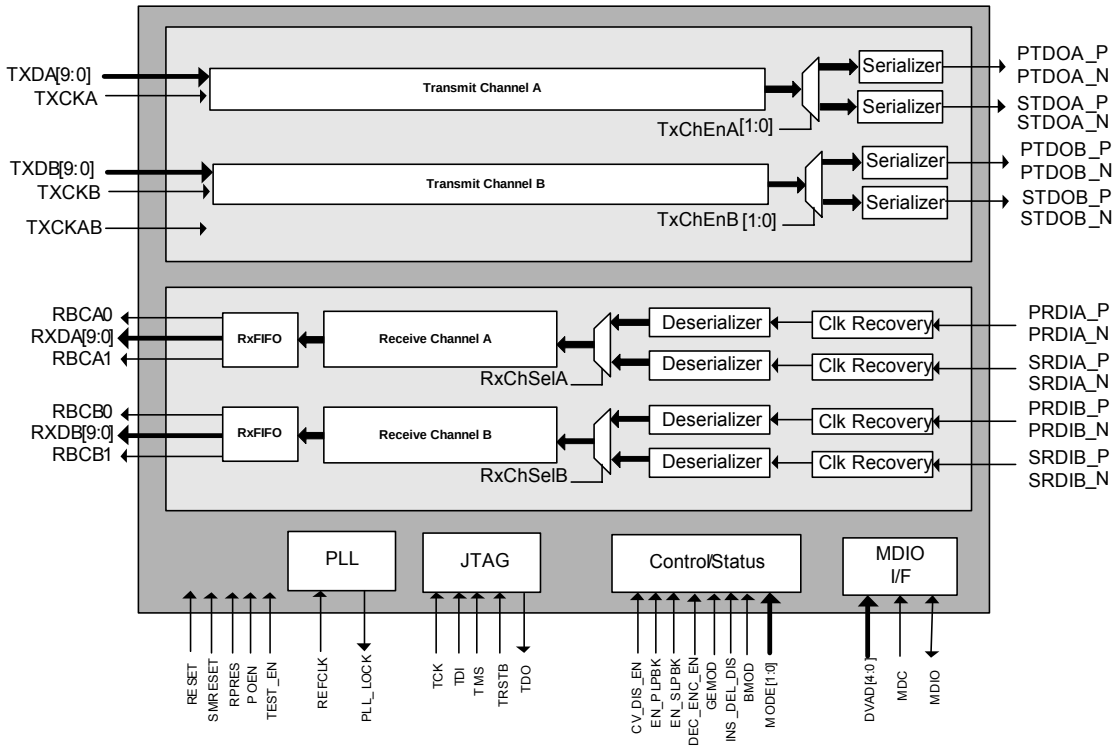
Figure 2 IEEE 802.3-2000 Gigabit Ethernet Supported Functions



6 Block Diagram

The block diagram of the DualPHY 1G device is shown in Figure 3.

Figure 3 DualPHY 1G Block Diagram



7 Description

7.1 Overview

The PM8374A DualPHY 1G device is a low-power two-channel transceiver suitable for applications such as high-speed serial backplanes and dense Gigabit Ethernet line cards.

In the transmit direction, the PM8374A takes 8-bit or 10-bit data, serializes the data and transmits it differentially at rates between 933 Mbit/s and 1.25 Gbit/s. The PM8374A integrates a SDR/DDR parallel interface, 8B/10B encoder, IEEE 802.3-2000 Gigabit Ethernet PCS logic, serializer, clock synthesis unit, and differential transmitters.

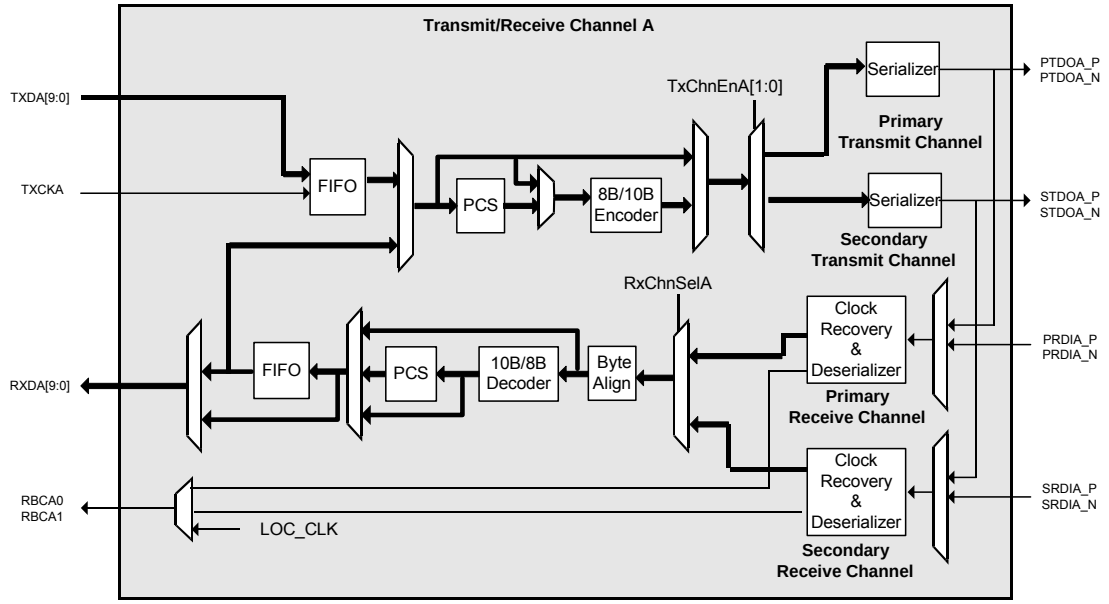
In the receive direction, the PM8374A receives serial differential data, recovers the data and converts the data back to 8-bit or 10-bit data. The PM8374A integrates differential receivers, clock recovery unit, PCS logic, 8B/10B decoder, receive FIFOs, and an SDR/DDR parallel interface.

A system requires rate compensation if the transmitting device and receiving device are operating from different clock sources (asynchronous system). For example, if two asynchronous 1.25 Gbit/s links from two line cards are transmitting over a backplane to one receiving device, the receiving device must provide rate compensation to achieve a common local clock. The receive logic compensates for these clock differences by inserting or deleting special 8B/10B IDLE characters.

The DualPHY 1G device provides redundant serial transmit and serial receive ports. The active port can be selected through the Management Interface for each pair of transmit and receive ports.

The PM8374A has two primary channels and two secondary channels (A and B). Figure 4 shows a detailed block diagram of channel A's primary and secondary channels. The block diagram of channel B is identical to channel A's primary and secondary channels.

Figure 4 DualPHY 1G Detailed Channel Block Diagram



The DualPHY 1G device supports IEEE 802.3-2000 Gigabit Ethernet and Fibre Channel Physical Interfaces (FC-PI) Rev. 13. The high-speed outputs feature programmable output current that enables directly driving 50 Ω (100 Ω differential) systems. This allows direct interface to optical modules, coax, or serial backplanes.

The DualPHY 1G device supports a Single Data Rate (SDR) or a Dual Data Rate (DDR) Parallel Interface with independent receive and transmit ports. Depending on which mode of operation is being used, the DualPHY 1G parallel interface will operate as an SDR interface or a DDR interface. Section 10.1, Modes of Operation, describes these interfaces in detail.

The selection of interface modes, as well as operating features such as the internal 8B/10B encoding/decoder, full duplex PCS, frequency compensation, and parallel loopback can be done via the two-pin serial MDC/MDIO management interface or through external pins for systems that do not support MDC/MDIO.

A two-pin serial management interface using IEEE 802.3 MDC/MDIO protocol for configuration and diagnostic access is also provided. The DualPHY 1G device supports various loopback modes for testing and debug including individual serial channel loopback. Support for built-in self test (BIST) via an internal packet generator/checker is also provided on a per-transceiver basis.

The part is produced in 0.18 µm, 1.8 V CMOS technology with compatible 1.8/2.5 V I/Os. IEEE 1149.1 JTAG is fully supported and the 289-pin CABGA package has a small 19x19 mm footprint.

8 Pin Diagram

The DualPHY 1G device is packaged in a 289-ball Chip Array Ball Grid Array (CABGA) package having a body size of 19 mm by 19 mm. Figure 5 shows the bottom view of the pin diagram of the DualPHY 1G device.

Figure 5 DualPHY 1G Pin Diagram (Bottom View)

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	GND	PTDOB_P	PTDOB_N	GND	TXDB[8]	TXDB[6]	TXDB[4]	TXDB[2]	TXDB[0]	TXDA[8]	TXDA[6]	TXDA[4]	TXDA[2]	TXDA[0]	GND	GND	GND	A
B	GND	STDOB_P	STDOB_N	GND	TXDB[9]	TXDB[7]	TXDB[5]	TXDB[3]	TXDB[1]	TXDA[9]	TXDA[7]	TXDA[5]	TXDA[3]	TXDA[1]	GND	GND	GND	B
C	GND	PTDOA_P	PTDOA_N	GND	RPRES	REFCLK	TMS	TCK	TDI	GEMOD	TDO	TXCKB	TXCKA	GND	GND	GND	GND	C
D	GND	STDOA_P	STDOA_N	GND	POEN	DVAD[4]	DVAD[3]	NC	NC	TRSTB	EN_SLPBK	NC	NC	NC	GND	GND	GND	D
E	GND	NC	NC	GND	VDD	VDD	VDD	VDD	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	GND	TXCKAB	GND	GND	E
F	GND	NC	NC	GND	VDD	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	VDDQ	GND	NC	GND	GND	F
G	GND	NC	NC	GND	VDD	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	VDDQ	GND	RESET	GND	GND	G
H	GND	NC	NC	GND	VDD	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	VDDQ	GND	MDC	GND	GND	H
J	GNDA	GNDA	VDDA	VDDA	VDD	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	VDDQ	GND	CV_DIS_EN	DEC_ENC_EN	MDIO	J
K	GND	PRDIB_P	PRDIB_N	GND	VDD	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	VDDQ	GND	NC	NC	NC	K
L	GND	SRDIB_P	SRDIB_N	GND	VDD	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	VDDQ	GND	SMRESET	NC	NC	L
M	GND	PRDIA_P	PRDIA_N	GND	VDD	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	T_GND	VDDQ	GND	INS_DEL_DIS	NC	NC	M
N	GND	SRDIA_P	SRDIA_N	GND	VDD	VDD	VDD	VDD	VDDQ	VDDQ	VDDQ	VDDQ	VDDQ	GND	ENPLBPBK	NC	NC	N
P	GND	GND	GND	GND	DVAD[2]	MODE[1]	MODE[0]	NC	BMOD	NC	NC	NC	NC	NC	NC	NC	NC	P
R	GND	GND	GND	GND	DVAD[1]	DVAD[0]	PLL_LOCK	RBCB1	RBCB0	RBCA1	RBCA0	NC	NC	NC	NC	NC	NC	R
T	GND	GND	GND	GND	RXDB[9]	RXDB[7]	RXDB[5]	RXDB[3]	RXDB[1]	RXDA[9]	RXDA[7]	RXDA[5]	RXDA[3]	RXDA[1]	NC	NC	NC	T
U	GND	GND	GND	GND	RXDB[8]	RXDB[6]	RXDB[4]	RXDB[2]	RXDB[0]	RXDA[8]	RXDA[6]	RXDA[4]	RXDA[2]	RXDA[0]	NC	NC	NC	U
	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

9 Pin Description

The following tables describe all pins of the DualPHY 1G device.

Table 2 Receive Path Pins

Pin Name	Type	Pin No.	Function
SRDIA_P SRDIA_N PRDIA_P PRDIA_N SRDIB_P SRDIB_N PRDIB_P PRDIB_N	Input High-speed Differential	N16 N15 M16 M15 L16 L15 K16 K15	Differential, high-speed serial **Receive Data Input pins**. This data must be 8B/10B line coded and operate in the range from 933 Mbit/s and 1.25 Gbit/s. The differential inputs are internally terminated with 100 Ω differential terminations. These ports are ignored when Serial Loopback is enabled using either the EN_SLPBK input or the INT_EN_SERIAL_LPBK [B:A] bits in Loopback Register (Register 0x16). These inputs are enabled by default. If a channel is enabled, active data must be provided to it. Do not use pull-up/pull-down resistors on the high-speed differential inputs. These inputs may be left unconnected when this channel is not used.
RBCA0	Output CMOS	R7	In HRRC Mode, the Receive Backplane Channel A0 clock is 180 degrees out of phase with the RBCA1 clock. In HRRC Mode, the rising edge of RBCA0 can be used to sample odd data on RXDA[9:0]. In RRRC mode, the RBCA0 pin is not used and should be left unconnected. While in LRRC or Parallel Loopback Mode, the RXCLK4 bit in Register 0x18 PMC Control 3 determines whether the RBCA0 pin is active or inactive.
RBCA1	Output CMOS	R8	In HRRC or RRRC Mode, the Receive Backplane Channel A1 clock is the receive clock for Channel A. In RRRC mode the rising edge of RBCA1 can be used to sample RXDA[9:0]. In HRRC Mode, the rising edge of RBCA1 can be used to sample even data on RXDA[9:0]. While in LRRC or Parallel Loopback Mode, the RXCLK4 bit in Register 0x18 PMC Control 3 determines whether the RBCA1 pin is active or inactive.

Pin Name	Type	Pin No.	Function
RXDA[9] RXDA[8] RXDA[7] RXDA[6] RXDA[5] RXDA[4] RXDA[3] RXDA[2] RXDA[1] RXDA[0]	Output CMOS	T8 U8 T7 U7 T6 U6 T5 U5 T4 U4	Parallel **Receive Data Backplane** from primary or secondary channel **A (PRDIA_P, PRDIA_N or SRDIA_P, SRDIA_N).** When PCS_ENABLE is 1, this data may optionally be 8B/10B decoded. If decoded, Bits 9:0 of RXDA are defined as (Error Bit + K Bit + Data[7:0]). Data that appears here is provided in an SDR fashion when operating in LRRC or RRRC modes and in a DDR fashion when operating in HRRC Mode. RXDA0 represents the first bit of the word received on the differential pairs PRDIA_P, PRDIA_N or SRDIA_P, SRDIA_N. When in LRRC Mode, RXDA[9:0] is updated using either the rising edges of RBCA1 or RBCB1 depending on the state of control bit RXCLK4. When in RRRC Mode, RXDA[9:0] is updated using the rising edges of RBCA1. For HRRC Mode, RXDA[9:0] is updated using both the rising edges of RBCA1 and RBCA0.
RBCB0	Output CMOS	R9	In HRRC Mode, the Receive Backplane Channel D0 clock is 180 degrees out of phase with the RBCD1 clock. In HRRC Mode, the rising edge of RBCB0 can be used to sample odd data on RXDB[9:0]. In RRRC mode, the RBCB0 pin is not used and should be left unconnected. While in LRRC or Parallel Loopback Mode, the RBCB0 pin is the complementary clock that RXDA[9:0] and RXDB[9:0],] are referenced to. The RXCLK4 bit 4 in Register 0x18 PMC Control 3 determines whether the RBCB0 signal is output on the RBCA0 clock output.
RBCB1	Output CMOS	R10	In HRRC or RRRC Mode, the Receive Backplane Channel B1 clock is the receive clock for Channel B. In RRRC mode the rising edge of RBCB1 can be used to sample RXDB[9:0]. In HRRC Mode, the rising edge of RBCB1 can be used to sample even data on RXDB[9:0]. While in LRRC or Parallel Loopback Mode, the RDCB1 pin is the clock that RXDA[9:0] and RXDB[9:0] are referenced to. The RXCLK4 bit in Register 0x18, PMC Control 3, determines whether the RBCb1 signal is output on the RBCA1 clock output.
RXDB[9] RXDB[8] RXDB[7] RXDB[6] RXDB[5] RXDB[4] RXDB[3] RXDB[2] RXDB[1] RXDB[0]	Output CMOS	T13 U13 T12 U12 T11 U11 T10 U10 T9 U9	Parallel **Receive Data Backplane** from primary or secondary channel **B (PRDIB_P, PRDIB_N or SRDIB_P, SRDIB_N).** When PCS_ENABLE is 1, this data may optionally be 8B/10B decoded. If decoded, Bits 9:0 of RXDB are defined as (Error Bit + K Bit + Data[7:0]). Data that appears here is provided in a SDR fashion when operating in LRRC or RRRC modes and in a DDR fashion when operating in HRRC Mode. RXDB0 represents the first bit of the word received on the differential pairs PRDIB_P, PRDIB_N or SRDIB_P, SRDIB_N. When in LRRC or RRRC Mode, RXDB[9:0] is updated using the rising edges of RBCB1. For HRRC Mode, RXDB[9:0] is updated using both the rising edges of RBCB1 and RBCB0.

Table 3 Transmit Path Pins

Pin Name	Type	Pin No.	Function
STDOA_P STDOA_N PTDOA_P PTDOA_N STDOB_P STDOB_N PTDOB_P PTDOB_N		D16 D15 C16 C15 B16 B15 A16 A15	Differential, high-speed serial **Transmit Data Output** pins. This data is operating from between 933 Mbit/s and 1.25 Gbit/s and is 8B/10B encoded. The differential outputs are internally terminated with 100-ohm differential terminations. These outputs are inactive when serial loopback is enables. These outputs are enabled by default. Do not use pull-up or pull-down resistors on the high-speed differential outputs. The outputs may be left unconnected if this channel is not used.
TXCKAB	Input CMOS	E3	Parallel **Transmit Clock for Channel A and B**. TXCKAB is used to clock in data for both of the input parallel transmit ports TXDA and TXDB (default configuration). Optionally, when the TXCLK4 bit in the PMC Control 2 register is set to logic 1, TXDA[9:0] is sampled by TXCKA and TXDB[9:0] is sampled by TXCKB. If this pin is not used, it should be tied to ground.
TXCKA	Input CMOS	C5	Parallel **Transmit Clock for Channel A**. The rising edges of TXCKA are used to clock in TXDA[9:0]. TXCKA can be used to clock in data for TXDA when the TXCLK4 bit in the PMC Control 2 register is set to logic 1. The default configuration (TXCLK4=0) is for TXCKAB to clock in data for both of the input parallel transmit ports TXDA and TXDB. If this pin is not used, it should be tied to ground.
TXDA[9] TXDA[8] TXDA[7] TXDA[6] TXDA[5] TXDA[4] TXDA[3] TXDA[2] TXDA[1] TXDA[0]	Input CMOS	B8 A8 B7 A7 B6 A6 B5 A5 B4 A4	Parallel **Transmit Data Backplane** to primary or secondary channel **A (PTDOA_P, PTDOA_N or STDOA_P, STDOA_N)**. This data can optionally be 8B/10B encoded. If encoded, Bits 9:0 of TXDA are defined as (Reserved Bit + K Bit + Data[7:0]). Data that appears here is provided in a SDR fashion regardless of operating mode. In all modes of operation, TXDA0 represents the first bit of the word that is transmitted on the differential pairs PTDOA_P, PTDOA_N and STDOA_P, STDOA_N. In all modes of operation, either TXCKA or TXCKAB is used to load in data using its rising edges, depending on the state of control bit TXCLK4. If these pins are not used, they should be tied to ground.

Pin Name	Type	Pin No.	Function
TXCKB	Input CMOS	C6	Parallel **Transmit Clock for Channel B**. The rising edges of TXCKB are used to clock in TXDB[9:0]. TXCKB can be used to clock in data for TXDB when the TXCLK4 bit in PMC Control 2 Register is set to logic 1. The default configuration (TXCLK4=0) is for TXCKAB to clock in data for both of the input parallel transmit ports TXDA and TXDB. If this pin is not used, it should be tied to ground.
TXDB[9] TXDB[8] TXDB[7] TXDB[6] TXDB[5] TXDB[4] TXDB[3] TXDB[2] TXDB[1] TXDB[0]	Input CMOS	B13 A13 B12 A12 B11 A11 B10 A10 B9 A9	Parallel **Transmit Data Backplane** to primary or secondary channel **B (PTDOBD_P, PTDOB_N or STDOB_P, STDOB_N)**. This data can optionally be 8B/10B encoded. If encoded, Bits 9:0 of TXDB are defined as (Reserved Bit + K Bit + Data[7:0]). Data that appears here is provided in an SDR fashion regardless of operating mode. In all modes of operation, TXDB0 represents the first bit of the word that is transmitted on the differential pairs PTDOB_P, PTDOB_N and STDOB_P, STDOB_N. In all modes of operation, either TXCKB or TXCKAB is used to load in data using its rising edges, depending on the state of control bit TXCLK4. If these pins are not used, they should be tied to ground

Table 4 MDC/MDIO Pins

Pin Name	Type	Pin No.	Function
DVAD[4] DVAD[3] DVAD[2] DVAD[1] DVAD[0]	Input CMOS	D12 D11 P13 R13 R12	SERDES **Device Address**. Pins DVAD[4:2] define the base device address of the DualPHY 1G device. Pins DVAD[1:0] are not used and should be tied to logic 0. The MDC/MDIO protocol addresses this device when the 3 MSBs of the PHYAD address match pins DVAD[4:2]. The two LSBs of the MDC/MDIO protocol PHYAD address point to the specific SERDES within the device.
MDIO	Input/Output CMOS	J1	**Management Data Input/Output**. This terminal is the management interface (MI) serial port. During MI write cycles, input data is placed on this terminal and sampled by MDC. During a MI read cycle the MDIO terminal outputs management interface register information. Input data is sampled on the rising edge of MDC. Input and output data on this terminal is referenced to the rising edge of MDC. Note that MDIO should be externally pulled up to VDDQ with a 10 kΩ resistor for proper operation between accesses.
MDC	Input CMOS	H3	**Management Data Clock**. Used to control data transfer to/from the management interface registers. Management interface input data is sampled on the rising edges of MDC. When data is to be output on the MDIO terminal it is referenced to the rising edge of MDC. MDC can be aperiodic. The presence of a clock on REFCLK is required for proper operation of the MDC/MDIO interface.

Table 5 Configuration/Status Pins

Pin Name	Type	Pin No.	Function
CV_DIS_EN	Input CMOS	J3	**Code Violation/Disparity Error Code Enable** (Active high). This static signal must be pulled high or low prior to deasserting RESET. Enables the error code option. If a code violation or disparity error is detected, the outputs RXDy[9:0] are set to 1. This option requires that the decoder be enabled. This terminal is logically OR'd with the CODE_VIOL_DIS_ENABLE bit (Register 0x11).When not asserted, the CV bit indicates the disparity error.
DEC_ENC_EN	Input CMOS	J2	**Decoder/Encoder Enable** (Active high). This static signal must be pulled high or low prior to deasserting RESET. Enables the internal 8B/10B encoder/ decoder across all channels. When set to 0, the device processes 10B encoded data only. This terminal is logically OR'd with the INT_DEC_ENC_ENABLE(7) bit (Register 0x11); i.e., the INT_DEC_ENC_ENABLE(7) bit must be low in order for this pin to function.
EN_SLPBK	Input CMOS	D7	**Enable Serial Data Loop-back** (Active high). This static signal must be pulled high or low prior to deasserting RESET. Enables the loop-back function for serial data. When high, serial data is routed from the output of the serializer block to the input of the clock recovery block for each channel. The TDOy_P/TDOy_N serial outputs are held at a logical 1 state. The RDIy_P/RDIy_N serial inputs are ignored. Should be held low for normal operation.
SMRESET	Input Pulldown CMOS	L3	This active-high **State Machine Reset** signal provides an asynchronous DualPHY 1G reset to all state machine flip flops. It has no affect on the PLL or the configuration and status flip flops accessible by the MDC/MDIO port. The minimum reset assertion time is typically less than 500 ns. This terminal is logically ORed with the Soft_Reset bit (Register 0x11) and provides the same functionality.
INS_DEL_DIS	Input Pulldown CMOS	M3	**Insert/Delete Disable**. This static signal must be pulled high or low prior to deasserting RESET. When low, the DualPHY 1G device performs frequency compensation on incoming data. When high, frequency compensation is disabled.
ENPLPBK	Input Pulldown CMOS	N3	**Enable Parallel Loopback**. This static signal must be pulled high or low prior to deasserting RESET. When high, the DualPHY 1G device internally connects all receive channel parallel ports to their corresponding transmit parallel ports. Data is still sent to the parallel outputs. When low, this connection is broken.

Pin Name	Type	Pin No.	Function
GEMOD	Input Pulldown CMOS	C8	**Gigabit Ethernet Mode** (active high) When asserted, the device will: 1. Configuration words that pass through the PHY during the Auto-Negotiation process may be inserted/deleted for frequency compensation 2. /K28.5/ followed by any non-K character are recognized as an IDLE sequence which can be inserted or deleted for frequency compensation (except when BMOD is asserted, chip will treat /K28.5/D10.1/ as described in BMOD pin description) 3. Modify IDLE to correct disparity by substituting /D5.6/ for /D16.2/ in a /K28.5/ Dx.y/ transmit IDLE pair. GEMOD is OR'd with GE_REG. PCS_ENABLE must be set to 0 when GE_REG = 1. See Register 0x18, Bit 15 for additional information. This static signal must be pulled high or low prior to deasserting RESET.
BMOD	Input Pulldown CMOS	P9	**Busy Bit Mode**, active high. This static signal must be pulled high or low prior to deasserting RESET. When asserted, the K28.5/D10.1 adjacent pair will be treated as valid data and passed through the FIFO. When deasserted, it will be treated as an IDLE sequence and can be deleted. This pin is valid only when GEMOD is asserted. BMOD is OR'ed with BUSY_REG.
MODE1 MODE0	Input CMOS	P12 P11	**Mode Selector** bits. This static signal must be pulled high or low prior to deasserting RESET. The MODE[1:0] input selects the interface mode according to the table below. Also see Register 0x11. Mode — Description 00 — Locally Referenced Receive Clock (LRRC) Mode 01 — Reserved 10 — Remotely Referenced Receive Clock (RRRC) Mode 11 — Half-rate Receive Clock (HRRC) Mode
REFCLK	Input CMOS	C12	**Reference Clock**. Requires an accurate, low jitter, 100 ppm for frequencies between 93.3 and 125 MHz reference clock. The clock synthesis PLL uses REFCLK to generate a phase locked 10X internal clock. The PLL expects an uninterrupted reference clock. If the reference clock is disrupted for any duration of time, a hardware reset maybe necessary to allow the PLL to fully recover. REFCLK is referenced to VDDQ voltage levels (see the D.C Characteristics Section for details about Vol and Voh logic thresholds). The presence of a clock on REFCLK is required for proper operation of the MDC/MDIO interface.
PLL_LOCK	Output CMOS	R11	**PLL Lock** is an external indication that the internal clock synthesis PLL has locked to REFCLK.

Pin Name	Type	Pin No.	Function
RESET	Input CMOS	G3	The active-high **Reset** (RESET) signal provides an asynchronous DualPHY 1G reset to all flip-flops. The minimum reset assertion time is 500 ns.

Table 6 JTAG Pins

Pin Name	Type	Pin No.	Function
TCK	Input CMOS	C10	The **Test Clock** (TCK) signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TDI	Input CMOS Pullup	C9	The **Test Data Input** (TDI) signal carries test data into the DualPHY 1G device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an integral pull-up resistor.
TMS	Input Pullup CMOS	C11	The **Test Mode Select** (TMS) signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an integral pull-up resistor.
TRSTB	Input CMOS	D8	The active-low **Test Reset** (TRSTB) signal provides an asynchronous DualPHY 1G test access port reset via the IEEE P1149.1 test access port. TRSTB must be pulled low during normal device operation. This places the JTAG logic into the reset state.
TDO	Output Tristate CMOS	C7	The **Test Data Output** (TDO) signal carries test data out of the DualPHY 1G device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. TDO is a tristate output which is inactive except when scanning of data is in progress.

Table 7 Miscellaneous Pins

Pin Name	Type	Pin No.	Function
NC	No Connect	D4 D5 D6 D9 D10 E15 E16 F3 F15 F16 G15 G16 H15 H16 K1 K2 L1 L2 M1 M2 N1 N2 P1 P2 P3 P4 P5 P6 P7 P8 P10 R1 R2 R3 R4 R5 R6 T1 T2 T3 U1 U2 U3	**Not Connected**. These pins should be left floating.
POEN	Input CMOS	D13	**Parallel Output Enable** (active high). Tristates all the parallel output data drivers (RXDy[9:0]) and clock drivers (RXCy) when low.
NC	Input Pulldown CMOS	K3	Reserved for PMC Test Purposes. Must be left unconnected.
RPRES	Analog Bias	C13	Terminal for a **Precision Resistor** of 10k 1% reference resistor is connected between this terminal and ground. This sets the internal reference current sources.

Table 8 Digital Power and Digital Ground Pins

Pin Name	Type	Pin No.	Function
VDD	Power Digital Core	E10 E11 E12 E13 F13 G13 H13 J13 K13 L13 M13 N13 N12 N11 N10	Digital core power. This is, V_{DD} = 1.8 V $\pm$ 5%, for the digital core logic.
VDDQ	Power Digital I/O	E9 E8 E7 E6 E5 F5 G5 H5 J5 K5 L5 M5 N5 N6 N7 N8 N9	Digital I/O power.
GND	Ground Digital	A1 A2 A3 A14 A17 B1 B2 B3 B14 B17 C1 C2 C3 C4 C14 C17 D1 D2 D3	Digital ground.

Pin Name	Type	Pin No.	Function
		D14 D17 E1 E2 E4 E14 E17 F1 F2 F4 F14 F17 G1 G2 G4 G14 G17 H1 H2 H4 H14 H17 J4 K4 K14 K17 L4 L14 L17 M4 M14 M17 N4 N14 N17 P14 P15 P16 P17 R14 R15 R16 R17 T14 T15 T16 T17 U14 U15 U16 U17	

Pin Name	Type	Pin No.	Function
T_GND	Ground Digital Thermal	F6 F7 F8 F9 F10 F11 F12 G6 G7 G8 G9 G10 G11 G12 H6 H7 H8 H9 H10 H11 H12 J6 J7 J8 J9 J10 J11 J12 K6 K7 K8 K9 K10 K11 K12 L6 L7 L8 L9 L10 L11 L12 M6 M7 M8 M9 M10 M11 M12	Thermal ground. Used as a ground pin and to conduct heat away from the part and into the PCB. This ground should be attached to the same ground plane as GND.

Table 9 Analog Power and Ground Pins

Pin Name	Type	Pin No.	Function
VDDA	Power Analog	J14 J15	Analog Power. This is, V_{DDA} = 1.8 V ± 5% and must be separated from digital power.
GNDA	Ground Analog	J16 J17	Analog ground. Connect to same ground plane as GND pins.

Notes:

1. All DualPHY 1G inputs and bi-directionals present minimum capacitive loading and operate at CMOS logic levels.
2. Digital and analog ground pins are not connected together internally. Failure to connect any of these pins can cause malfunction or damage to the DualPHY 1G device.
3. Digital and analog power pins are not connected together internally. Failure to connect any of these pins could also result in malfunction or damage to the DualPHY 1G device.

10 Functional Description

10.1 Modes of Operation

The DualPHY 1G device has four modes of operation:

- Locally Referenced Receive Clock (LRRC) Mode
- Remotely Referenced Receive Clock (RRRC) Mode
- Half-rate Receive Clock (HRRC) Mode
- Parallel Loopback Mode

LRRC and Parallel Loopback modes use the channel Receive FIFOs to synchronize the received data to the local clock domain (REFCLK). The LRRC Mode configures the Parallel Receive and Transmit Interface into two 10-bit Single Data Rate (SDR) Ports.

RRRC Mode bypasses the channel Receive FIFOs, which enables both channels to operate independently with their own recovered clock and data. RRRC Mode configures the Parallel Receive and Transmit Interface into two 10-bit Single Data Rate (SDR) Ports.

HRRC Mode also bypasses the channel Receive FIFOs, which enables both channels to operate independently with their own recovered clock and data. HRRC Mode configures the Parallel Receive Interface into two 10-bit Dual Data Rate (DDR) Ports, each having their own common and complimentary half rate receive clocks. The Transmit Interface is configured as two 10-bit Single Data Rate (SDR) Ports with full rate transmit clocks.

When the DualPHY 1G device is configured in LRRC or Parallel Loopback Mode, the Receive FIFO is enabled to synchronize the incoming serial data to the local clock domain determined by REFCLK. While operating in this mode, the DualPHY 1G device can be programmed to perform frequency compensation on a channel-by-channel basis.

When the DualPHY 1G device is configured in RRRC or HRRC Mode, the Receive FIFO is bypassed. In these modes, both channels operate independently with their own recovered clock and data on a dedicated set of terminals. Since this mode provides a recovered clock per channel, the frequency difference between REFCLK and recovered clock (receive data rate) is limited only by the capture range of the clock recovery circuit. The DualPHY 1G clock recovery circuit can tolerate frequency differences of ±200 ppm of the REFCLK frequency (with no packet size or IPG restriction). This mode provides the lowest possible latency since the internal Receive FIFOs are bypassed.

10.1.1 Locally Recovered Receive Clock (LRRC) Mode

LRRC Mode uses the Receive FIFOs to transfer data from the recovered clock domain to the local (REFCLK) clock domain on both channels. To activate this mode, the MODE pins must be set to logic 00. In this mode, the two channels of high-speed receive data coming into the DualPHY 1G device can be sourced from different clocks by the DualPHY 1G device's link partners. Figure 6 illustrates the receive data path for LRRC Mode. It shows the data path from one of the DualPHY 1G device's two high-speed serial input channels to one of its 10-bit parallel receive output port. The RBCB1 and RBCB0 are common across both parallel ports.

Figure 6 LRRC Mode Receive Data Path

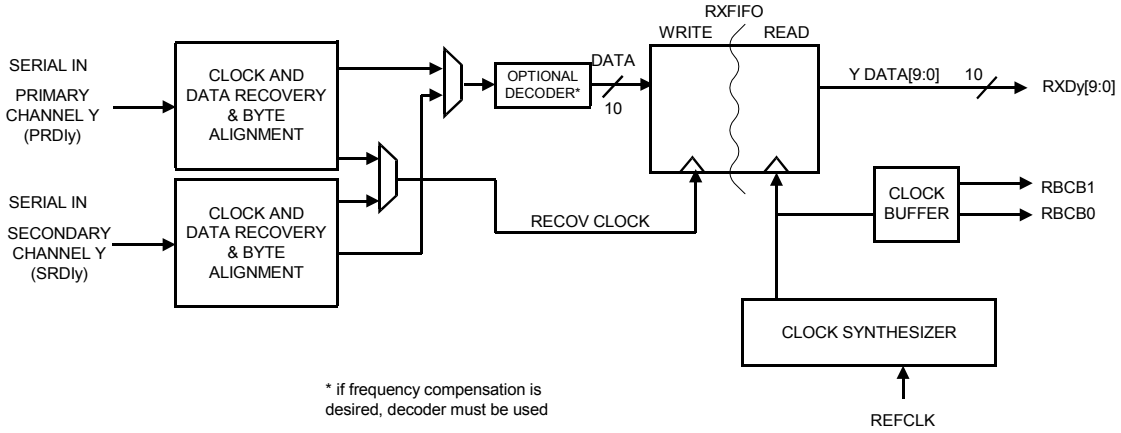


Table 10 defines the Mode Options for LRRC Mode. In **Mode Option 1**, the INS_DEL_DIS pin is set to a logic 0 which allows idle patterns to be inserted or deleted into the Receive FIFO to compensate for clock rate differences. DEC_ENC_EN is set to a logic 1 which enbles the internal 8B/10B encoder/decoder.

In **Mode Option 2**, the INS_DEL_DIS pin is set to a logic 1 which disables the inserts and deletes of idles in the Receive FIFO. This can be done in synchronous systems that guarantee that the clock that sourced the serial receive data is the same as the REFCLK.

In **Mode Option 3**, DEC_ENC_EN is set to a logic 0 and INS_DEL_DIS is set to a logic 1. This allows 10B data to be passed through the Receive FIFO to the parallel outputs, in a synchronous system.

In **Mode Option 4**, PCS_ENABLE is set to a logic 1, INS_DEL_DIS is set to a logic 0, and DEC_ENC_EN is set to a logic 1. This enables full duplex PCS functionality with frequency compensation.

Table 10 LRRC Mode Options

			RX interface			Pin Settings							
Mode Option	Parallel Interface	**LRRC Mode** (MODE[1:0] = 00) Channel data are sampled on the positive edge of RBCD1 and TXCK. One 10-bit data port supports a single channel.	FIFOs	RXCLK(s)	Frequency	MODE1	MODE0	DEC_ENC_EN	GEMOD	BMOD	PCS_ENABLE (Config Bit Only)	INS_DEL_DIS	ENPLPBK
1	**8B**	**With frequency compensation**											
		Receive RXDy[7:0] = 8-bit data RXDy[8] = K bit RXDy[9] = code violation bit Transmit TXDy[7:0] = 8-bit data TXDy[8] = K bit TXDy[9] = reserved	on	1	f_{REFCLK}	0	0	1	*	*	0	0	0
2	**8B**	**Without frequency compensation**											
		Same as option 1 except the Receive FIFO insert/delete function is disabled. The REFCLK signals of the remote transmit PHY and local receiving PHY must be synchronous.	on	1	f_{REFCLK}	0	0	1	*	*	0	1	0
3	**10B**	**Without frequency compensation**											
		Receive RXDy[9:0] = 10-bit block encoded data Transmit TXDy[9:0] = 10-bit block encoded data	on	1	f_{REFCLK}	0	0	0	0	0	0	1	0
4	**PCS**	**Full Duplex PCS with frequency compensation**											
		Receive RXDy[7:0] = 8-bit data RXDy[8] = RX_DV RXDy[9] = RX_ER Transmit TXDy[7:0] = 8 bit data TXDy[8] = TX_EN TXDy[9] = TX_ER	on	1	f_{REFCLK}	0	0	1	0	0	1	0	0

* Optional: Processing of Gigabit Ethernet data via GEMOD=1 (and optionally busy bit via BMOD=1), otherwise should be set to zero.

10.1.2 Remotely Referenced Receive Clock (RRRC) Mode

In RRRC Mode both channels operate independently with their own recovered clock and data. Since this mode does not use the Receive FIFOs, the frequency difference between REFCLK and recovered clock (receive data rate) is limited only by the capture range of the clock recovery circuit. Therefore, the DualPHY 1G device can tolerate frequency differences of ±200 ppm of the REFCLK frequency (with no packet size or IPG restriction). This mode provides the lowest possible latency since the internal Receive FIFOs are bypassed.

Figure 7 illustrates the receive data path for RRRC Mode. It documents the data path from one of the DualPHY 1G device's two high-speed serial input channels to one of its 10-bit SDR parallel receive output ports.

Figure 7 RRRC Mode Receive Data Path

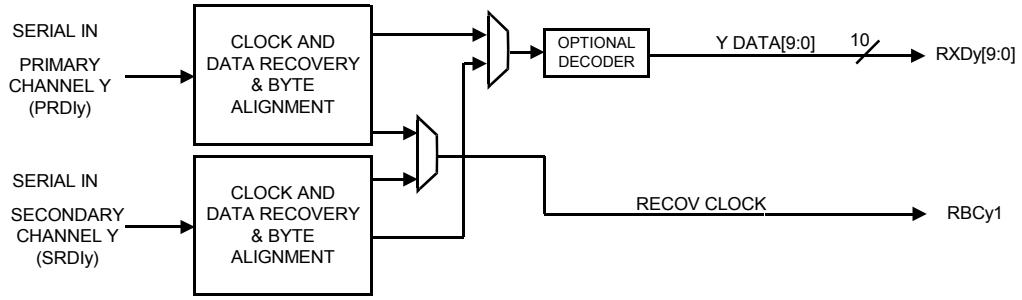


Table 11 defines the Mode Options for RRRC Mode. The INS_DEL_DIS is automatically disabled while in RRRC Mode. To activate this mode, the MODE pins must be set to logic 10.

In **Mode Option 1**, DEC_ENC_EN is set to a logic 1, which enbles the internal 8B/10B encoder/decoder.

In **Mode Option 2**, DEC_ENC_EN is set to a logic 0, which disables the internal 8B/10B encoder/decoder.

In **Mode Option 3**, PCS_ENABLE is set to a logic 1 and DEC_ENC_EN is set to a logic 1. This enables full duplex PCS functionality.

Table 11 RRRC Mode Options

			RX interface			Pin Settings							
Mode Option	Parallel Interface	**RRRC Mode** (MODE[1:0] = 10) Channel data are sampled on the rising edge of the byte clock, RBCY1. Each 10-bit data port supports a single channel.	FIFOs	RBC(s)	Frequency	MODE1	MODE0	DEC_ENC_EN	GEMOD	BMOD	PCS_ENABLE (Conf Bit only)	INS_DEL_DIS	ENPLPBK
1	**8B**	**8B/10B Encoder/Decoder Enabled**											
		Receive RXDy[7:0] = 8 bit data RXDy[8] = K bit RXDy[9] = code violation bit Transmit TXDy[7:0] = 8 bit data TXDy[8] = K bit TXDy[9] = reserved	off	4	$f_{recoveredclk}$	1	0	1	*	*	0	X	0
2	**10B**	**8B/10B Encoder/Decoder Disabled**											
		Receive RXDy[9:0] = 10-bit block encoded data Transmit TXDy[9:0] = 10-bit block encoded data	off	4	$f_{recoveredclk}$	1	0	0	0	0	0	X	0
3	**PCS**	**Full Duplex PCS**											
		Receive RXDy[7:0] = 8 bit data RXDy[8] = RX_DV RXDy[9] = RX_ER Transmit TXDy[7:0] = 8 bit data TXDy[8] = TX_EN TXDy[9] = TX_ER	off	4	$f_{recoveredclk}$	1	0	1	0	0	1	X	0

*Optional: Processing of Gigabit Ethernet data via GEMOD=1(and optionally Busy Bit via BMOD=1)
Otherwise should be set to 0

10.1.3 Half Rate Receive Clock (HRRC) Mode

The Half Rate Receive Clock (HRRC) Mode maps two channels of serial data to two ports. Each port consists of a 10-bit receive data output bus and a 10-bit transmit input data bus. A half-rate complementary receive clock pair (RBCB1/RBCB0, RBCA1/RBCA0) is used as a reference for each receive data port. The receive clocks are derived from the remote reference clock of each remote transmitter. A full-rate transmit clock for the two ports can be a single common clock (TXCKAB) or two individual transmit clocks (TXCKB, TXCKA).The transmit clock is input from a local source for each channel, TXCKB and TXCKA.

HRRC allows each channel to operate independently with its own recovered clock and data on a dedicated set of terminals. Frequency differences of ±200 ppm[1] of the REFCLK frequency can be tolerated.

Figure 8 illustrates the receive data path for HRRC Mode. It documents the data path from one of the DualPHY 1G device's two high-speed serial input channels to one of its 10-bit DDR parallel receive output ports.

The internal 8B/10B Encoder/Decoder and the PCS Logic must be disabled while operating in HRRC Mode. When PCS logic is disabled the PM8374A will not keep track of even and odd byte locations. If the interfacing logic is implementing the PCS functions, this logic will also have to keep track of even and odd byte locations as commas are expected to be sent in even byte locations. If PCS functionality is not part of the system the PM8374A does not impose any restrictions regarding byte positions.

Figure 8 Receive Data Path for HRRC Mode

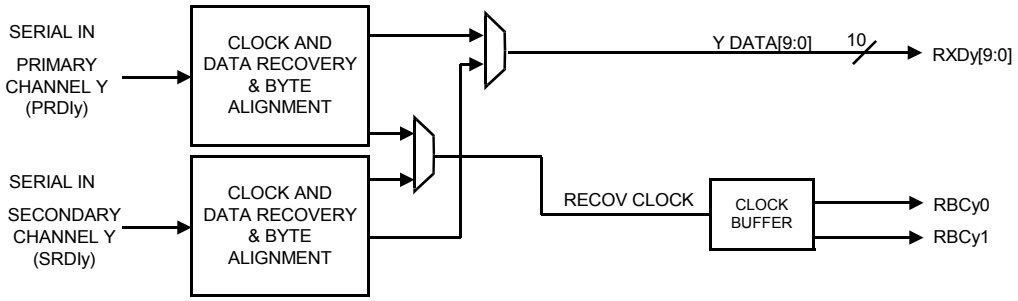


Table 12 defines the Mode Options for HRRC Mode. The INS_DEL_DIS is automatically disabled while in HRRC Mode. To activate this mode, the MODE pins must be set to logic 11. In **Mode Option 1**, DEC_ENC_EN is set to a logic 0, which disables the internal 8B/10B encoder/decoder.

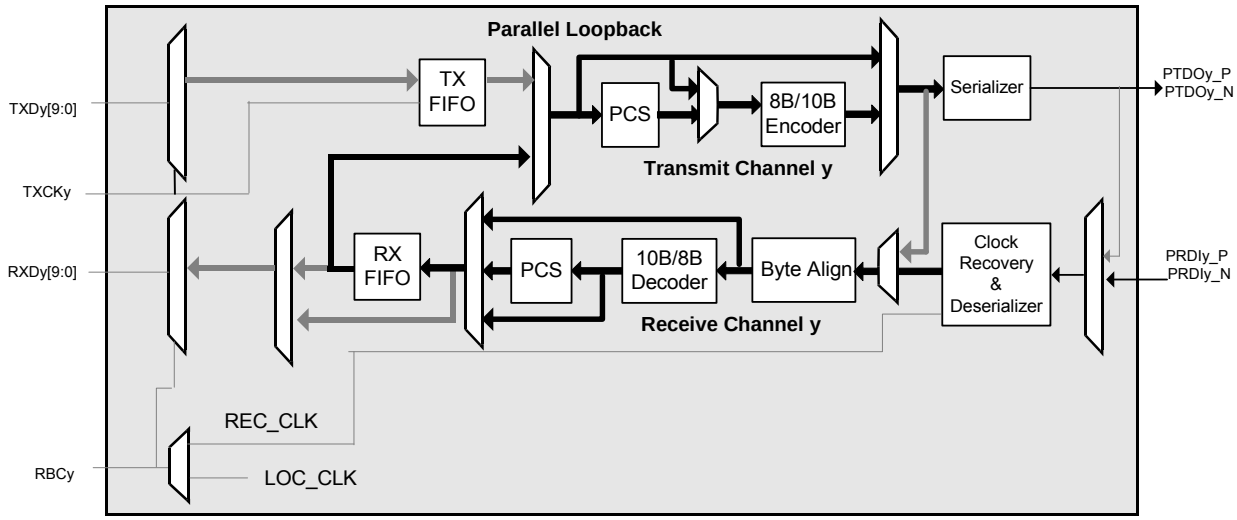
Table 12 HRRC Mode Options

			RX interface			Pin Settings							
Mode Option	Parallel Interface	**HRRC Mode** (MODE[1:0] = 11) Channel data are sampled on both edges of the half rate byte clock, RBCx1. (RBCx0 is the complementary clock) Each 10-bit data port supports a single channel.	FIFOs	RBC(s)	Frequency	MODE1	MODE0	DEC_ENC_EN	GEMOD	BMOD	PCS_ENABLE (Conf Bit only)	INS_DEL_DIS	ENPLPBK
1	**10B**	**8B/10B Encoder/Decoder Disabled**											
		Receive RXDy[9:0] = 10-bit block encoded data Transmit TXDy[9:0] = 10-bit block encoded data	off	8	$f_{recoveredclk}$	1	1	0	0	0	0	X	0

10.1.4 Parallel Loopback Mode

Parallel Loopback Mode provides a means to transmit a serial data stream on the high-speed transmit outputs (TDO) that has been received on the high-speed receive inputs (RDI), without external intervention. This is useful for retiming serial data streams or for diagnostic/test purposes. Figure 9 shows the data path for a channel that is configured in Parallel Loopback Mode.

Figure 9 Parallel Loopback Data Path



The DualPHY 1G device is configured into parallel loopback via the MDC/MDIO management registers. Any of the configurations described in the LRRC Mode section can also be configured to loop data internally from the parallel receive outputs to the parallel transmit outputs. Parallel Loopback requires that the Receive FIFO be enabled; therefore RRRC and HRRC Modes, which by-pass the Receive FIFO, are not supported when the DualPHY 1G device is configured in parallel loopback mode.

The Parallel Loopback Mode is enabled by setting the EN_PAR_LPBK_[B:A] bits to logic 1 in the Loopback Control Register. The parallel receive outputs will still be valid in Parallel Loopback Mode unless the POEN pin or the IPOEN bit is set to logic 0 in PMC Control 2 Register, because this will tri-state the parallel outputs. The parallel transmit input data is ignored in Parallel Loopback and the transmit FIFO is also bypassed. The 8B/10B encoders/decoders can be disabled if 10B symbol preservation is desired; however, the encoding/decoding will have to be done externally.

10.2 Channel Redundancy

The DualPHY 1G device supports two primary and secondary channel pairs. Channel pairing is fixed. Each receive channel pair is able to individually select its primary or secondary channel. Each transmit channel pair can be enabled individually or simultaneously to allow redundant data to be transmitted on both channels. The configuration for each channel is done via the MDC/MDIO interface. The selection bits are located in the Redundancy Control Register (Register 0x1D).

It is important to note that during internal serial data loopback testing, the channel loopback enable bits in the Loopback control register must be coordinated with the redundancy control register's channel-select bits so that transmit primary and secondary channels are paired with their receive channel counterparts.

10.3 Serial Channel Overview

The DualPHY 1G device uses high-speed serial channel technology to communicate data between chips. Each channel consists of a differential transmit pair and a differential receive pair. The device supports PECL voltage swings and the receiver inputs are designed to be capacitively-coupled external to the device. A clock is embedded in the serial data stream at the transmitter and extracted at the receiver, where it is used to recover the data. Data is de-serialized, decoded and processed internally as nine-bit bytes (8 data bits and 1 control bit) plus decode error indication.

The DualPHY 1G device requires that received data be 8B/10B encoded to ensure sufficient transition density. The DualPHY 1G device's internal 8B/10B encoder/decoder can be disabled if an external 8B/10B encoder/decoder is used. The 8B/10B coding method offers several advantages including high-transition density, low DC offset, and availability of special control characters (see Section 10.3.1).

10.3.1 8B Code Group Bit Mappings

All DualPHY 1G registers that contain 8B code groups adhere to the following convention:

- Bit0, the LSB – contains the A-bit of the code group
- Bit7, the MSB – contains the H-bit of the code group
- Bit8, contains the k-bit (if applicable)

Table 13 identifies the valid control code groups that will encode/decode properly. Do not specify any other control code groups in the DualPHY 1G registers or apply these code groups to the TXDy[8:0] interface.

Table 13 Valid K Bit Values

K-Bit	Valid 9-bit Value (hex)	Code	Definition
K28.0	0x11C	/R/[1]	Suggested Skip/Replace Idle Character
K28.1	0x13C		Alternate Skip/Replace Idle Character
K28.2	0x15C		Alternate Skip/Replace Idle Character
K28.3	0x17C	/A/	Suggested Alignment Idle Character
K28.4	0x19C		Alternate Skip/Replace Idle Character
K28.5	0x1BC	/K/	Synchronization Idle Character
K28.6	0x1DC		Alternate Skip/Replace Idle Character
K28.7	0x1FC		Special Diagnostics Character[2]
K23.7	0x1F7	/R/	Carrier-Extend for 1000BaseX PCS Apps
K27.7	0x1FB	/S/	Start-of-Packet
K29.7	0x1FD	/T/	End-of-Packet
K30.7	0x1FE	/V/	Error Propagation

Note:

1. Refer to Table 48-4 Defined ordered_sets and special code groups in the IEEE Draft P802.3-2000.
2. This character is not to be used as part of normal transmission data. Please see section 36.2.4.9 in IEEE 802.3 for further details.

For backplane applications, the usage of these characters is not limited by the DualPHY 1G device. Any characters not used as Alignment or Idle characters will be passed transparently between DualPHY 1G devices.

For Gigabit Ethernet applications, these characters must be used in a manner consistent with the 802.3 specification.

10.3.2 Clock Synthesizer

The Clock Synthesizer uses a PLL to synthesize a clock from the REFCLK input. The frequency of the PLL clock is 10 times the frequency of REFCLK, and a single synthesized clock is used to transmit serial data on both transmit channels.

The PLL clock frequency can be varied over a range of 1.0 GHz to 1.25 GHz by changing the frequency of REFCLK. The PLL has a fixed multiplication ratio of 10, so the frequency of REFCLK must be 1/10 the required PLL clock frequency as illustrated in Table 14.

The PLL in the Clock Synthesizer requires a 10 KΩ ± 1% precision resistor on the RPRES terminal.

Table 14 Example REFCLK and PLL Clock Combinations

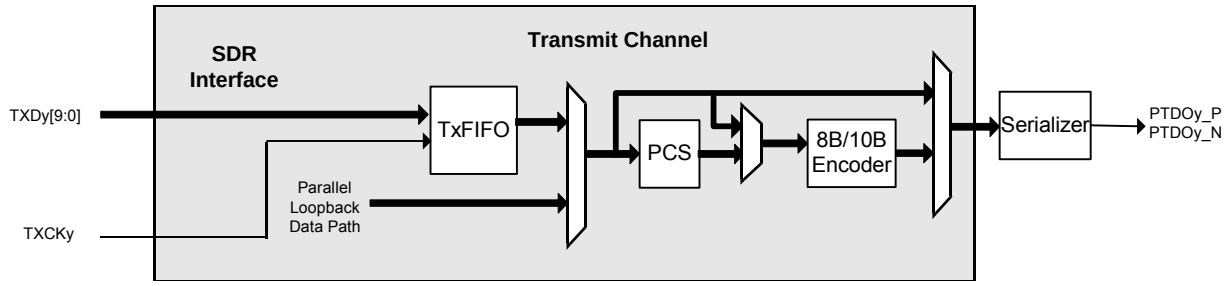
REFCLK Frequency	Multiplier	PLL Clock Frequency	Transmit Data Rate
93.3 MHz	10x	933MHz	933 Mbit/s
106.25 MHz	10X	1.0625 GHz	1.0625 Gbit/s
125 MHz	10X	1.25 GHz	1.25 Gbit/s

10.3.3 Transmit Path

The DualPHY 1G device contains two transmit channels. Each channel consists of a SDR Parallel Interface, Transmit FIFO, Transmit PCS, 8B/10B Encoder, and Serializer. The configuration of these functional blocks is shown in Figure 10.

The device can accept 8-bit plus control bit, GMII formatted data, or 10-bit coded data on the TXDy ports. The data must be frequency-synchronous with REFCLK. The 8B/10B encoder and PCS logic may be bypassed depending on the type of data presented.

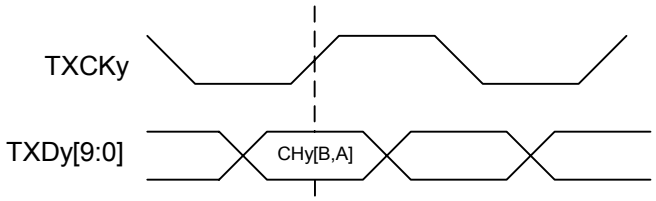
Figure 10 Transmit Channel Functional Blocks



SDR Parallel Interface

The transmit parallel interface consists of 20 data pins that are divided across the two transmit channels. Channels A and B each use ten pins. The pins are utilized by applying the input data in a Single-Data Rate (SDR) fashion; that is, data is applied on the rising edges of the transmit clock. The parallel transmit interface is employed as a SDR interface for all operational modes of the DualPHY 1G device. The transmit data for each channel is sampled on the rising edge of the corresponding transmit clock. This is depicted in Figure 11, where y refers to A or B.

Figure 11 Transmit Timing



The device may be configured so that each TXDy port has its own clock or so that both channels share a common clock. When the TXCLK4 bit is set to logic 0 in PMC Control 2 Register, both TXDy ports are sampled by a common clock, TXCKAB. When the TXCLK4 bit is set to logic 1, TXCKA samples TXDA, and TXCKB samples TXDB. Clocks TXCKA, TXCKB, and TXCKAB (if used) must all be synchronous to REFCLK, but the phase of each clock can be different. The Transmit FIFO will account for the phase differences (see the Transmit FIFO description for addition details).

The transmit data can be 10B encoded data if the encoder is disabled, 8B data plus K control bit if the encoder is enabled, or 8 bits of data (TXD) plus TX_EN and TX_ER for Gigabit Ethernet applications

Table 15 describes the mapping of data bits to the transmit data ports. When the encoder is disabled, the 10B word is mapped to a TBI (Ten-Bit Interface) and is generally described by “abcdeifghj” where “a” is the least significant bit and serialized onto the wire first, and “j” is the most significant bit.

When the encoder is enabled, the 8B word is represented by “HGFEDCBA” where “H” is the most significant bit, “A” is the least significant bit, and the control value is “K”. When the PCS logic is enabled, the transmit data is mapped to GMII signals. When the encoder is enabled, the transmit data is 10B-encoded internally and is generally described by “abcdeifghj” where “a” is the least significant bit and serialized onto the wire first and “j” is the most significant bit.

Table 15 Parallel Transmit Interface Pin Mapping

	10B Transmit Data	8B Transmit Data	GMII DATA
TXDy9	j	TIE LOW	TX_ER
TXDy8	h	K	TX_EN
TXDy7	g	H	TXD7
TXDy6	f	G	TXD6
TXDy5	i	F	TXD5
TXDy4	e	E	TXD4
TXDy3	d	D	TXD3
TXDy2	c	C	TXD2
TXDy1	b	B	TXD1
TXDy0	a	A	TXD0

Transmit FIFO

The Transmit FIFO is a six-word by 10-bit FIFO that transfers data from the TXCKy domain to the internal clock domain that is synchronous to REFCLK. The TXCKy and the REFCLK must be synchronous. Once an arbitrary phase relationship is established, the phase deviation must not vary by more than ±500ps. Should the phase change by more than ±500 ps, momentary corruption of data may occur.

Transmit PCS

The DualPHY 1G device supports the 1000Base-X PCS for full-duplex applications. Note that carrier sense (CRS) and collision detect (COL) are not supported per *IEEE 802.3-2000* standard. The PCS functionality is enabled by setting the PCS_ENABLE bit to logic 1 in PMC Control 2 Register and the INT_DEC_ENC_ENABLE bit in PMC Control 2 Register or the DEC_ENC_EN pin to logic 1.

The PCS transmit logic contains an 8B/10B encoder and a single transmit state machine whose operation is consistent with the operation of the two transmit state machines that run in unison within clause 36 of IEEE *802.3-2000*. All transmit blocks are compliant with the *IEEE 802.3-2000* (Clauses 36 and 37).

8B/10B Encoder

When enabled, the encoder accepts an 8-bit word plus the k-bit and encodes these bits into a 10-bit parallel code. The encoder generates a running disparity for its own use in generating sub-blocks of 6- and 4-bit codes. These sub-blocks limit the run length and maintain DC balance of the serialized bits. The user can present data as an un-encoded byte along with a control signal indicating a "K" character, or can disable the encoding logic and present pre-encoded 10-bit data. The Encoder logic is enabled either by connecting the DEC_ENC_EN pin to logic 1 or programming PMC Control 2 Register, bit 7 (INT_DEC_ENC_ENABLE) with logic value 1. Rules for encoding are specified in IEEE *802.3-2000*.

When the encoder is enabled and input pin GEMOD or PMC Control 3 Register, bit 15 (GE_REG) is set to logic 1 and PMC Control 2 Register, bit 2 (PCS_ENABLE) is set to logic 0, the encoder will substitute a D5.6 octet for a D16.2 octet when it follows a K28.5 character and the current running disparity is negative. This functionality is useful when the input data stream is generated from a 1000Base-X PCS Transmit state machine and the current running disparity during Interpacket Gap (IPG) must be maintained such that positive commas are encoded.

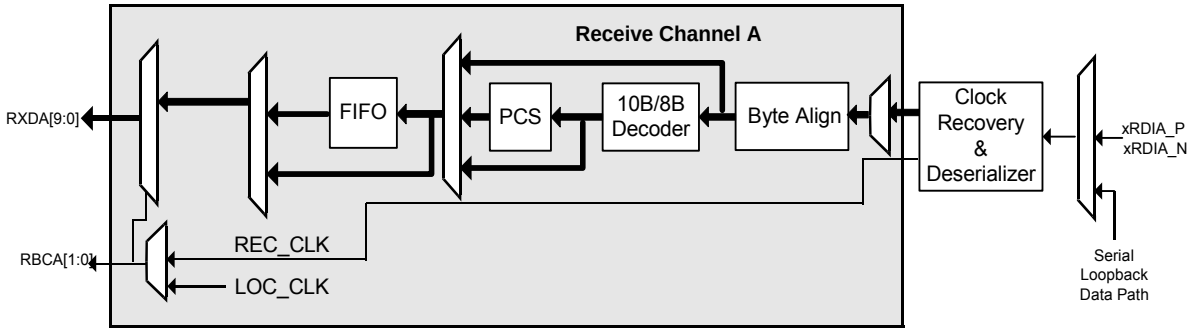
Serializer

The serializer accepts 10-bit transmission characters and converts them from a parallel format to a serial bit stream at bit rates between 933 Mbit/s and 1.25 Gbit/s. The serializer accepts a 10-bit parallel word with the least significant bit being transmitted first.

10.3.4 Receive Path

The DualPHY 1G device contains two receive channels. Each channel consists of a Clock and Data Recovery Unit (CDRU), Byte Alignment logic, 8/B/10B Decoder, Receive PCS, Receive FIFO, and a SDR/DDR Parallel Output Interface. The configuration of these functional blocks is shown in Figure 12.

Figure 12 Receive Channel Functional Blocks



Each channel's CDRU, comma detection, and byte alignment logic run independently. The comma detection logic is programmable to detect +comma, -comma, or both. The decoded words with K bits are optionally retimed by the Receive FIFO, with IDLE character insertion/deletion for frequency compensation.

The receiver input data must be AC-coupled and must have a transfer rate of between 933 Mbits/s and 1.25 Gbit/s. The DualPHY 1G device supports on-chip 100 Ω differential termination. The data is expected to be a 10-bit encoded data stream as specified in *IEEE 802.3-2000*. The clock recovery circuit recovers a clock (REC_CLK) from the incoming data. The recovered clock is used to sample the data. Both the recovered clock and data are provided to the deserializer independently for each channel.

Serial input ports may be internally looped-back to the serial output ports for testing purposes. While in a serial loopback mode, the serial output pins are held at a differential one. Serial loopback may be enabled using one of the following mechanisms:

- Assert INT_EN_PRI_SERIAL_LPBK/INT_EN_SEC_SERIAL_LPBK control bit in the Loopback Control Register
- Assert Loopback bit in the channel's GMII Control register
- Assert EN_SLPBK pin to loopback both channels simultaneously

When the CODE_VIOL_DIS_ENABLE bit (bit 14, PMC Control 2 register) is set or the CV_DIS_EN pin is asserted, a code or disparity violation detected by the receiver will replace the byte in violation by the encoding of all-1's or 0xFF on the data pins and a 1 on the K bit. The associated code error counter is incremented. The error code is propagated through DualPHY 1G device and eventually transmitted at the egress.

Clock and Data Recovery

A receive clock is extracted from the 10-bit coded serial data stream independently on each channel. The extracted clock frequency is between 933 Mbit/s and 1.25 Gbit/s. The data rate of the received serial bit stream should also be between 933 Mbit/s and 1.25 Gbit/s to guarantee proper lock. The receive clock locks to the input within 2 µS after a valid input data stream is applied. The recovered clock will be synchronous to the REFCLK if no data is present on the RDI serial inputs.

The bit synchronization time is the time required for the Clock and Data Recovery unit to recover the incoming bitstream error-free. This time is influenced by several factors, including:

- Receive jitter.
- Relative phase difference between the incoming bitstream and the signal to which the CDRU was previously synchronized.
- Transition density.
- DC Common Mode voltage offsets

The bit synchronization time is independent of the ppm offset. However, the incoming bitstream must be within +/-200 ppm of the local REFCLK.

The CDR unit requires the maximum bit synchronization time when the receiver eye opening is at the minimum permissible opening, and the relative phase alignment between the bitstream and the CDR is the worst case. Under these conditions, the maximum bit synchronization time is determined by the transition density of the incoming bit stream.

An 8B/10B-coded bitstream that contains the idle ordered set of K28.5, D16.2 will provide a nominal transition density of approximately 60%, and will result in a maximum bit synchronization time of 500 bit times. With other transition densities, the bit synchronization time can be calculated as:

> **T_BitSync** (in bit times) = 24000 / (nominal transition density expressed as a percentage)

This determination of bit sync time is only applicable when the CDRU inputs are switched from one transitioning bitstream to another. Should the inputs remain inactive for several thousands of bit times, bit synchronization will be delayed while the external AC coupling capacitors at the input of the SERDES charge to their steady state values. In this case, the maximum bit synchronization time is 2000 bit times.

The de-serializer converts the received serial stream into 10-bit parallel data, and the de-serialized data is then byte-aligned.

Byte Alignment and Synchronization

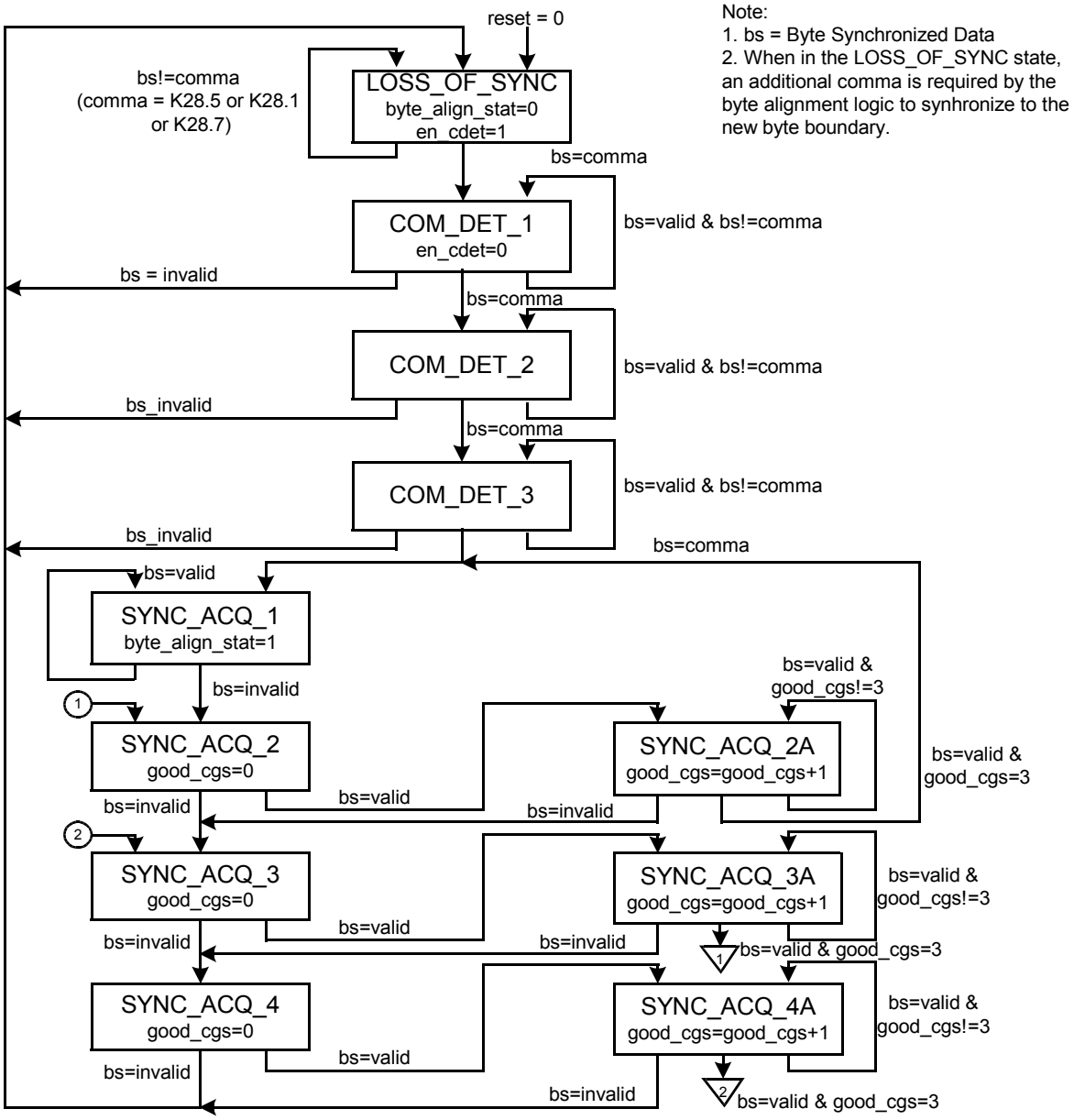
The character alignment logic searches the coded incoming serial stream for a sequence defined in *IEEE 802.3-2000* as a comma. A comma is the sequence 0b0011111, or its complement, and is unique in valid 10B-coded data. This makes the comma useful for detecting proper alignment of incoming characters to byte boundaries. Upon detection of a comma, the alignment logic shifts the incoming data to align the received data properly in the 10-bit character field. An optional Byte-Sync State machine, shown in Figure 13, is implemented on a per-channel basis to enable character alignment and preserve the alignment through occasional bit errors.

If a channel's Byte Synchronization State Machine is in the LOSS_OF_SYNC state, it can acquire synchronization by detecting four code-groups that contain commas without detecting code-group errors. An initial comma must be detected by the character alignment logic before the state machine can start the synchronization process. Once synchronization is acquired, the channel moves into the SYNC_ACQ_1 state. The state machine tests the received code-group to move between the SYNC_ACQ_1 and LOSS_OF_SYNC states. To prevent loss of synchronization during occasional bit errors, hysteresis can be added by setting the BA_HYST_EN bit in PMC Control 3 Register. The Byte Sync State Machine operates independently from the PCS Synchronization State Machine described in PCS Receive Section.

Hysteresis is normally disabled upon reset. In this case, once the channel's synchronization state machine has entered the SYNC_ACQ_1 state, any realignment caused by the detection of a comma in a new location causes the channel to move to the LOSS_OF_SYNC state. If hysteresis is enabled, the synchronization process uses the hysteresis defined in the synchronization state machine. Even if a channel's hysteresis is disabled, the synchronization state machine continues to monitor alignment and supply a synchronization status indication. If a channel's synchronization state machine enters the LOSS_OF_SYNC state, the corresponding BYTE_ALIGN_STAT_[B:A] bit in Auto-Negotiation Status Register 2 latches the status and holds it until a read of that register is preformed.

The serial bit stream must be ordered 'abcdeifghj' with 'a' being the first bit received and 'j' the last bit received. The recovered receive clocks are neither stretched nor slivered during character alignment. During alignment, up to four 10-bit code groups may be deleted or modified while aligning the code group to the edges of the receive clock. No more than four code groups will be deleted or modified.

Figure 13 Byte Synchronization State Machine



8B/10B Decoder

When enabled, each receive channel decodes incoming data into an 8-bit data byte and an associated control bit called the k-bit. Information is routed and processed internally in this 9-bit parallel form. The decoder monitors for proper disparity and coding logging errors. A 10^{th} bit for indicating a code violation or disparity error is also routed with the 9-bit parallel data. When the CODE_VIOL_DIS_ENABLE bit (bit 14, PMC Control 2) or the CV_DIS_EN pin is set, errors are reinforced by the receiver by substituting the code 0x3FF for the errored byte.

When the EN_CODE_ERR_CHK bit is set to logic 1 in Register 0x1B, the 8B/10B decoder in the corresponding channel will count coding errors received. When the error count reaches the maximum set by PKT_CNT[14:0] in Register 0x1C, the decoder will flag the condition by setting the CODE_ERR_EXCEED bit to logic 1 in Register 0x1B.

The 8B/10B coding error counters in all channels will be cleared whenever the CODE_ERR_STB bit is set to logic 1 in Register 0x24. CODE_ERR_STB is self-clearing.

Receive PCS

The DualPHY 1G device supports the 1000Base-X PCS for full-duplex applications. Note that carrier sense (CRS) and collision detect (COL) are not supported per *IEEE 802.3-2000* standard. The PCS functionality is enabled by setting the PCS_ENABLE bit and the INT_DEC_ENC_ENABLE bit in Register 0x11.

The PCS receive logic contains an 8B/10B decoder, synchronization state machine, receive state machine, and auto-negotiation (AN) state machine. All receive blocks are compliant with the *IEEE 802.3-2000* (Clauses 36 and 37). The AN state machine supports both base page and next page exchange and has programmable link timers. The link timer value can be programmed via LINK_TIMER_MODE bits [1:0] of Register 0x11. The link timers can be set to approximately 12.6 ms or 16.8 ms. To be compliant with the *IEEE 802.3-2000*, the default is 16.8 ms.

The management interface provides AN registers as prescribed by IEEE 802.3-2000. Additionally, two status registers, Register 0x19 (Auto Negotiation Status 1) and Register 0x1A (Auto Negotiation Status 2), have been added for polling the two separate ports with a single management register read.

Register 0x19 contains a base page received and a next page received indication for each port. These bits clear on read. Normally during AN, a channel's base page received bit will be set once, and then the next page received bit for that channel would be set for any subsequent pages received. If the base page received bit becomes set again during AN, it is an indication that AN has been restarted for that port.

Register 0x1A contains an indication for each channel that AN has completed. Both of the status registers reflect the same information found in Register 0x01 (Status), bit 5 and Register 0x06 (AN Expansion), bit 1. Reading Register 0x19 only clears that register; it does not clear the page received bits in Register 0x06. Similarly, when reading Register 0x06, Register 0x19 is not cleared.

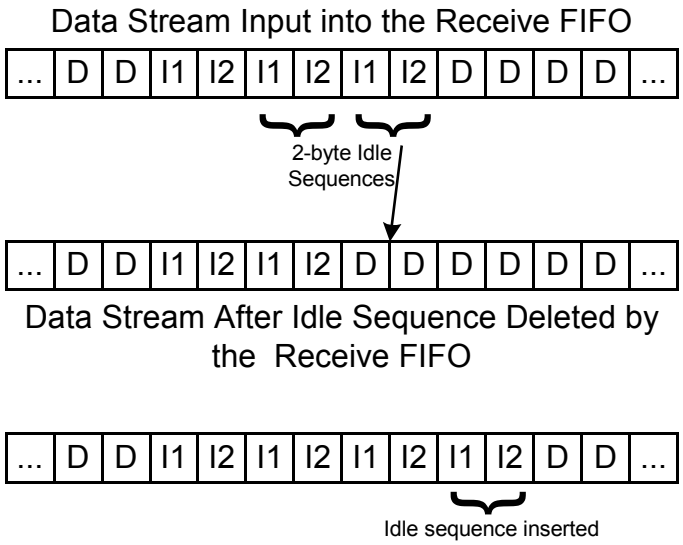
Additional information on PCS and GMII can be found in *IEEE* 802.3 sections 35 and 36.

Receive FIFO

The Receive FIFO transfers data from the recovered clock domain to the internal clock domain that is synchronous to REFCLK. The Receive FIFO compensates for differences in the clock tolerances. The Receive FIFO is used in the LRRC and Parallel Loopback Mode; it is not used in RRRC and HRRC Mode.

The Receive FIFO achieves clock tolerance compensation by inserting or deleting two-octet wide IDLE sequences as needed. Figure 14 illustrates the insertion (or deletion) of an IDLE sequence when the recovered clock is running slower (or faster) than the REFCLK. The Receive FIFO will only delete an IDLE sequence when more than one IDLE sequence has been recognized. When the Receive FIFO inserts an IDLE sequence, the IDLE sequence inserted is the same as the previous IDLE sequence received.

Figure 14 Insertion/Deletion of Idle Sequences by the Receive FIFO



The IDLE sequences are defined by registers 0x12 through 0x15. These registers are only used by the Receive FIFO and will not affect the de-serialization process. These registers are formatted as K-bit (bit 8) and data (bits 7:0). Generally, IDLE1 and IDLE1A should be programmed to one of the three valid control characters (K28.1, K28.5, or K28.7) that contain a comma pattern. The decoder must be enabled for the Receive FIFO to use these register values in the clock tolerance compensation logic.

The alternate IDLE sequence registers, IDLE1A and IDLE2A, are available for applications that make use of multiple idle sequences to indicate system conditions. An example of this would be flow control. One IDLE sequence might indicate “clear to send” while the other sequence indicates “not clear to send.” If only one IDLE sequence is desired, the two pairs of control registers should be programmed to the same value.

The DualPHY 1G device uses the values stored in the IDLE sequence registers to insert or delete idles in the Receive FIFO. Data can be presented to the DualPHY 1G device with either an IDLE1 or IDLE1A that is not followed by an IDLE2 or IDLE2A. In this condition, the data that follows the IDLE1 or IDLE1A must not be the same as the data stored in the IDLE2 or IDLE2A registers. If the data is the same, the DualPHY 1G device decodes the data pattern that follows the IDLE1 or IDLE1A as a valid IDLE2 or IDLE2A character and could delete it.

The insertion and deletion of IDLE sequences for clock tolerance compensation can be disabled by setting the INS_DEL_DIS bit in PMC Control 3 Register to logic 1.

Even if the incoming data stream does not contain IDLE sequences, the Receive FIFO can still transfer data from the recovered clock domain to the REFCLK domain and compensate for phase only.

The depth of the Receive FIFO determines the difference in clock frequency that the DualPHY 1G device can tolerate. The DualPHY 1G device has a sixteen-character-deep FIFO on each receive channel. Packet sizes of 20 Kbytes can be accommodated in systems with clock tolerances of ±100 ppm and appropriate IPG (8 bytes) when the Rx FIFO is enabled (LRRC or Parallel loopback mode).

Maximum Size Packets Supported

Internal logic within the device establishes a relationship between the frequency at which serial data is received (f_{DATA}), and 10x the reference clock frequency (f_{REFCLK}) provided by the local clock. This relationship allows the device to recover incoming serial data and place it on the REFCLK domain for further processing. The difference in these two frequencies is usually stated in parts per million (ppm) and is calculated as follows:

$$c_{ppm} = 10^6 \cdot \left| (10 \cdot f_{REFCLK} - f_{DATA}) / (10 \cdot f_{REFCLK}) \right| \quad (1)$$

The maximum allowable frequency offset between the incoming data and the local REFCLK is 200 ppm regardless of which operating mode is being used.

When operating in RRRC or HRRC mode there is no maximum packet size. The Receive FIFO is bypassed in this mode and each channel operates on its own independent recovered clock domain.

When operating in LRRC or parallel loopback mode, a maximum packet size is established due to the finite size of the Receive FIFO. The recovered data is sent through the Receive FIFO where all channels are placed on a common clock domain defined by the REFCLK frequency. The maximum packet size (in bytes) supported in this mode can be calculated by the following formula:

$$S_{max} = (10^6 \cdot 5) / c_{ppm} \quad (2)$$

The Receive FIFO performs frequency compensation by inserting or deleting IDLE pairs. Each IDLE pair consists of a two-byte sequence that is defined in the IDLE1/IDLE2 and IDLE1A/IDLE2A registers. The number of IDLE pairs required in each IPG is dependant upon S_{max} (the maximum packet size used in the system) and C_{ppm}. The number of required IDLE pairs (REQIDLPRS) can be calculated by using the following formula:

$$REQIDLPRS = int [S_{max} \cdot (2 \cdot C_{ppm} / 10^6)] \quad (3)$$

10.3.5 Gigabit Ethernet and PCS Operating Modes

The PCS_ENABLE bit (bit 2 in Register 0x11) is used to enable the 1000Base-X PCS logic. The GEMOD pin or the GE_REG register bit is used to enable a small subset of "PCS-type" functions. The description below specifies exact functions which GEMOD/GE_REG effects.

Note that PCS_ENABLE should not be set to logic 1 when either GEMOD or GE_REG register is set to logic 1.

Gigabit Ethernet with PCS Enabled

When the PCS logic is enabled the parallel interface is formatted as GMII data. The PCS logic includes TX and RX state machines, auto-negotiation, and byte alignment logic that are fully compliant with the IEEE 802.3 1000Base-X PCS specification.

Gigabit Ethernet with PCS Disabled - GEMOD Enabled and BMOD Disabled

When the GEMOD pin or GE_REG bit in the PMC Control 3 Register is set to logic 1, the parallel interface is formatted as 8B data. The receive FIFO recognizes a decoded /K28.5/ pattern followed by any valid data pattern, /Dx.y/, excluding the /D21.5/ and /D2.2/ data patterns, as an IDLE sequence that can be used for insertion or deletion in clock tolerance compensation. A decoded /K28.5/ pattern followed by the /D21.5/ or /D2.2/ data patterns and then followed by two valid data bytes are recognized as a four-byte configuration pattern as sent during auto-negotiation. These four-byte configuration patterns can be inserted or deleted for clock tolerance compensation.

Also, in this mode of operation IDLE patterns are corrected to ensure negative running disparity during the IPG by substituting /D5.6/ for /D16.2/ in a /K28.5/Dx.y/ transmit IDLE pair.

Note that Auto-Negotiation functions are NOT performed when GEMOD=1.

Gigabit Ethernet with PCS Disabled - GEMOD Enabled and BMOD Enabled

This mode operates the same as described above for Gigabit Ethernet with PCS Disabled - GEMOD enabled and BMOD disabled. For this mode, when the BMOD pin or the BUSY_REG bit in the PMC Control 3 Register is set to logic 1, a decoded /K28.5/ pattern followed by a /D10.1/ data byte will not be recognized as an IDLE sequence and will not be inserted or deleted.

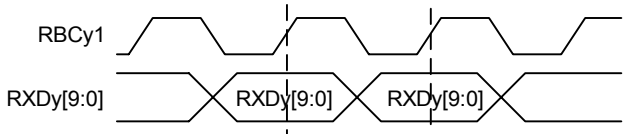
10.3.6 SDR/DDR Parallel Outputs

The parallel receive interface consists of 20 pins that are divided across two channels. Channels A and B use 10 pins each. Depending on the mode of operation, the pins are configured to operate in either as Single-Data Rate (SDR), that is, data is output on the rising edge of the receive clock; or as Dual-Data Rate (DDR), in which case data is output on both the rising and falling edge of the receive clock.

In RRRC Mode, the parallel receive pins are configured in SDR mode. The receive clocks are derived from the remote reference clock of each remote transmitter. A full rate receive clock (, RBCB1, RBCA1) is used as a reference for each receive data bus. Receive data for channels A and B is sampled on the rising edge of RBCy1; see Figure 15.

This mode allows each channel to operate independently with its own recovered clock and data on a dedicated set of terminals. Frequency differences of ±200 ppm[2] of the REFCLK frequency can be tolerated.

Figure 15 Receive Timing for RRRC Mode

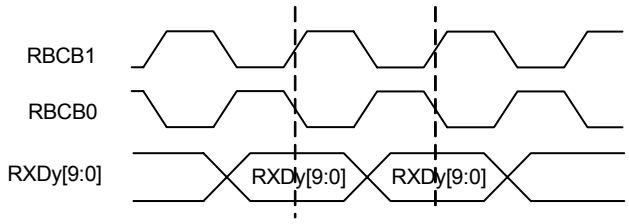


Note:

1. There is no complementary clock (RBCy0) provided in this mode.

In LRRCMode, the parallel receive pins are configured in SDR mode. Receive data for channels A and B are sampled on the rising edge of RBCB1 (falling edge of RBCB0); see Figure 16. This common complementary receive clock (RBCB1, RBCB0) is used as a reference for received data on both ports.

Figure 16 Receive Timing for LRRC Mode



[2] There is no restriction on IPG or packet size in this mode.

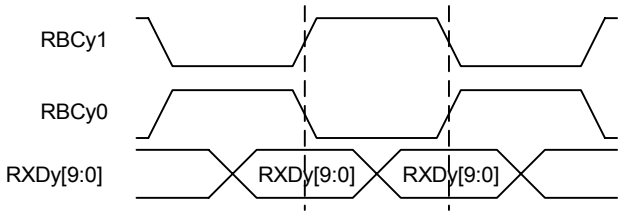
The frequency of the receive data for each channel must be within ±200 ppm[3] of the REFCLK. The receive FIFO on each channel transfers the data from the recovered clock domain to the local clock domain. Idle sequences (two-byte pairs)[4] are inserted or deleted as needed to compensate for the frequency difference between recovered and local clocks.

If the frequency of the recovered clock is the same as the local clock (i.e., a synchronous system), the insert/delete function of the receive FIFO can be disabled. In this case both the local receiver and the remote transmitter must use a common clock reference. This is useful when idle insertion and deletion is undesirable.

In HRRC Mode, the parallel receive pins are configured in DDR mode. The receive clocks are derived from the remote reference clock of each remote transmitter. A half-rate complementary receive clock pair (RBCB1/RBCB0, RBCA1/RBCA0) is used as a reference for each receive data port. Receive data for channels A and B is sampled on both edges of RBCy1/RBCy0; see Figure 17.

This mode allows each channel to operate independently with its own recovered clock and data on a dedicated set of terminals. Frequency differences of ±200 ppm[5] of the REFCLK frequency can be tolerated.

Figure 17 Receive Timing for HRRC Mode



The receive data can be 10B-encoded data when the decoder is disabled, 8B data plus K-bit control and code violation/disparity error indication bits when the decoder is enabled, or 8 bits of data (RXD) plus RX_DV and RX_ER (GMII data).

Table 16 describes the mapping of data bits to the receive data ports. When the decoder is disabled, the 10B word is mapped to a TBI (Ten-Bit Interface) and is generally described by "abcdeifghj" where "a" is the least significant bit and deserialized from the wire first; "j" is the most significant bit. When the decoder is enabled, the 8B word is represented by "HGFEDCBA" where "H" is the most significant bit, "A" is the least significant bit, the control value is "K", and the code violation/disparity error is "CV". When the PCS logic is enabled, the receive data is mapped to GMII signals.

[3] See the section "Maximum Packet Sizes Supported" for more detail on frequency offsets, packet sizes and IPG requirements for LRRC mode.
[4] An IDLE sequence is defined as either of the following combinations: IDLE1/IDLE2 or IDLE1A/IDLE2A. These values can be programmed in registers 18-21.
[5] There is no restriction on IPG or packet size in this mode.

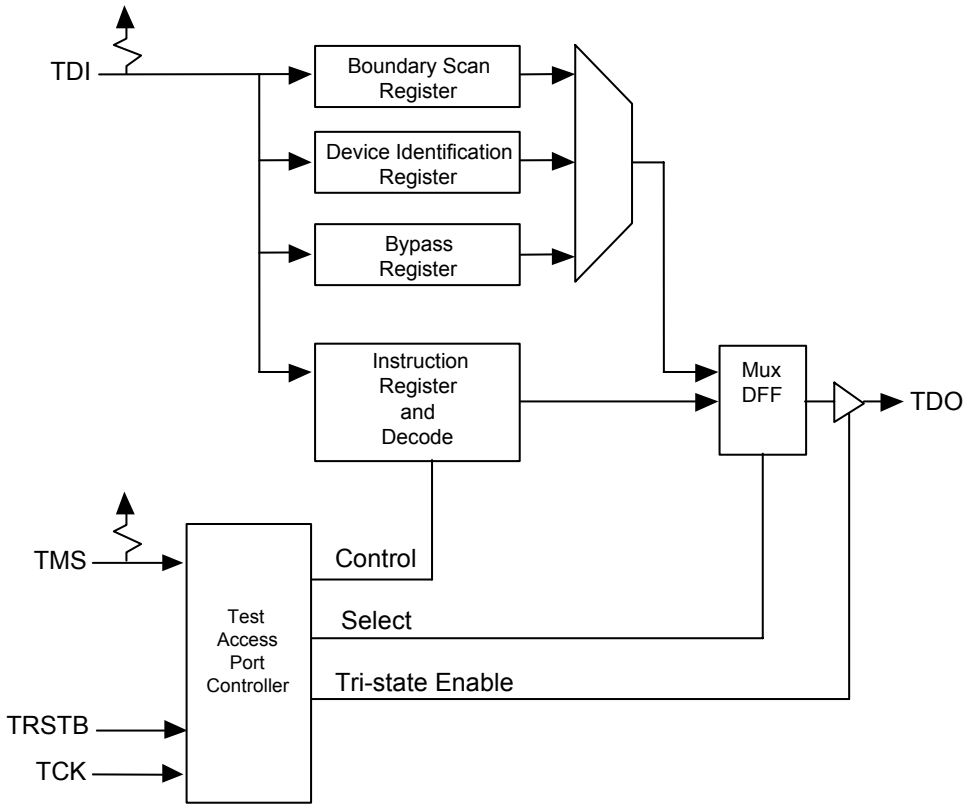
Table 16 Parallel Receive Interface Pin Mapping

	10B Receive Data	8B Receive Data	GMII DATA
RXDy9	J	CV	RX_ER
RXDy8	H	K	RX_DV
RXDy7	G	H	RXD7
RXDy6	F	G	RXD6
RXDy5	I	F	RXD5
RXDy4	E	E	RXD4
RXDy3	D	D	RXD3
RXDy2	C	C	RXD2
RXDy1	B	B	RXD1
RXDy0	A	A	RXD0

10.4 JTAG Test Access Port

The DualPHY 1G device supports the IEEE Boundary Scan Specification as described in the IEEE 1149.1 standards. The JTAG Test Access Port (TAP) consists of the five standard pins, TRSTB, TCK, TMS, TDI and TDO used to control the TAP controller and the boundary scan registers. The TRSTB input is the active-low reset signal used to reset the TAP controller. TCK is the test clock used to sample data on input, TDI and to output data on output, TDO. The TMS input is used to direct the TAP controller through its states. The basic boundary scan architecture is shown below.

Figure 18 Boundary Scan Architecture



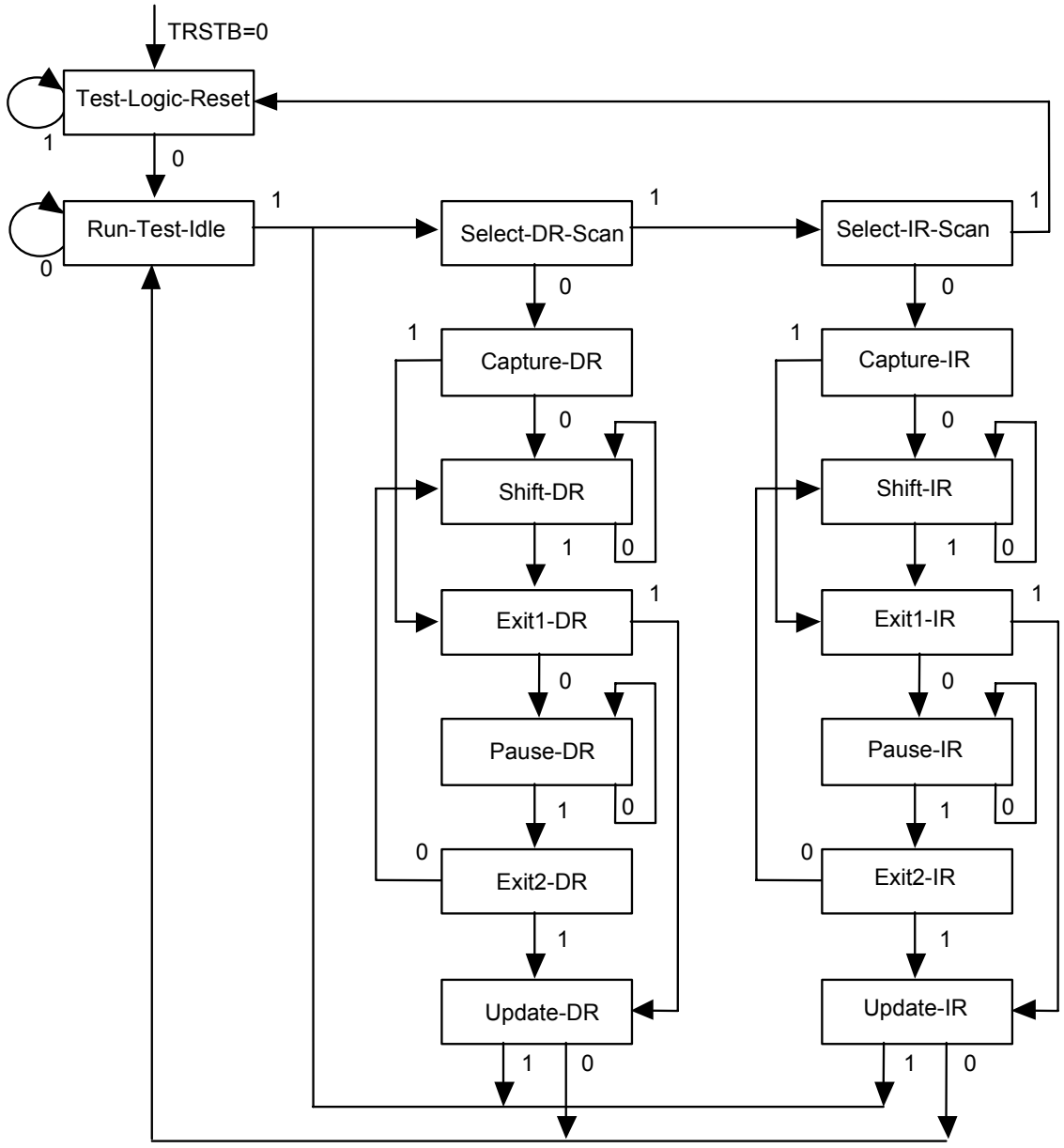
The boundary scan architecture consists of a TAP controller, an instruction register with instruction decode, a bypass register, a device identification register, and a boundary scan register. The TAP controller interprets the TMS input and generates control signals to load the instruction and data registers. The instruction register with instruction decode block is used to select the test to be executed and/or the register to be accessed. The bypass register offers a single-bit delay from primary input, TDI to primary output, TDO. The device identification register contains the device identification code.

The boundary scan register allows testing of board inter-connectivity. The boundary scan register consists of a shift register place in series with device inputs and outputs. Using the boundary scan register, all digital inputs can be sampled and shifted out on primary output, TDO. In addition, patterns can be shifted in on primary input, TDI and forced onto all digital outputs.

10.4.1 TAP Controller

The TAP controller is a synchronous finite state machine clocked by the rising edge of primary input, TCK. All state transitions are controlled using primary input, TMS. The finite state machine is shown in Figure 19.

Figure 19 TAP Controller Finite State Machine



Note:

1. TRSTB must be set to logic 1 in order to transition out of the Test-Logic-Reset State.
2. The values shown adjacent to each state transition in Figure 19 represents the signal present at TMS at the rising edge of TCK.
3. All transitions are dependent on the logic level of TMS.

Test-Logic-Reset

The test logic reset state is used to disable the TAP logic when the device is in normal mode operation. The state is entered asynchronously by asserting input, TRSTB. The state is entered synchronously regardless of the current TAP controller state by forcing input, TMS high for 5 TCK clock cycles. While in this state, the instruction register is set to the IDCODE instruction.

Run-Test-Idle

The run test/idle state is used to execute tests.

Capture-DR

The capture data register state is used to load parallel data into the test data registers selected by the current instruction. If the selected register does not allow parallel loads or no loading is required by the current instruction, the test register maintains its value. Loading occurs on the rising edge of TCK.

Shift-DR

The shift data register state is used to shift the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-DR

The update data register state is used to load a test register's parallel output latch. In general, the output latches are used to control the device. For example, for the EXTEST instruction, the boundary scan test register's parallel output latches are used to control the device's outputs. The parallel output latches are updated on the falling edge of TCK.

Capture-IR

The capture instruction register state is used to load the instruction register with a fixed instruction. The load occurs on the rising edge of TCK.

Shift-IR

The shift instruction register state is used to shift both the instruction register and the selected test data registers by one stage. Shifting is from MSB to LSB and occurs on the rising edge of TCK.

Update-IR

The update instruction register state is used to load a new instruction into the instruction register. The new instruction must be scanned in using the Shift-IR state. The load occurs on the falling edge of TCK.

The Pause-DR and Pause-IR states are provided to allow shifting through the test data and/or instruction registers to be momentarily paused.

10.4.2 Boundary Scan Instructions

The following is an description of the standard instructions. Each instruction selects a serial test data register path between input, TDI and output, TDO.

BYPASS

The bypass instruction shifts data from input, TDI to output, TDO with one TCK clock period delay. The instruction is used to bypass the device.

EXTEST

The external test instruction allows testing of the interconnection to other devices. When the current instruction is the EXTEST instruction, the boundary scan register is placed between input, TDI and output, TDO. Primary device inputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state. Primary device outputs can be controlled by loading patterns shifted in through input TDI into the boundary scan register using the Update-DR state.

SAMPLE

The sample instruction samples all the device inputs and outputs. For this instruction, the boundary scan register is placed between TDI and TDO. Primary device inputs and outputs can be sampled by loading the boundary scan register using the Capture-DR state. The sampled values can then be viewed by shifting the boundary scan register using the Shift-DR state.

IDCODE

The identification instruction is used to connect the identification register between TDI and TDO. The device's identification code can then be shifted out using the Shift-DR state. The DualPHY 1G identification code has not been assigned at this time.

STCTEST

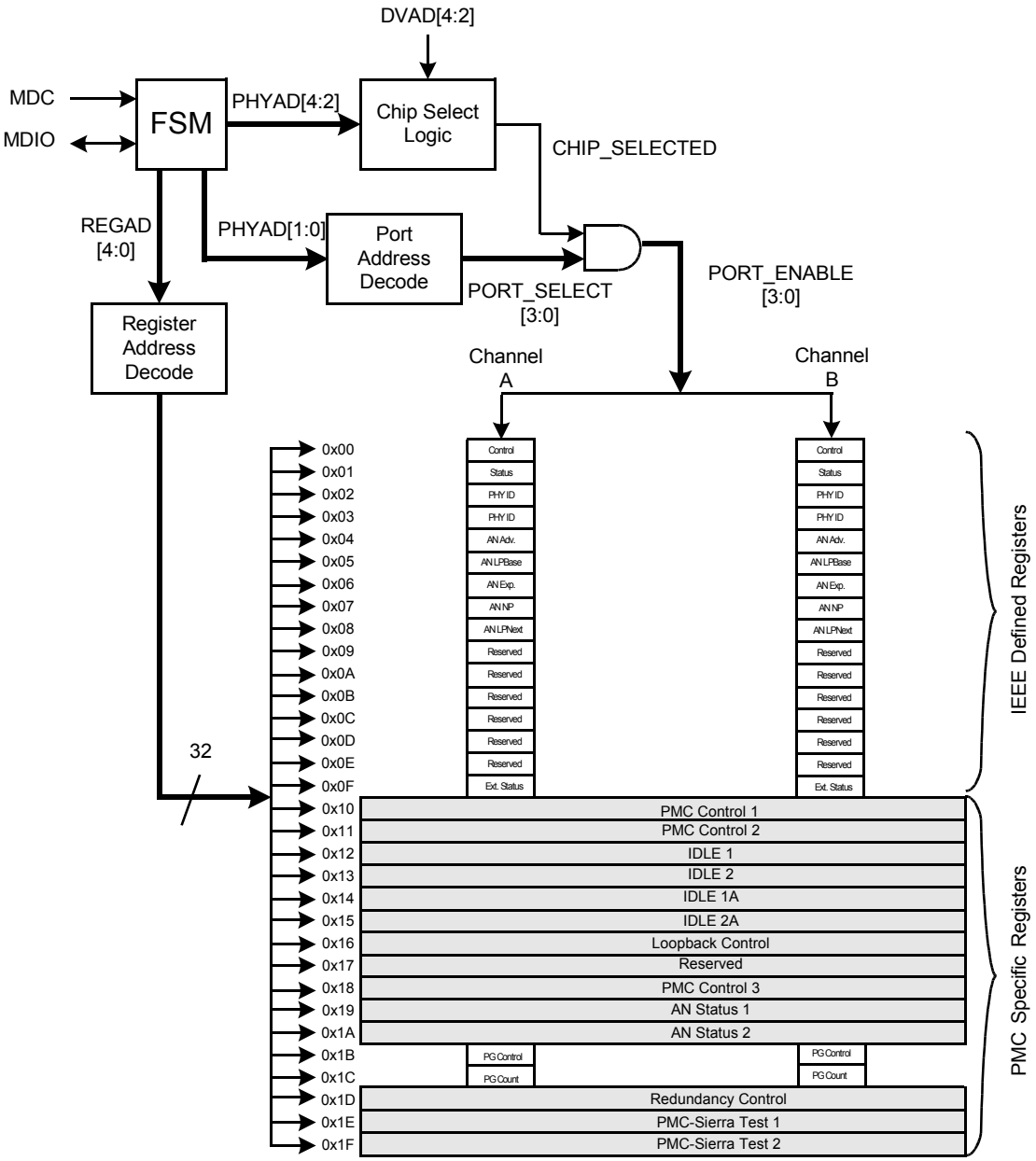
The single transport chain instruction is used to test out the TAP controller and the boundary scan register during production test. When this instruction is the current instruction, the boundary scan register is connected between TDI and TDO. During the Capture-DR state, the device identification code is loaded into the boundary scan register. The code can then be shifted out output, TDO using the Shift-DR state

10.5 Microprocessor Interface

The DualPHY 1G device implements a management interface that uses a protocol defined in *IEEE* 802.3. This two-wire interface is used for configuration, control, and status of up to sixteen DualPHY 1G devices. The two-wire interface consists of MDC (management data clock) and MDIO (management data I/O) terminals. This interface allows serial read/write of internal control and status registers.

The register map is defined in Table 19. Note that there are both global address registers, used for both channels and addressed only by bits PHYAD[4:2] of the management frame, and per-port address registers, addressed using all bits of PHYAD of the management frame. Figure 20 illustrates the addressing of both the global and per-port registers.

Figure 20 Register Access



Frames transmitted on the management interface have the frame structure shown in Table 17. The order of bit transmission is from left to right.

Table 17 Management Interface Frame Format

	PRE	ST	OP	PHYAD	REGAD	TA	Data	Idle
READ	1 1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1 1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

PRE (Preamble) - At the beginning of each transaction, the management interface controller sends a sequence of 32 contiguous logic '1' bits on MDIO with 32 corresponding cycles on MDC to provide the device with a pattern that it can use to establish synchronization. The device observes a sequence of 32 contiguous '1' bits on MDIO with 32 corresponding cycles on MDC before it responds to any transaction.

ST (Start of Frame) - is indicated by a <01> pattern. This pattern assures transitions from the default logic 1 line state to 0 and back to 1.

OP (Operation Code) - The operation code for a read transaction is <10>, while the operation code for a write transaction is <01>.

PHYAD (PHY Address) - is five bits, allowing 32 unique channel addresses. Although the DualPHY 1G device supports only two channels, each device consumes four channel addresses. Therefore, a total of eight DualPHY 1G devices are addressable on a single MDIO bus. The first PHY address bit transmitted and received is the MSB of the address.

The DualPHY 1G device will respond only when the PHYAD[4:2] bits match the DVAD[4:2] terminal values. (Note the DVAD[1:0] terminals are unused and should be tied to ground.) A given channel in the device is addressable by the PHYAD[1:0] bits, as shown in Table 18.

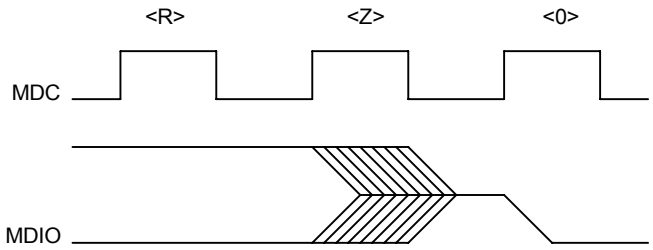
Table 18 PHYAD[1:0] Address Mapping

PHYAD[1]	PHYAD[0]	DualPHY 1G Channel
0	0	Reserved
0	1	Reserved
1	0	Channel A
1	1	Channel B

REGAD (Register Address) – is five bits, allowing 32 individual registers to be addressed within each DualPHY 1G device. The first Register Address bit transmitted and received is the MSB of the address.

TA (Turnaround) – is a two-bit-time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction. For a read transaction, both the management interface controller and the DualPHY 1G device remain in a high-impedance state for the first bit time of the turnaround. The DualPHY 1G device drives a 0 bit during the second bit time of the turnaround of a read transaction. During a write transaction, the management interface controller drives a 1 bit for the first bit time of the turnaround and a 0 bit for the second bit time of the turnaround.

Figure 21 Behavior of MDIO During TA Field of a Read Transaction



DATA - 16-bit field. The first data bit transmitted and received is bit 15 (MSB) of the register being addressed.

IDLE – logic state on MDIO is high-impedance. MDIO must be pulled high when not driven.

Table 19 Register Memory Map

Address (Hex)	Register
0x00	GMII Control
0x01	GMII Status
0x02	GMII PHY Identifier
0x03	GMII PHY Identifier
0x04	GMII Auto-Negotiation Advertisement
0x05	GMII Auto-Negotiation Link Partner Base Page Ability
0x06	GMII Auto-Negotiation Expansion
0x07	GMII Auto-Negotiation Next Page Transmit
0x08	GMII Auto-Negotiation Link Partner Next Page Received
0x09	GMII Reserved
0x0A	GMII Reserved
0x0B	GMII Reserved
0x0C	GMII Reserved
0x0D	GMII Reserved
0x0E	GMII Reserved
0x0F	GMII Extended Status

Address (Hex)	Register
0x10	PMC Control 1
0x11	PMC Control 2
0x12	IDLE 1
0x13	IDLE 2
0x14	IDLE 1A
0x15	IDLE 2A
0x16	Loopback Control
0x17	Reserved
0x18	PMC Control 3
0x19	Auto-Negotiation Status 1
0x1A	Auto-Negotiation Status 2
0x1B	Packet Generator/Checker Control/Status
0x1C	Packet Generator Count Control
0x1D	Redundancy Control Register
0x1E	Reserved/PMC Test 1
0x1F	Reserved/PMC Test 2

Note:

1. Registers 0x00 – 0x0F are only valid when PCS_ENABLE = 1.
2. Registers 0x1B and 0x1C are only valid when PCS_ENABLE = 0.

11 Normal Mode Register Description

Normal mode registers are used to configure and monitor the operation of the DualPHY 1G device.

Notes on Normal Mode Register Bits:

1. Writing values into unused register bits has no effect. However, to ensure software compatibility with future, feature-enhanced versions of the product, unused register bits must be written with logic 0. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read
2. In configuration bits that can be written into can also be read back. This allows the processor controlling the DualPHY 1G device to determine the programming state of the block
3. Writeable normal mode register bits are cleared to logic 0 upon reset unless otherwise noted
4. Writing into read-only normal mode register bit locations does not affect device operation unless otherwise noted
5. Certain register bits are reserved. These bits are associated with either reserved addresses dictated by the IEEE 802.3 standard or PMC-Sierra Test functions. To ensure that the DualPHY 1G device operates as intended, reserved register bits must be written with their default value as indicated by the register bit description

11.1 IEEE Defined Registers

Register 0x00: GMII Control

Bit	Type	Function	Default
Bit 15	R/W[1]	RESET	0
Bit 14	R/W	LOOPBACK	0
Bit 13	R	SPEED_SELECTION_LSB	0
Bit 12	R/W	AN_ENABLE	1
Bit 11	R/W	POWER_DOWN	0
Bit 10	R/W	ISOLATE	0
Bit 9	R/W[1]	RESTART_AN	0
Bit 8	R	DUPLEX_MODE	1
Bit 7	R	COLLISION_TEST	0
Bit 6	R	SPEED_SELECTION_MSB	1
Bit 5	R	RESERVED	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

Note:

1. When written with a 1, this bit self clears.

The GMII Control Register provides control over the basic functionality of the DualPHY 1G device. For additional information refer to *IEEE* Standard 802.3, Section 22.2.4.1.

SPEED_SELECTION_MSB

The SPEED_SELECTION_MSB bit is used in conjunction with the SPEED_SELECTION_LSB bit (bit 13) to select the speed of operation. Since the DualPHY 1G device only supports 1000Mbps operation, the SPEED_SELECTION_MSB is a read-only bit that is always set to logic 1.

COLLISION_TEST

The Collision Test function is not supported by the DualPHY 1G device. Therefore, the COLLISION_TEST bit is a read-only bit that is always set to logic 0.

DUPLEX_MODE

The DualPHY 1G device operates in full-duplex mode. Therefore, the DUPLEX_MODE bit is a read-only bit that is always set to logic 1.

RESTART_AN

If a PHY reports that it lacks the ability to perform Auto-Negotiation, or if Auto-Negotiation is disabled, the DualPHY 1G device will return a value of logic 0 in the RESTART_AN bit. If this is the case, the RESTART_AN bit should be written as logic 0 and any attempt to write logic 1 will be ignored. A PHY reports via the AN_ENABLE bit (bit 12).

Otherwise, the Auto-Negotiation process is started by setting the RESTART_AN to logic 1. This bit is self-clearing, and the RESTART_AN bit will return a logic 1 until the Auto-Negotiation process has been initiated. The Auto-Negotiation process is not affected by writing logic 0 into bit RESTART_AN bit.

ISOLATE

The ISOLATE bit is initialized to logic 0 for normal operation. If the ISOLATE bit is set to logic 1 and the DualPHY 1G device's PCS Logic is enabled, the associated transmit and receive channel data paths will be disabled and will be isolated from the GMII. If the PCS Logic is disabled, the state of the ISOLATE bit has no effect on the channel's operation.

POWER_DOWN

The associated channel on the DualPHY 1G device is placed in a low-power consumption state by setting the POWER_DOWN bit to logic 1. Clearing the POWER_DOWN bit to logic 0 allows for normal operation. The DualPHY 1G device's PCS Logic must be enabled to allow the POWER_DOWN bit to operate as specified. If the PCS Logic is disabled, the state of the POWER_DOWN bit has no effect on the channel's operation. While in the power-down state, the DualPHY 1G device responds to management transitions.

AN_ENABLE

The Auto-Negotiation process is enabled by setting the AN_ENABLE bit to logic 1. If the AN_ENABLE bit is enabled, the Speed Select and Duplex Mode bits have no effect on the link configuration other then providing status. If the AN_ENABLE bit is cleared to logic 0 then the Speed Select and Duplex Mode bits determines the link configuration.

SPEED_SELECTION_LSB

The SPEED_SELECTION_LSB bit is used in conjunction with the SPEED_SELECTION_MSB bit (bit 6) to select the speed of operation. Since the DualPHY 1G device supports only 1000 Mbit/s operation, the SPEED_SELECTION_LSB is a read-only bit that is always set to logic 0.

LOOPBACK

The DualPHY 1G device is placed into High-speed Serial Loopback Mode when the LOOPBACK bit is set to logic 1. When the LOOPBACK bit is set, the DualPHY 1G device accepts data from the GMII transmit data path and returns it to the GMII receive data path. Clearing the LOOPBACK bit to logic 0 allows the DualPHY 1G device to operate normally. The DIGITAL_LOOPBACK_EN Control Bit (Bit 7 of Register 0x18) must be set to logic 0 to operate this Serial Loopback Mode.

RESET

Setting this bit to logic 1 resets the associated channel in the DualPHY 1G device. This action sets the status and control registers to their default states. As a consequence, this action can change the internal state of the DualPHY 1G device and the state of the physical link associated with the DualPHY 1G device.

This bit is self-clearing and the device will return a logic 1 in bit 15 until the reset process is complete. The device is not required to accept a write transaction to the control register until the reset process is complete. Writing to bits of the control register other than bit 15 will have no effect until the reset process is completed.

Register 0x01: GMII Status

Bit	Type	Function	Default
Bit 15	R	100BASE-T4	0
Bit 14	R	100BASE-X_FULL_DUPLEX	0
Bit 13	R	100BASE-X_HALF_DUPLEX	0
Bit 12	R	10MBS_FULL_DUPLEX	0
Bit 11	R	10MBS_HALF_DUPLEX	0
Bit 10	R	100BASE-T2_FULL_DUPLEX	0
Bit 9	R	100BASE-T2_HALF_DUPLEX	0
Bit 8	R	EXTENDED_STATUS	1
Bit 7	R	RESERVED	0
Bit 6	R	MF_PREAMBLE_SUPPRESSION	1
Bit 5	R	AN_COMPLETE	0
Bit 4	R[1]	REMOTE_FAULT	0
Bit 3	R	AN_ABILITY	1
Bit 2	R[2]	LINK_STATUS	0
Bit 1	R	JABBER_DETECT	0
Bit 0	R	EXTENDED_CAPABILITY	1

Notes:

1. This bit latches high and is cleared when read
2. This bit latches low and is set when read

The GMII Status Register provides status over the basic functionality of the device. All of the bits in the Status Register are read-only; a write to this register has no effect. For additional information refer to *IEEE* Standard 802.3, Section 22.2.4.2.

EXTENDED_CAPABILITY

The EXTENDED_CAPABILITY bit is set to logic 1 which indicates that the DualPHY 1G device provides an extended set of capabilities that can be accessed through the extended register set.

JABBER_DETECT

The DualPHY 1G device is specified to operate at 1000 Mbit/s. PHYs specified to operate at this speed do not incorporate the Jabber Detect function, as this function is defined to be performed in the repeater unit at this speed. Therefore, the device always returns a logic 0 for JABBER_DETECT.

LINK_STATUS

When the LINK_STATUS bit is read as logic 1, it indicates that the DualPHY 1G device has determined that a valid link has been established. When read as logic 0, it indicates that the link is not valid. The LINK_STATUS bit is implemented with a latching function, such that the occurrence of a link failure will cause the LINK_STATUS bit to be cleared and remain cleared until the GMII Status Register is read.

AN_ABILITY

The DualPHY 1G device has the ability to perform Auto-Negotiation. Therefore, the AN_ABILITY bit will return logic 1 when read.

REMOTE_FAULT

When the REMOTE_FAULT bit is read as logic 1, it indicates that a remote fault condition has been detected. The REMOTE_FAULT bit is implemented with a latching function, such that the occurrence of a remote fault will cause the REMOTE_FAULT bit to be set and remain set until the GMII Register is read or when the device is reset.

AN_COMPLETE

When the AN_COMPLETE bit is read as logic 1, it indicates that the Auto-Negotiation process has been completed, and that the contents of the extended registers implemented by the Auto-Negotiation protocol are valid. The DualPHY 1G device returns a logic 0 in the AN_COMPLETE bit if Auto-Negotiation is disabled.

MF_PREAMBLE_SUPPRESSION

The DualPHY 1G device is capable of accepting management frames regardless of whether they are or are not preceded by the preamble pattern described in the IEEE Standard 802.3, Section 22.2.4.4.2. Therefore, the MF_PREAMBLE_SUPPRESSION bit returns a logic 1 when read.

EXTENDED_STATUS

The DualPHY 1G device provides extended base register status information in GMII register 0x0F. Therefore, this bit returns a logic 1 when read.

100BASE-T2_HALF_DUPLEX

The DualPHY 1G device does not support half duplex link transmission and reception using the 100BASE-T2 signaling specification. Therefore, this bit returns a logic 0 when read.

100BASE-T2_FULL_DUPLEX

The DualPHY 1G device does not support full duplex link transmission and reception using the 100BASE-T2 signaling specification. Therefore, this bit returns a logic 0 when read.

10MBS_HALF_DUPLEX

The DualPHY 1G device does not support half duplex link transmission and reception while operating at 10 Mb/s. Therefore, this bit returns a logic 0 when read.

10MBS_FULL_DUPLEX

The DualPHY 1G device does not support full duplex link transmission and reception while operating at 10 Mb/s. Therefore, this bit returns a logic 0 when read.

100BASE-X_HALF_DUPLEX

The DualPHY 1G device does not support half duplex link transmission and reception using the 100BASE-X signaling specification. Therefore, this bit returns a logic 0 when read.

100BASE-X_FULL_DUPLEX

The DualPHY 1G device does not support full duplex link transmission and reception using the 100BASE-X signaling specification. Therefore, this bit returns a logic 0 when read.

100BASE-T4

The DualPHY 1G device does not support link transmission and reception using the 100BASE-T4 signaling specification. Therefore, this bit returns a logic 0 when read.

Register 0x02: GMII PHY Identifier 1

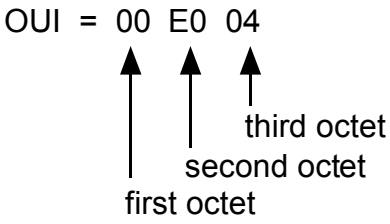
Bit	Type	Function	Default
Bit 15	R	PHY_ID_1[15]	0
Bit 14	R	PHY_ID_1[14]	0
Bit 13	R	PHY_ID_1[13]	0
Bit 12	R	PHY_ID_1[12]	0
Bit 11	R	PHY_ID_1[11]	0
Bit 10	R	PHY_ID_1[10]	0
Bit 9	R	PHY_ID_1[9]	0
Bit 8	R	PHY_ID_1[8]	0
Bit 7	R	PHY_ID_1[7]	0
Bit 6	R	PHY_ID_1[6]	0
Bit 5	R	PHY_ID_1[5]	0
Bit 4	R	PHY_ID_1[4]	1
Bit 3	R	PHY_ID_1[3]	1
Bit 2	R	PHY_ID_1[2]	1
Bit 1	R	PHY_ID_1[1]	0
Bit 0	R	PHY_ID_1[0]	0

The GMII PHY Identifier 1 register contains bits 3 through 18 of the Organizationally Unique Identifier (OUI) assigned to PMC-Sierra by the IEEE. This PHY Identifier is intended to provide sufficient information to support the ResourceTypeID object as required in *IEEE* Standard 802.3, Section 30.1.2.

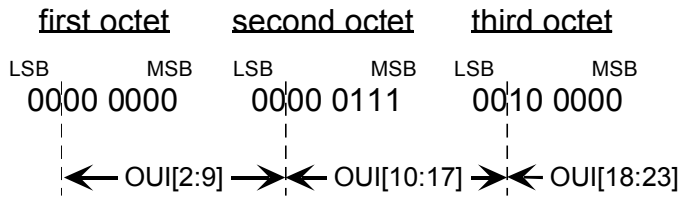
PHY_ID_1[15:0]

The PHY_ID_1 bits contain bits 3 through 18 of the Organizationally Unique Identifier (OUI). The 3rd bit of the OUI is assigned to PHY_ID_1[15], the 4th bit of the OUI is assigned to PHY_ID_1[14], and so on. Bit PHY_ID_1[0] contains the 18th bit of the OUI. The default setting for PHY_ID_1[15:0] is 0x001C.

The Organizationally Unique Identifier (OUI) field is a 24-bit field that extends across the two GMII PHY Identifier Registers. Its value is 0x00E004. The mapping of the OUI to the PHY Identifier registers is described below.



Each octet is represented as a conventional two digit hexadecimal numeral where the first (left-most) digit of the pair is the more significant. The mapping of the OUI to the GMII PHY Identifier registers of the DualPHY device 1G is described below.



PHY Identifier 1 [15:0] = OUI[2:17] = 001C

PHY Identifier 2 [15:10] = OUI[18:23] = 20

Register 0x03: GMII PHY Identifier 2

Bit	Type	Function	Default
Bit 15	R	PHY_ID_2[15]	1
Bit 14	R	PHY_ID_2[14]	0
Bit 13	R	PHY_ID_2[13]	0
Bit 12	R	PHY_ID_2[12]	0
Bit 11	R	PHY_ID_2[11]	0
Bit 10	R	PHY_ID_2[10]	0
Bit 9	R	PHY_ID_2[9]	0
Bit 8	R	PHY_ID_2[8]	0
Bit 7	R	PHY_ID_2[7]	0
Bit 6	R	PHY_ID_2[6]	1
Bit 5	R	PHY_ID_2[5]	0
Bit 4	R	PHY_ID_2[4]	1
Bit 3	R	PHY_ID_2[3]	0
Bit 2	R	PHY_ID_2[2]	0
Bit 1	R	PHY_ID_2[1]	0
Bit 0	R	PHY_ID_2[0]	0

The GMII PHY Identifier 2 register contains the 19th through 24th bits of the Organizationally Unique Identifier (OUI) assigned to PMC-Sierra by the IEEE, the six-bit Manufacturing Model Number and the four-bit Revision Number. The default value for the GMII PHY Identifier 2 register is 0x8050.

PHY_ID_2[3:0]

PHY_ID_2[3:0] contain the four-bit Revision Number of the DualPHY 1G device. The default setting for these bits change with device revision. The revision number for Revision A of the DualPHY 1G device is 0x00.

PHY_ID_2[9:4]

PHY_ID_2[9:4] contain the six-bit Manufacturing Model Number. The default setting for these bits is 0x05.

PHY_ID_2[15:10]

PHY_ID_2[15:10] contain the 19th through 24th bits of the Organizationally Unique Identifier (OUI). The default setting for these bits is 0x20.

Register 0x04: GMII Auto-Negotiation Advertisement

Bit	Type	Function	Default
Bit 15	R/W	NEXT_PAGE	0
Bit 14	R	RESERVED	0
Bit 13	R/W	REMOTE_FAULT[1]	0
Bit 12	R/W	REMOTE_FAULT[0]	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R/W	PAUSE[1]	0
Bit 7	R/W	PAUSE[0]	0
Bit 6	R/W	HALF_DUPLEX	0
Bit 5	R/W	FULL_DUPLEX	1
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

The GMII Auto-Negotiation Advertisement register contains the advertised ability of the DualPHY 1G device. Before Auto-Negotiation starts, this register is configured to advertise the abilities of the DualPHY 1G device.

FULL_DUPLEX

The DualPHY 1G device is capable of full-duplex operation. This bit is set to logic 1 for normal operation

HALF_DUPLEX

The DualPHY 1G device supports only full-duplex operation. This bit should be set to logic 0 for normal operation.

PAUSE[1:0]

PAUSE Capabilities. The DualPHY 1G device's PAUSE capability is encoded in bits 8:7. The decoding of these bits is shown in the Pause Encoding Table below.

[7]	[8]	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

REMOTE_FAULT[1:0]

The DualPHY 1G device's remote fault condition is encoded in bits 13:12 of the base page. Values are shown in Remote Fault Encoding Table shown below. The default value is 0b00. The DualPHY 1G device indicates a fault by setting a non-zero Remote Fault encoding and re-negotiating.

[12]	[13]	Description
0	0	No error, link OK
0	1	Offline
1	0	Link Failure
1	1	Auto-Negotiation Error

NEXT_PAGE

The base page and subsequent next pages can set the NEXT_PAGE bit to logic 1 to request next page transmission. Subsequent next pages can set the NEXT_PAGE bit to logic 0 in order to communicate that there is no more next page information to be sent.

Register 0x05: GMII Auto-Negotiation Link Partner Ability Base Page

Bit	Type	Function	Default
Bit 15	R	NEXT_PAGE	0
Bit 14	R	ACKNOWLEDGE	0
Bit 13	R	REMOTE_FAULT[1]	0
Bit 12	R	REMOTE_FAULT[0]	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R	PAUSE[1]	0
Bit 7	R	PAUSE[0]	0
Bit 6	R	HALF_DUPLEX	0
Bit 5	R	FULL_DUPLEX	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

The GMII Auto-Negotiation Link Partner Ability Base Page register contains the advertised ability of the link partner's base page. The values contained in the GMII Auto-Negotiation Link Partner Ability Base Page register are guaranteed to be valid either once the Auto-Negotiation has successfully completed, as indicated by the Auto-Negotiation Complete bit in the GMII Status register or when the Page Received bit in the GMII Auto-Negotiation Expansion Register is set to logic 1.

All of the bits in the GMII Auto-Negotiation Link Partner Ability Base Page register are read-only. A write to this register has no effect.

FULL_DUPLEX

If the FULL_DUPLEX bit is set to logic 1, the DualPHY 1G device's Link Partner is capable of operating in full-duplex mode. This bit is initialized to logic 0.

HALF_DUPLEX

If the HALF_DUPLEX bit is set to logic 1, the DualPHY 1G device's Link Partner is capable of operating in half-duplex mode. This bit is initialized to logic 0.

PAUSE[1:0]

PAUSE Capabilities. The Link Partner's PAUSE capability is encoded in bits 8:7. The decoding of these bits is shown in the Pause Encoding Table below.

[7]	[8]	Capability
0	0	No PAUSE
0	1	Asymmetric PAUSE toward link partner
1	0	Symmetric PAUSE
1	1	Both Symmetric PAUSE and Asymmetric PAUSE toward local device

REMOTE_FAULT[1:0]

The Link Partner's remote fault condition is encoded in bits 13:12 of the base page. Values are shown in Remote Fault Encoding Table shown below. The default value is 0b00. The Link Partner indicates a fault by sending a non-zero Remote Fault encoding and during Auto-Negotiation.

[12]	[13]	Description
0	0	No error, link OK
0	1	Offline
1	0	Link_Failure
1	1	Auto-Negotiation_Error

ACKNOWLEDGE

The Acknowledge (Ack) bit is used by the Auto-Negotiation function to indicate that the local device has successfully received its link partner's base page. When read as logic:

0: the device has not received the message.

1: the device has received the message.

NEXT_PAGE

The base page and subsequent next pages can set the NEXT_PAGE bit to logic 1 to indicate that there are additional next pages to be received. Subsequent next pages can set the NEXT_PAGE bit to logic 0 in order to communicate that there the last page has been received.

Register 0x06: GMII Auto-Negotiation Expansion

Bit	Type	Function	Default
Bit 15	R	RESERVED	0
Bit 14	R	RESERVED	0
Bit 13	R	RESERVED	0
Bit 12	R	RESERVED	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R	RESERVED	0
Bit 7	R	RESERVED	0
Bit 6	R	RESERVED	0
Bit 5	R	RESERVED	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	NEXT_PAGE_ABLE	1
Bit 1	R[1]	PAGE_RECEIVED	0
Bit 0	R	RESERVED	0

Notes:

1. This bit latches high and is cleared when read

All of the bits in the GMII Auto-Negotiation Expansion register are read-only. A write to this register has no effect.

PAGE_RECEIVED

The PAGE_RECEIVED bit is reset to logic 0 on a read to the GMII Auto-Negotiation Expansion register. After the Page Received bit is set, the Auto-Negotiation Link Partner Ability Next Page register should be read before the Auto-Negotiation Next Page Transmit register is written. This prevents overlaying the Auto-Negotiation Link Partner Ability Next Page register.

NEXT_PAGE_ABLE

The Next Page Able bit is set to logic 1 to indicate that the DualPHY 1G device supports the Next Page function.

Register 0x07: GMII Auto-Negotiation Next Page Transmit

Bit	Type	Function	Default
Bit 15	R/W	NEXT_PAGE	0
Bit 14	R	RESERVED	0
Bit 13	R/W	MESSAGE_PAGE	0
Bit 12	R/W	ACKNOWLEDGE_2	0
Bit 11	R	TOGGLE	0
Bit 10	R/W	MESSAGE_UNFORMATTED_CODE FIELD[10]	0
Bit 9	R/W	MESSAGE_UNFORMATTED_CODE FIELD[9]	0
Bit 8	R/W	MESSAGE_UNFORMATTED_CODE FIELD[8]	0
Bit 7	R/W	MESSAGE_UNFORMATTED_CODE FIELD[7]	0
Bit 6	R/W	MESSAGE_UNFORMATTED_CODE FIELD[6]	0
Bit 5	R/W	MESSAGE_UNFORMATTED_CODE FIELD[5]	0
Bit 4	R/W	MESSAGE_UNFORMATTED_CODE FIELD[4]	0
Bit 3	R/W	MESSAGE_UNFORMATTED_CODE FIELD[3]	0
Bit 2	R/W	MESSAGE_UNFORMATTED_CODE FIELD[2]	0
Bit 1	R/W	MESSAGE_UNFORMATTED_CODE FIELD[1]	0
Bit 0	R/W	MESSAGE_UNFORMATTED_CODE FIELD[0]	0

The GMII Auto-Negotiation Next Page Transmit register contains the advertised ability of the DualPHY 1G device's next page.

MESSAGE_UNFORMATTED_CODE FIELD[10:0]

The MESSAGE_UNFORMATTED_CODE FIELD is an eleven-bit-wide field, encoding 2048 possible messages. Message Code Field definitions are found in the IEEE 802.3u/Annex 28C.

TOGGLE

The TOGGLE bit is used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange. The bit is always set to the opposite value of the Toggle bit in the previously exchanged Link Code Word. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word and therefore can assume a value of logic 1 or zero.

ACKNOWLEDGE_2

The ACKNOWLEDGE_2 bit is used by next page function to indicate that a device has the ability to comply with the message. When read as logic:

0: the device cannot comply with message.
1: the device will comply with message.

MESSAGE_PAGE

The MESSAGE_PAGE bit is used by the Next Page function to differentiate a Message Page from an Unformatted Page. When read as logic:

0: Unformatted Page.

1: Message Page.

NEXT_PAGE

The NEXT_PAGE bit is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. When read as logic:

0: Last Page.

1: Additional Next Page(s) will follow.

Register 0x08: GMII Auto-Negotiation Link Partner Next Page Ability

Bit	Type	Function	Default
Bit 15	R	NEXT_PAGE	0
Bit 14	R	ACKNOWLEDGE	0
Bit 13	R	MESSAGE_PAGE	0
Bit 12	R	ACKNOWLEDGE_2	0
Bit 11	R	TOGGLE	0
Bit 10	R	MESSAGE_UNFORMATTED_CODE FIELD[10]	0
Bit 9	R	MESSAGE_UNFORMATTED_CODE FIELD[9]	0
Bit 8	R	MESSAGE_UNFORMATTED_CODE FIELD[8]	0
Bit 7	R	MESSAGE_UNFORMATTED_CODE FIELD[7]	0
Bit 6	R	MESSAGE_UNFORMATTED_CODE FIELD[6]	0
Bit 5	R	MESSAGE_UNFORMATTED_CODE FIELD[5]	0
Bit 4	R	MESSAGE_UNFORMATTED_CODE FIELD[4]	0
Bit 3	R	MESSAGE_UNFORMATTED_CODE FIELD[3]	0
Bit 2	R	MESSAGE_UNFORMATTED_CODE FIELD[2]	0
Bit 1	R	MESSAGE_UNFORMATTED_CODE FIELD[1]	0
Bit 0	R	MESSAGE_UNFORMATTED_CODE FIELD[0]	0

The GMII Auto-Negotiation Link Partner Next Page Ability register contains the ability of the link partner's next page. The GMII Auto-Negotiation Link Partner Next Page Ability register is a read only register. Any writes to this register will have no effect.

MESSAGE_UNFORMATTED_CODE FIELD[10:0]

The MESSAGE_UNFORMATTED_CODE FIELD is an eleven bit wide field, encoding 2048 possible messages. Message Code Field definitions are found in the IEEE 802.3u/Annex 28C.

TOGGLE

The TOGGLE bit is used by the Arbitration function to ensure synchronization with the Link Partner during Next Page exchange. The bit is always set to the opposite value of the Toggle bit in the previously exchanged Link Code Word. The initial value of the Toggle bit in the first Next Page transmitted is the inverse of bit 11 in the base Link Code Word and therefore can assume a value of logic 1 or 0.

ACKNOWLEDGE_2

The ACKNOWLEDGE_2 bit is used by next page function to indicate that a device has the ability to comply with the message. When read as logic:

0: the device cannot comply with message.

1: the device will comply with message.

MESSAGE_PAGE

The MESSAGE_PAGE bit is used by the Next Page function to differentiate a Message Page from an Unformatted Page. When read as logic:

0: Unformatted Page.

1: Message Page.

ACKNOWLEDGE

The ACKNOWLEDGE bit is used by the next page function to indicate that a device has received the message. When read as logic:

0: device has not received the message.

1: device has received the message.

NEXT_PAGE

The NEXT_PAGE bit is used by the Next Page function to indicate whether or not this is the last Next Page to be transmitted. When read as logic:

0: Last Page.

1: Additional Next Page(s) will follow.

Register 0x09 through 0x0E: Reserved

Bit	Type	Function	Default
Bit 15	R	RESERVED	0
Bit 14	R	RESERVED	0
Bit 13	R	RESERVED	0
Bit 12	R	RESERVED	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R	RESERVED	0
Bit 7	R	RESERVED	0
Bit 6	R	RESERVED	0
Bit 5	R	RESERVED	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

Registers 0x09 through 0x0E are reserved for future use. These registers are read-only. Any writes to these registers will have no effect.

Register 0x0F: GMII Extended Status

Bit	Type	Function	Default
Bit 15	R	1000BASE-X_FULL_DUPLEX	1
Bit 14	R	1000BASE-X_HALF_DUPLEX	0
Bit 13	R	1000BASE-T_FULL_DUPLEX	0
Bit 12	R	1000BASE-T_HALF_DUPLEX	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R	RESERVED	0
Bit 7	R	RESERVED	0
Bit 6	R	RESERVED	0
Bit 5	R	RESERVED	0
Bit 4	R	RESERVED	0
Bit 3	R	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

The Extended Status register is supported by the DualPHY 1G device. All bits in the Extended Status register are read-only. Any writes to this register will have no effect.

1000BASE-T_HALF_DUPLEX

This bit will always be read as logic 0, as the DualPHY 1G device does not support 1000BASE-T Half Duplex Operation.

1000BASE-T_FULL_DUPLEX

This bit will always be read as logic 0, as the DualPHY 1G device does not support 1000BASE-T Full Duplex Operation.

1000BASE-X_HALF_DUPLEX

This bit will always be read as logic 0, as the DualPHY 1G device does not support 1000BASE-X Half Duplex Operation.

1000BASE-X_FULL_DUPLEX

This bit will always be read as logic 1, as the DualPHY 1G device has the ability to perform full duplex link transmission and reception using the 1000BASE-X signaling specification.

11.2 PMC-Sierra Specific Registers

Register 0x10: PMC Control 1

Bit	Type	Function	Default
Bit 15	R/W	ENABLE_CHN_B	1
Bit 14	R	RESERVED	0
Bit 13	R/W	ENABLE_CHN_A	1
Bit 12	R	RESERVED	0
Bit 11	R/W	RESERVED	1
Bit 10	R	RESERVED	0
Bit 9	R/W	RESERVED	1
Bit 8	R	RESERVED	0
Bit 7	R/W	COMMA_DETECT_SEL[1]	1
Bit 6	R/W	COMMA_DETECT_SEL[0]	0
Bit 5	R/W	HIGH_AMPLITUDE	1
Bit 4	R	RESERVED	0
Bit 3	R/W	FILTER_COEFFICIENTS [3]	1
Bit 2	R/W	FILTER_COEFFICIENTS [2]	0
Bit 1	R/W	FILTER_COEFFICIENTS [1]	0
Bit 0	R/W	FILTER_COEFFICIENTS [0]	0

The PMC Control 1 register provides control over custom functionality in the DualPHY 1G device. This register controls functionality across both channels of the device.

FILTER_COEFFICIENTS[3:0]

These bits select the time constants of the digital filter of the clock recovery function. The requirement for advancing the phase of the recovered clock by 1/16 of a baud interval is that the difference between the number of late and early data edges exceeds 4x FILT[3:0]. While the clock phase tracking is not a linear control system, FILT[3:0] provide the capability to track frequency modulation (jitter) on the input waveforms ranging from approximately 1 MHz to 16 MHz without attenuation.

For proper operation, use the default setting. Values 0x1 through 0xF are valid. A value of 0x0 is not valid and should not be used.

HIGH_AMPLITUDE

This bit selects the drive capability for the TDO+ and TDO- terminals. When set to 1, the TDO+/TDO- terminals are configured for high-amplitude drive. When set to logic 0, the terminals are configured for low-amplitude drive

COMMA_DETECT_SEL[1:0]

These bits enable positive, negative, or both positive and negative comma detection. When COMMA_DETECT_SEL[1] is set to 1, positive comma detection is enabled. Setting COMMA_DETECT_SEL[0] to 1 enables negative comma detection.

ENABLE_CHN_A and B

The ENABLE_CHN bit enables or disables the operation of the associated Channel on the DualPHY 1G device. If these bits are set to logic 1 the associated channel is enabled. Both ENABLE_CHN bits are initialized to logic 1.

Register 0x11: PMC Control 2

Bit	Type	Function	Default
Bit 15	R/W	TXCLK4	0
Bit 14	R/W	CODE_VIOL_DIS_ENABLE	0
Bit 13	R/W	Reserved	1
Bit 12	R/W	Reserved	0
Bit 11	R/W	Reserved	0
Bit 10	R/W	Reserved	0
Bit 9	R/W	IPOEN	1
Bit 8	R/W	ENABLE_COMMA_DETECT	1
Bit 7	R/W	INT_DEC_ENC_ENABLE	0
Bit 6	R/W	MDE_CNTRL	0
Bit 5	R/W	INT_MODE_SEL[1]	0
Bit 4	R/W	INT_MODE_SEL[0]	0
Bit 3	R/W	SOFT_RESET	0
Bit 2	R/W	PCS_ENABLE	0
Bit 1	R/W	LINK_TIMER_MODE1	0
Bit 0	R/W	LINK_TIMER_MODE0	0

The PMC Control 2 register provides control over custom functionality in the DualPHY 1G device. This register controls functionality across both channels of the device.

LINK_TIMER_MODE[1:0]

These bits control the duration of the link timers within the Auto-Negotiation logic.

[1]	[0]	Duration
0	0	16.8 ms
0	1	12.6 ms
1	0	500 ns (test mode)
1	1	250 ns (test mode)

PCS_ENABLE

When this bit is set to logic 1, the chip processes PCS data and treats the parallel interface as GMII (8 bits of data plus TX_ER/TX_EN or RX_DV/RX_ER). PCS_ENABLE = 1 takes priority over GEMOD or GE_REG = 1.

SOFT_RESET

This bit resets all the logic and state machines in the receive and transmit channels to their original state. The PLL, configuration and status register bits are not affected by the assertion of this bit. This bit is NOT self-clearing. Once set by an MDC/MDIO access, it can be cleared immediately with another MDC/MDIO access. This bit is logically ORed with the SMRESET pin and provides the same functionality.

INT_MODE_SEL[1:0]

The Internal Mode Select bits control the DualPHY 1G device's mode of operation when the MDE_CNTRL bit is set to logic 1. The bit definition of the Internal Mode Select bits is shown below.

INT_MODE_SEL[1]	INT_MODE_SEL[0]	Description
0	0	LRRC Mode
0	1	Reserved
1	0	RRRC Mode
1	1	HRRC Mode

If the MDE_CNTRL bit is set to a logic 0, the MODE1 and MODE0 terminals control the DualPHY 1G device's mode of operation.

MDE_CNTRL

The MDE_CNTRL bit is used to select the control mode of the DualPHY 1G device. If set to logic 1, the INT_MODE_SEL[1:0] bits control the device mode. If set to logic 0, the mode terminals (MODE1, MODE0) control the device mode

INT_DEC_ENC_ENABLE

The INT_DEC_ENC_ENABLE bit is logically OR'd with the DEC_ENC_EN input terminal. It controls if the Internal Decoder/Encoder is enabled. If it is set to logic 1 the Internal Decoder/Encoder is enabled.

ENABLE_COMMA_DETECT

The ENABLE_COMMA_DETECT bit controls if the Comma Detect is enabled and if byte alignment will be performed on incoming comma sequences. Based on the configuration of the Comma Detect Select Bits in the PMC Control 1 Register, the comma alignment can be programmed to align on positive, negative, or both positive and negative commas. If this bit is set to logic 1, the Comma Detect is enabled.

IPOEN

The IPOEN bit controls the Internal Parallel Output Enable. This bit is logically ANDed with the POEN input terminal. If it is set to logic 1 the Parallel Outputs are enabled.

CODE_VIOL_DIS_ENABLE

The CODE_VIOL_DIS_ENABLE bit controls if the Internal Code Violation/Disparity Code is enabled. When set to logic 1, this bit enables the CV_DIS code function. It is logically OR'd with the CV_DIS_EN input terminal.

TXCLK4

The TXCLK4 bit controls the selection of the Transmit and Receive Clocks. If the TXCLK4 bit is set to logic 1, two separate TXCK input pins (TXCKB, and TXCKA) are active, each providing the input timing reference for the corresponding channels. When the TXCLK4 bit is set to logic 0, a single TXCK input (TXCKAB) is used as the timing reference for both input channels.

Register 0x12: IDLE 1

Bit	Type	Function	Default
Bit 15	R	RESERVED	0
Bit 14	R	RESERVED	0
Bit 13	R	RESERVED	0
Bit 12	R	RESERVED	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R/W	IDLE_1[8]	1
Bit 7	R/W	IDLE_1[7]	1
Bit 6	R/W	IDLE_1[6]	0
Bit 5	R/W	IDLE_1[5]	1
Bit 4	R/W	IDLE_1[4]	1
Bit 3	R/W	IDLE_1[3]	1
Bit 2	R/W	IDLE_1[2]	1
Bit 1	R/W	IDLE_1[1]	0
Bit 0	R/W	IDLE_1[0]	0

The PMC IDLE 1 register provides programmability for the first Idle code. The PMC IDLE 1 and IDLE 2 registers make up an IDLE pair.

IDLE_1[8:0]

The IDLE_1 Code bits allow the first IDLE character to be programmed. The default is set to 0x1BC (K28.5) when RESET is asserted. This default value is suitable for Gigabit Ethernet applications or for frequency compensation in serial backplane applications.

Register 0x13: IDLE 2

Bit	Type	Function	Default
Bit 15	R	RESERVED	0
Bit 14	R	RESERVED	0
Bit 13	R	RESERVED	0
Bit 12	R	RESERVED	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R/W	IDLE_2[8]	0
Bit 7	R/W	IDLE_2[7]	0
Bit 6	R/W	IDLE_2[6]	1
Bit 5	R/W	IDLE_2[5]	0
Bit 4	R/W	IDLE_2[4]	1
Bit 3	R/W	IDLE_2[3]	0
Bit 2	R/W	IDLE_2[2]	0
Bit 1	R/W	IDLE_2[1]	0
Bit 0	R/W	IDLE_2[0]	0

The PMC IDLE 2 register provides programmability for the second Idle code. The PMC IDLE and IDLE 2 registers make up an IDLE pair.

IDLE_2[8:0]

The IDLE_2 Code bits allow the second IDLE character to be programmed. The default is set to D16.2 when RESET is asserted. This default value is suitable for Gigabit Ethernet applications only. For frequency compensation in serial backplane applications, this value should be set to 0x11C (K28.0).

Register 0x14: IDLE 1A

Bit	Type	Function	Default
Bit 15	R	RESERVED	0
Bit 14	R	RESERVED	0
Bit 13	R	RESERVED	0
Bit 12	R	RESERVED	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R/W	IDLE_1A[8]	1
Bit 7	R/W	IDLE_1A[7]	1
Bit 6	R/W	IDLE_1A[6]	0
Bit 5	R/W	IDLE_1A[5]	1
Bit 4	R/W	IDLE_1A[4]	1
Bit 3	R/W	IDLE_1A[3]	1
Bit 2	R/W	IDLE_1A[2]	1
Bit 1	R/W	IDLE_1A[1]	0
Bit 0	R/W	IDLE_1A[0]	0

The PMC IDLE_1A register provides programmability for an alternate first Idle code. The PMC IDLE_1A and IDLE_2A registers make up an IDLE pair.

IDLE_1A[8:0]

The IDLE 1 Alternate Code bits allow the first IDLE character to be programmed. The default is set to K28.5 when RESET is asserted.

Register 0x15: IDLE 2A

Bit	Type	Function	Default
Bit 15	R	RESERVED	0
Bit 14	R	RESERVED	0
Bit 13	R	RESERVED	0
Bit 12	R	RESERVED	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R/W	IDLE_2A[8]	0
Bit 7	R/W	IDLE_2A[7]	0
Bit 6	R/W	IDLE_2A[6]	1
Bit 5	R/W	IDLE_2A[5]	0
Bit 4	R/W	IDLE_2A[4]	1
Bit 3	R/W	IDLE_2A[3]	0
Bit 2	R/W	IDLE_2A[2]	0
Bit 1	R/W	IDLE_2A[1]	0
Bit 0	R/W	IDLE_2A[0]	0

The PMC IDLE 2 register provides programmability for an alternate second Idle code. The PMC IDLE 1A and IDLE 2A registers make up an IDLE pair.

IDLE_2A[8:0]

The IDLE 2 Alternate Code bits allow the second IDLE character to be programmed. The default is set to D16.2 when RESET is asserted.

Register 0x16: Loopback Control

Bit	Type	Function	Default
Bit 15	R/W	INT_EN_PRI_SERIAL_LPBK_B	0
Bit 14	R/W	INT_EN_SEC_SERIAL_LPBK_B	0
Bit 13	R/W	INT_EN_ PRI_SERIAL_LPBK_A	0
Bit 12	R/W	INT_EN_ SEC_SERIAL_LPBK_A	0
Bit 11	R/W	RESERVED	0
Bit 10	R/W	RESERVED	0
Bit 9	R/W	RESERVED	0
Bit 8	R/W	RESERVED	0
Bit 7	R/W	EN_PAR_LPBK_B	0
Bit 6	R	RESERVED	0
Bit 5	R/W	EN_PAR_LPBK_A	0
Bit 4	R	RESERVED	0
Bit 3	R/W	RESERVED	0
Bit 2	R	RESERVED	0
Bit 1	R/W	RESERVED	0
Bit 0	R	RESERVED	0

The PMC Loopback Control register provides control over the DualPHY 1G device's serial and parallel loopback capabilities.

EN_PAR_LPBK_A:B

The EN_PAR_LPBK_A:B bits control the loop-back function for the parallel data on each channel. When these bits are set to a logic 1, the associated RXDy[9:0] outputs are routed to the corresponding channel inputs. In normal operation, the TXDy[9:0] inputs are routed to the channel inputs. If the EN_SLPBK pin is asserted, then EN_PAR_LPBK_A:B bits are ignored.

EN_PRI_SERIAL_LPBK_A:B and EN_SEC_SERIAL_LPBK_A:B

The EN_PRI_SERIAL_LPBK_A:B and EN_SEC_SERIAL_LPBK_A:B bits enable the loop-back function for the corresponding serial channel. When set to logic 1, the DualPHY 1G device routes the internal output of the Serializer to the input of the clock recovery block. The TDO+/TDO- terminals for the selected channel are held in the differential 1 state as long as these bits are active.

Internal Serial Loop-back must be coordinated with the Redundancy Control Register's (0x1D) Channel Select Bits so that the transmit primary and secondary channels are paired with their receive channel counterparts.

The EN_PRI_SERIAL_LPBK_A:B and EN_SEC_SERIAL_LPBK_A:B bits are logically OR'd with the input terminal EN_SLPBK.

Register 0x17: Reserved

Bit	Type	Function	Default
Bit 15	R/W	RESERVED	0
Bit 14	R/W	RESERVED	0
Bit 13	R/W	RESERVED	0
Bit 12	R/W	RESERVED	0
Bit 11	R[1]	RESERVED	0
Bit 10	R[1]	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R/W	RESERVED	1
Bit 7	R/W	RESERVED	0
Bit 6	R/W	RESERVED]	1
Bit 5	R/W	RESERVED]	1
Bit 4	R/W	RESERVED]	1
Bit 3	R/W	RESERVED	1
Bit 2	R/W	RESERVED	1
Bit 1	R/W	RESERVED	0
Bit 0	R/W	RESERVED]	0

Register 0x18: PMC Control 3

Bit	Type	Function	Default
Bit 15	R/W	GE_REG	0
Bit 14	R/W	BUSY_REG	0
Bit 13	R/W	RESERVED	0
Bit 12	R/W	INS_DEL_DIS	0
Bit 11	R	RESERVED	0
Bit 10	R/W	RESERVED	1
Bit 9	R/W	BA_HYSAT_EN	0
Bit 8	R/W	RESERVED	1
Bit 7	R/W	DIGITAL_LPBK_EN	0
Bit 6	R/W[1]	CODE_ERR_STB	0
Bit 5	R/W	RESERVED	0
Bit 4	R/W	RXCLK4	0
Bit 3	R/W	SYNC_ERR_CODE_EN	0
Bit 2	R	RESERVED	0
Bit 1	R	RESERVED	0
Bit 0	R	RESERVED	0

Notes:

1. When written with a 1, this bit self clears.

The PMC Control 3 register provides control over custom functionality in the DualPHY 1G device. This register controls functionality across both channels of the device.

SYNC_ERR_CODE_EN

When the SYNC_ERR_CODE_EN bit is set to logic 1, the DualPHY 1G device will output a 0x3FF value on the channel's parallel receive bus, if its synchronization state machine enters the LOSS_OF_SYNC state. The 0x3FF value will be output until the state machine regains synchronization. The operation of SYNC_ERR_CODE_EN is not dependent on the state of the BA_HYST_EN control bit.

When the SYNC_ERR_CODE_EN bit is set to logic 0, the state of the channel's synchronization state machine has no effect on the data that is output on its parallel receive bus.

If a particular differential serial input is unconnected (floating) and both the CODE_VIOL_DIS_ENABLE and SYNC_ERR_CODE_EN bits are asserted, the receive bus will output a pure stream of 0x3FFs. Note that it is possible that there will be an occasional valid code due to the random nature of the data.

RXCLK4

The RXCLK4 bit controls the enabling of the Receive Clocks while operating in LRRC or Parallel Loopback Modes. If set to logic 1, the RBCB0 clock is output on the RBCA0 pin and RBCB1 is output on the RBCA1 pin. If the RXCLK4 bit is set to logic 0, the RBCA0 and RBCA1, pins are inactive while operating in LRRC Mode.

CODE_ERR_STB

When set to logic 1, CODE_ERR_STB will clear all 8B/10B code error counters within the 8B/10B decoder blocks. The CODE_ERR_STB bit is self-clearing. When set to logic 0, the 8B/10B code error counters will continue to increment on received code errors until the maximum count, CODE_ERR_THR[14:0] is reached. CODE_ERR_THR is equivalent to PKT_CNT[14:0] in the Packet Generator Control register when EN_CODE_ERR_CHK is logic 1.

DIGITAL_LPBK_EN

When set to logic 1, DIGITAL_LPBK_EN enables the INT_EN_SERIAL_LPBK_[B:A] bits in the Loopback Control register to enable the purely digital loopback path per channel. This path is from the output of the encoder in the transmit path to the input of the byte alignment logic in the receive path.

When set to logic 0, DIGITAL_LPBK_EN enables the INT_EN_SERIAL_LPBK_[B:A] bits in the Loopback Control register to enable the high-speed serial loopback path. Note that digital loopback is only valid when primary channels are selected. Selecting secondary channels while the DIGITAL_LPBK_EN is asserted is not valid and will cause the part to malfunction.

BA_HYST_EN

When set to logic 1, BA_HYST_EN enables the byte synchronization state machine within the byte alignment logic to control when the byte alignment logic can realign to a comma.

When BA_HYST_EN is set to logic 0, the byte alignment logic will realign immediately to a received comma pattern.

INS_DEL_DIS

The INS_DEL_DIS bit controls whether the DualPHY 1G device inserts or deletes IDLEs into its Receive FIFOs for clock compensation. When the INS_DEL_DIS bit is set to logic 1, the DualPHY 1G device will not insert and delete IDLEs from its Receive FIFO. If the INS_DEL_DIS bit is set to logic 0, the DualPHY 1G device inserts and delete IDLEs from its Receive FIFO.

BUSY_REG

The BUSY_REG bit is used to enable or disable the Busy Mode. Busy Mode functionality is only valid when Gigabit Ethernet Mode is enabled. When the BUSY_REG is set to logic 1, the following function is enabled:

- /K28.5/D10.1/ sequences are treated as non-IDLE. Therefore, they are not modified by the insert/delete logic.

When the BUSY_REG is set to logic 0, the /K28.5/D10.1/ sequence is treated as IDLE and can be repeated or deleted by the insert/delete logic.

This BUSY_REG bit is logically OR'd with the BMOD input terminal.

GE_REG

The GE_REG bit is used to enable or disable the Gigabit Ethernet Mode. When the GE_REG bit is set to logic 1, the following functions are enabled:

- Configuration words that pass through the PHY during the Auto-Negotiation process may be inserted/deleted for frequency compensation
- /K28.5/ followed by any non-K character are recognized as an IDLE sequence which can be inserted or deleted for frequency compensation (except when BMOD is asserted, chip will treat /K28.5/D10.1/ as described in BMOD pin description)
- Modify IDLE to correct disparity by substituting /D5.6/ for /D16.2/ in a /K28.5/Dx.y/ transmit IDLE pair.

The GE_REG bit is logically ORed with the GEMOD input terminal. PCS_ENABLE must be set to logic 0 when GE_REG is set to logic 1.

Register 0x19: Auto-Negotiation Status 1

Bit	Type	Function	Default
Bit 15	R[1]	BASE_PAGE_RX_B	0
Bit 14	R[1]	RESERVED	0
Bit 13	R[1]	BASE_PAGE_RX_A	0
Bit 12	R[1]	RESERVED	0
Bit 11	R[1]	RESERVED	0
Bit 10	R[1]	RESERVED	0
Bit 9	R[1]	RESERVED	0
Bit 8	R[1]	RESERVED	0
Bit 7	R[1]	NEXT_PAGE_RX_B	0
Bit 6	R[1]	RESERVED	0
Bit 5	R[1]	NEXT_PAGE_RX_A	0
Bit 4	R[1]	RESERVED	0
Bit 3	R[1]	RESERVED	0
Bit 2	R[1]	RESERVED	0
Bit 1	R[1]	RESERVED	0
Bit 0	R[1]	RESERVED	0

Notes:

1. This bit latches high and is cleared when read

The Auto-Negotiation Status 1 register provides Base Page and Next Page reception status for each channel of the DualPHY 1G device.

NEXT_PAGE_RX_A and B

The NEXT_PAGE_RX bit indicates if a Next Page has been successfully received on the specified Channel. Both NEXT_PAGE_RX bits are cleared on a read.

BASE_PAGE_RX_A and B

The BASE_PAGE_RX bits indicate if a Base Page has been successfully received on the specified Channel. Both BASE_PAGE_RX bits are cleared on a read.

Register 0x1A: Auto-Negotiation Status 2

Bit	Type	Function	Default
Bit 15	R	AN_CMPLETE_B	0
Bit 14	R	RESERVED	0
Bit 13	R	AN_CMPLETE_A	0
Bit 12	R	RESERVED	0
Bit 11	R	RESERVED	0
Bit 10	R	RESERVED	0
Bit 9	R	RESERVED	0
Bit 8	R	RESERVED	0
Bit 7	R[1]	BYTE_ALIGN_STAT_B	0
Bit 6	R[1]	RESERVED	0
Bit 5	R[1]	BYTE_ALIGN_STAT_A	0
Bit 4	R[1]	RESERVED	0
Bit 3	R[1]	RESERVED	0
Bit 2	R[1]	RESERVED	0
Bit 1	R[1]	RESERVED	0
Bit 0	R[1]	RESERVED	0

Notes:

1. This bit latches low and is set when read

The Auto-Negotiation Status 2 register provides Auto-Negotiation Complete status for each channel of the DualPHY 1G device.

BYTE_ALIGN_STAT_A and B

The BYTE_ALIGN_STAT provide byte alignment status. When read as logic 0, the byte synchronization state machine within the byte alignment logic for the specified channel has determined that byte alignment has been lost. This failure indication will be sustained until register 0x1A is read even if byte alignment is regained.

When read as logic 1, the byte synchronization state machine within the byte alignment logic for the associated channel has determined that byte alignment has been achieved.

AN_CMPLETE_A and B

The AN_CMPLETE bits indicate if the Auto-Negotiation has completed on the specified Channel of the DualPHY 1G device.

Register 0x1B: Packet Generator/Checker Control/Status

Bit	Type	Function	Default
Bit 15	R/W	EN_PKT_GEN	0
Bit 14	R/W	EN_PKT_COMP	0
Bit 13	R/W[1]	ERROR_CNT_RESET	0
Bit 12	R/W[1]	FORCE_ERROR	0
Bit 11	R/W	EN_CODE_ERR_CHK	0
Bit 10	R[2]	CODE_ERR_EXCEED	0
Bit 9	R[2]	RXFIFO_RESYNC	0
Bit 8	R[2]	TXFIFO_RESYNC	0
Bit 7	R	ERROR_CNT[7]	0
Bit 6	R	ERROR_CNT[6]	0
Bit 5	R	ERROR_CNT[5]	0
Bit 4	R	ERROR_CNT[4]	0
Bit 3	R	ERROR_CNT[3]	0
Bit 2	R	ERROR_CNT[2]	0
Bit 1	R	ERROR_CNT[1]	0
Bit 0	R	ERROR_CNT[0]	0

Notes:

1. When written with a 1, this bit self clears.
2. This bit latches high and is cleared when read

The Packet Generator/Checker Control/Status register provides control and status information for DualPHY 1G device's Packet Generator and Checker capabilities. The DualPHY 1G device provides a Packet Generator/Checker Control/Status register for each channel.

ERROR_CNT[7:0]

The ERROR_CNT bits identify the number of errors that have occurred on the associated channel. This counter resets to 0x00h upon set the ERROR_CNT RESET bit. The Error Counter does not rollover when it reaches its maximum count of 0xFFh. It holds the 0xFFh value until it is reset.

TXFIFO_RESYNC

When read as logic 1, the TXFIFO_RESYNC bit indicates that the transmit FIFO within the channel has resynchronized its read and write pointers to avoid pointer collision. This resynchronization indication will be sustained until register 0x1B is read.

RXFIFO_RESYNC

When read as logic 1, the RXFIFO_RESYNC bit indicates that the Receive FIFO within the channel has resynchronized its read and write pointers to avoid pointer collision. This resynchronization indication will be sustained until register 0x1B is read.

CODE_ERR_EXCEED

When read as logic 1, the CODE_ERR_EXCEED bit indicates that the 8B/10B code error counter within the decoder logic has exceeded the error count threshold, CODE_ERR_THR[14 :0]. CODE_ERR_THR is equivalent to PKT_CNT[14 :0] in register 0x1C when EN_CODE_ERR_CHK is set to logic 1.

When the error count exceeds the CODE_ERR_THR, CODE_ERR_EXCEED will be sustained as logic 1 until register 0x1B is read. The 8B/10B coding error counters in all channels will be cleared whenever the CODE_ERR_STB bit in register 0x18 is set to logic 1.

The Code Error test feature can be used with the Packet Generator enabled and operating in Continuous Test Generation Mode.

EN_CODE_ERR_CHK

When set to logic 1, the 8B/10B code error counter within the decoder logic will count received code errors and will indicate that the count has exceeded the CODE_ERR_THR count by setting CODE_ERR_EXCEED to logic 1.

When set to logic 0, the 8B/10B code error counter is disabled.

FORCE_ERROR

The FORCE_ERROR bit forces the packet generator to create a single byte error in the next data byte or in the next packet if IDLE is currently being generated. This bit is self clearing.

ERROR_CNT_RESET

The ERROR_CNT_RESET bit resets the Error Counter to 0x00. This bit is self clearing.

EN_PKT_COMP

The EN_PKT_COMP bit enables the Packet Comparator for an associated channel.

EN_PKT_GEN

The EN_PKT_COMP bit enables the Packet Generator for an associated channel.

Register 0x1C: Packet Generator Count Control

Bit	Type	Function	Default
Bit 15	R/W	CONT_TEST_GEN	0
Bit 14	R/W	PKT_CNT[14]	0
Bit 13	R/W	PKT_CNT[13]	0
Bit 12	R/W	PKT_CNT[12]	0
Bit 11	R/W	PKT_CNT[11]	0
Bit 10	R/W	PKT_CNT[10]	0
Bit 9	R/W	PKT_CNT[9]	0
Bit 8	R/W	PKT_CNT[8]	0
Bit 7	R/W	PKT_CNT[7]	0
Bit 6	R/W	PKT_CNT[6]	0
Bit 5	R/W	PKT_CNT[5]	0
Bit 4	R/W	PKT_CNT[4]	0
Bit 3	R/W	PKT_CNT[3]	0
Bit 2	R/W	PKT_CNT[2]	0
Bit 1	R/W	PKT_CNT[1]	0
Bit 0	R/W	PKT_CNT[0]	0

The Packet Generator Count Control register provides control over the Packet Generator capabilities. The DualPHY 1G device provides a Packet Generator Count Control register for each channel.

PKT_CNT[14:0]

The PKT_CNT bits define the total number of frames that the Packet Generator will send for an associated channel.

In order to generate a fixed number of packets, the desired packet count must be first written into PKT_CNT[14:0], then the packet generator must be turned on by setting Bit 15 in register 0x1B to a logic 1 (EN_PKT_GEN). Once the packet generator finishes sending packets, it will go back to sending idle pairs. Additional sets of packets can be generated by toggling the EN_PKT_GEN bit from logic 0 to logic 1.

PKT_CNT is also used to define the 8B/10B code error threshold, CODE_ERR_THR, when EN_CODE_ERR_CHK is set to logic 1. The 8B/10B code error counter within the decoder logic will count received code errors and will indicate that the count has exceeded the CODE_ERR_THR count by setting CODE_ERR_EXCEED to logic 1. The valid range for the Code Error Threshold is 0x0000 to 0x7FFE. A value of 0x7FFF will not set the CODE_ERR_EXCEED to logic 1.

CONT_TEST_GEN

The CONT_TEST_GEN bit controls whether the Packet Generator for an associated channel will send continues frames or if it will send the PKT_CNT[14 :0] number of frames. If the CONT_TEST_GEN bit is set to logic 1, it will send an unlimited number of frames. If it is set to logic 0, the number of frames will be limited by the value set in the PKT_CNT[14 :0] bits.

Register 0x1D: Redundancy Control

Bit	Type	Function	Default
Bit 15	R/W	RESERVED	0
Bit 14	R/W	RESERVED	0
Bit 13	R/W	RESERVED	0
Bit 12	R/W	RESERVED	0
Bit 11	R/W	TX_CHAN_ENB_B[1]	0
Bit 10	R/W	TX_CHAN_ENB_B[0]	1
Bit 9	R/W	TX_CHAN_ENB_A[1]	0
Bit 8	R/W	TX_CHAN_ENB_A[0]	1
Bit 7	R/W	RESERVED	0
Bit 6	R/W	RESERVED	1
Bit 5	R/W	RESERVED	0
Bit 4	R/W	RESERVED	1
Bit 3	R/W	RX_CHN_SEL_B	0
Bit 2	R/W	RX_CHN_SEL_A	0
Bit 1	R/W	RESERVED	0
Bit 0	R/W	RESERVED	0

The Redundancy Control register provides control over the selection of the high-speed channels' primary and secondary inputs and outputs.

It is important to note that during internal serial data loopback testing, channel loopback enable bits in the Loopback control register must be coordinated with the redundancy control register's channel select bits so that transmit primary and secondary channels are paired with their receive channel counterparts.

TX_CHAN_ENB_A:B[1:0]

The TX_CHAN_ENB_A:B bits control which high speed serial output is enabled for channels A and B.

[1]	[0]	Delay
0	0	Primary Output Disabled Secondary Output Disabled
0	1	Primary Output Enabled Secondary Output Disabled
1	0	Primary Output Disabled Secondary Output Enabled
1	1	Primary Output Enabled Secondary Output Enabled

RX_CHN_SEL_A:B

The RX_CHAN_SEL_A:B bits control which high speed serial input is selected for channels A thru D. If the receive channel select bit for the associated channel is set to logic 0, the primary high speed input is selected. If the channel select bit is set to logic 1, the secondary high speed input is selected.

12 Test Features Description

12.1 Packet Generator and Packet Comparator

There is one packet generator and one packet comparator for each channel in the device. A packet generator is located within the transmit logic of each channel. A packet comparator is located within the receive logic of each channel.

Turning on the packet generator in a particular lane causes the transmit logic to ignore data which is present on that lane's transmit parallel input ports. Normally the transmit data is serialized and sent to its respective serial output; however with the packet generator enabled, the output of the packet generator is serialized instead and then sent to its respective serial output.

When a packet comparator is enabled, data which is received goes to both the packet comparator and its respective parallel outputs. This allows the actual data that is received to be snooped, if necessary, for debugging purposes.

The packet generator and comparator can only be operated while the device is configured for LRRC with PCS disabled. Other modes are not supported.

The packet generators and packet comparator are intended for test and diagnostics of the part, board or system. No logic is included to provide graceful transitions between normal operation and packet generation operation, so transition artifacts are likely to occur at the parallel receiver outputs. When disabling the packet generator, a soft reset is recommended for proper device operation.

12.1.1 Practical Uses of the Packet Generator and Packet Comparators

The packet generators and packet comparators can be used very effectively in internal serial loopback mode to confirm the operation of individual channels within the device.. When used in this manner, the packet generator of channel A communicates to the packet comparator of channel A, and the packet generator of channel B communicates to the packet comparator of channel B. This checks the majority of the analog and digital circuitry within this particular channel. However it does not check the analog or digital I/O.

The packet generator of a particular lane does not necessarily have to be used with the packet comparator of that same lane. In fact for a particular serial link, the packet generator of one device can communicate to the packet comparator of another device. This set-up is useful for verifying that a particular link is working. It also tests the analog outputs of the packet-generating device and the analog inputs of the packet-receiving device.

12.1.2 Packet Generator Operation

The packet generator creates a repetitive pattern of packets and IPG. The pattern is created as 8B data. The packet generator is started by setting the EN_PKT_GEN bit (Register 0x1B, bit 15). It sends a number of packets and then idles until it is disabled. The packet data is fixed and contains 256 characters, starting with 0x00 and incrementing to 0xFF. The number of packets, N, is configured in Register 0x28 and ranges from 1 to (2^{15}-1). The packet generator may also be configured to send continuous packets..

When the generator is enabled, 256 idle pairs are sent before packets are transmitted, and an IPG of ten idle pairs is sent between packets. After the N packets have been sent, idle pairs are sent continuously until the generator is disabled.

To test for stuck-at-0 faults in the packet comparator logic, errors can be introduced into the data packet by setting the FORCE_ERROR bit (Register 0x1B, bit 12). This is a self-clearing bit that forces one error in the data packet each time it is set. An error is created by replacing a character with the repeat of the preceding character, instead of the next character in the sequence. For instance, if the Packet Generator senses that the FORCE_ERROR bit is set during a data packet when 0x07 is being generated, the character after 0x07 would normally be 0x08. However, 0x07 will be repeated instead.

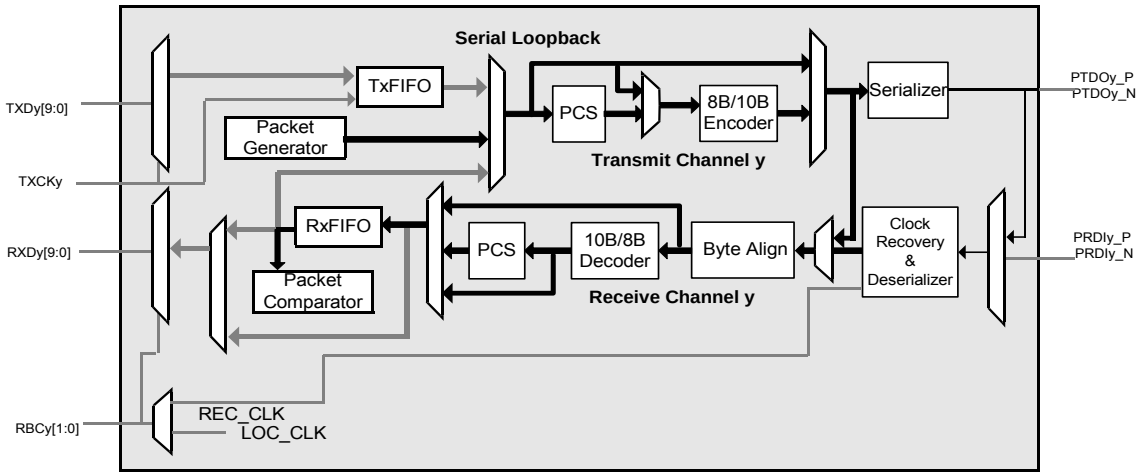
If the Packet Generator senses that the FORCE_ERROR bit is high during the IPG, SOP or EOP, the sequence 0x00, 0x00, 0x02h, etc. is sent at the start of the packet instead of the normal 0x00, 0x01, 0x02, etc. Finally, if the Packet Generator senses that the FORCE_ERROR bit is high during the 0xFF byte of the packet, the EOP is replaced with the data character 0xFF.

12.1.3 Packet Comparator Operation

The packet comparator looks for packets of 256 bytes starting with 0x00 and incrementing to 0xFF, framed by SOP and EOP. Idles are not checked or counted. If SOP is encountered and the subsequent 256 characters are not the sequence 0x00 to 0xFF followed by EOP, the error count in Register 0x1B is incremented.

To start the packet checker, EN_PKT_COMP, Register 0x1B, bit 14, must be set to 1. The error count is cleared by setting ERROR_CNT_RESET = 1 (Register 0x1B, bit 13). ERROR_CNT_RESET is self-clearing.

Figure 22 Serial Loopback Data Path, Packet Generator/Comparator Enabled



Links between two different DualPHY 1G devices can also be tested. Enabling the appropriate packet generator in the source DualPHY 1G device and the packet comparator in the sink DualPHY 1G device will accomplish this. The packet generator in a source DualPHY 1G device and the packet comparator in the sink DualPHY 1G device must be enabled. Serial Loopback in both devices is disabled.

12.2 JTAG Test Access Port

The DualPHY 1G JTAG Test Access Port (TAP) allows access to the TAP controller and the four TAP registers: instruction, bypass, device identification and boundary scan. Using the TAP, device input logic levels can be read, device outputs can be forced, the device can be identified and the device scan path can be bypassed. For more details on the JTAG port, please refer to the Operations section.

Table 20 Instruction Register

Instructions	Selected Register	Instruction Codes, IR[2:0]
EXTEST	Boundary Scan	000
IDCODE	Identification	001
SAMPLE	Boundary Scan	010
BYPASS	Bypass	011
BYPASS	Bypass	100
STCTEST	Boundary Scan	101
BYPASS	Bypass	110
BYPASS	Bypass	111

Table 21 Identification Register

Length	32 bits
Version number	0x0
Part Number	0x8354
Manufacturer's identification code	0x0CD
Device identification	0x083540CD

13 Operation

13.1 Power-up

The DualPHY 1G device can start in hardware only mode, without any microprocessor intervention, in all major operational modes. Table 22 shows pins that are available on the DualPHY 1G device for hardware only configuration.

A microprocessor interface is required for testing and debugging, and for activating the PCS logic within the DualPHY 1G device. A microprocessor is also needed for activating various loopback and packet generation/checking functionality.

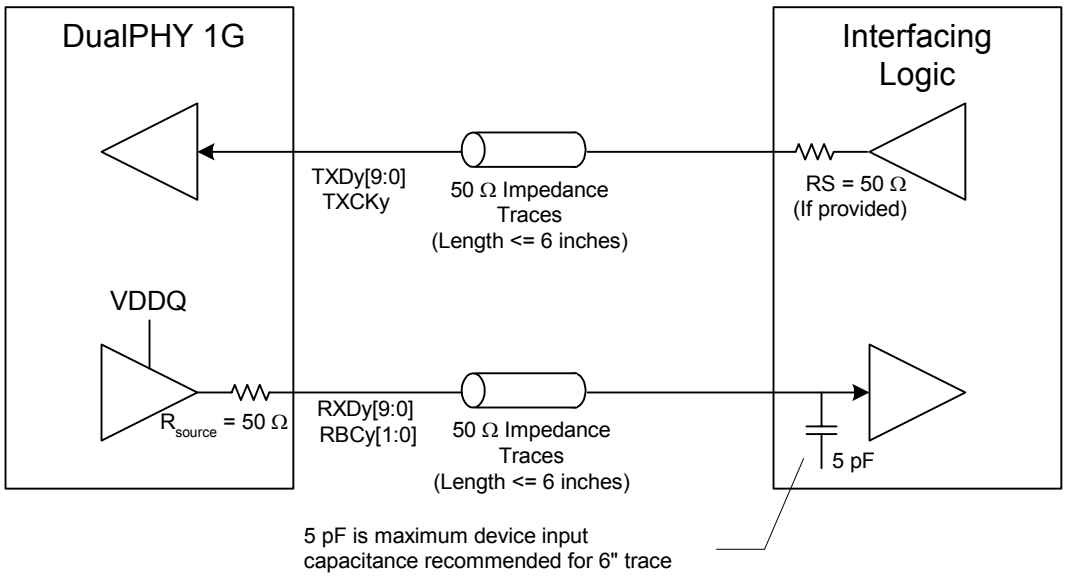
Power may be applied to the DualPHY 1G pins in any order. This includes the condition where VDD and VDDA are 1.8 V and VDDQ = 2.5 V.

13.2 Parallel Interface

The parallel interface uses CMOS input and output buffers that can operate at either 2.5 V or 1.8 V levels. The output buffer has an integrated series termination resistor providing output impedance of 50 Ω. The input buffer is a standard CMOS input, with no internal terminations. Figure 23 shows the recommended configuration of the parallel interface.

The interface is designed to operate over unterminated 50 Ω PCB traces. The maximum length of each trace should not exceed six inches. If trace lengths greater than six inches are necessary, PMC-Sierra strongly recommends that transmission line modeling and analysis be performed to evaluate the actual performance of the interface.

Figure 23 Parallel Receive and Transmit Interface



The parallel output drivers of the DualPHY 1G device drive traces which connect to the input pins of a receiving device. The minimum high (V_{oh}) and maximum low (V_{ol}) voltage levels which these inputs see are functions of silicon process variation, temperature and supply voltage of the DualPHY 1G device. Additionally, voltage levels at the input pins of the receiving device will be affected by the following:

- trace impedance
- length of the interconnecting trace
- input pin capacitance
- frequency of operation

It is important to note that these voltage levels do not necessarily correspond to the V_{oh} and V_{ol} levels that are specified in Table 25 of the D.C. Characteristics section. PMC-Sierra recommends that transmission line modeling and analysis be used to determine the dynamic performance of the interface with a specific application

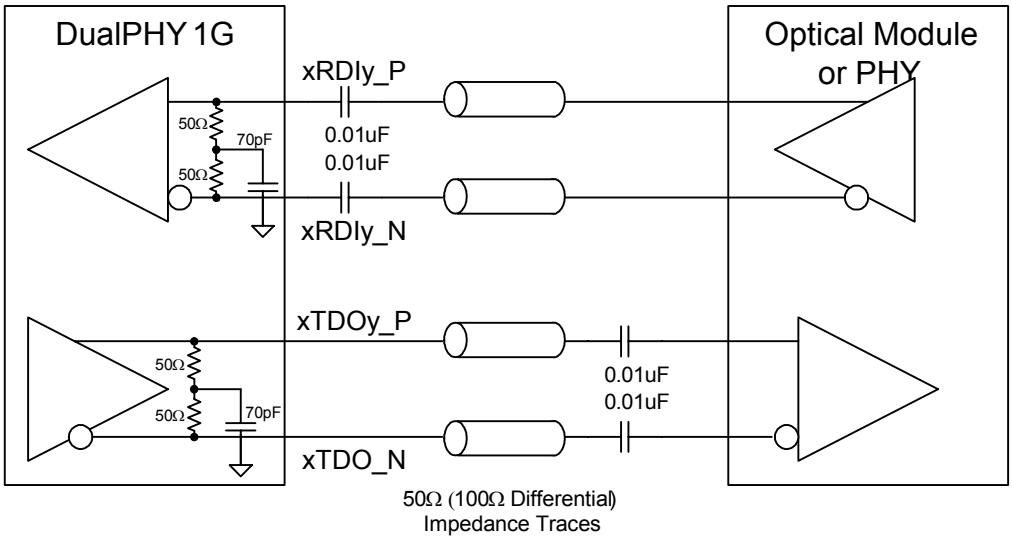
13.3 High-Speed Serial Interface

As shown in Figure 24, the high-speed serial interface is a set of differential drivers and receivers operating over 50 Ω transmission lines. The serial transmit outputs are internally terminated, complementary current-sourcing drivers. The serial receive inputs are differential receivers with internal 100 Ω differential terminations.

For proper operation, all high-speed inputs must be capacitively coupled, as shown in Figure 24. The DualPHY 1G device is internally biased to the proper DC operating point.

The equivalent line length difference between the P and N of the high speed inputs should be less than or equal to 5/16 of an inch (less than 50 ps of skew on FR4 material).

Figure 24 High-Speed Serial Interface



13.4 Clock Requirements

REFCLK is a maximum 125 MHz ±100 ppm, 40/60 or better oscillator. The maximum jitter allowed is 50 ps peak-to-peak, or approx 7 ps rms. REFCLK feeds a 2.5/1.8 V CMOS input. The oscillator requires good power supply rejection to provide a low-jitter clock input to the device. The driving crystal oscillator may be capacitively coupled to REFCLK and biased around the switching threshold of the REFCLK input.

13.5 Hardware/Software Configuration Options

The following table summarizes the relationships between the terminals and registers used to configure the DualPHY 1G device.

Table 22 Hardware/Software Configuration Options

Function	Terminals	Bit Name (Register Bit)	Relationship with S/W-H/W
8B/10B Encode/Decode	DEC_ENC_EN (J2)	INT_DEC_ENC_ENABLE (Reg 0x11, Bit 7)	OR
Parallel Output Enable	POEN (D13)	IPOEN (Reg 0x11, Bit 9)	AND
Code Violation	CV_DIS_EN (J3)	CODE_VIOL_DIS_ENABLE (Reg 0x11, Bit 14)	OR
Device Mode	MODE1, MODE0 (P12, P11)	INT_MODE_SEL [1:0] (Reg 0x11, Bits 5:4)	*
Gigabit Ethernet Mode (no autonegotiation and non-GMII)	GEMOD (C8)	GE_REG (Reg 0x18, Bit 15)	OR
Busy-Bit Mode	BMOD (P9)	BUSY_REG (Reg 0x18, Bit 14)	OR
Serial Loopback	EN_SLPBK (D7)	INT_EN_PRI_SERIAL_LPBK_ [D:A] (Reg 0x16, Bits 15, 13, 11, 9)	OR
Parallel Loopback	ENPLPBK (N3)	EN_PAR_LPBK_[D:A] (Reg 0x16, Bits 7, 5, 3, 1)	OR
Insert/Delete Disable	INS_DEL_DIS (M3)	INS_DEL_DIS (Reg 0x18, Bit 12)	OR

* MDE_CNTRL enables the use of the terminals.

13.6 Analog Considerations

A precision resistor must be connected between the RPRES terminal and ground. It is used as a reference for internal bias circuits. The value of RPRES must be 10kΩ ± 1%.

13.7 JTAG Considerations

A pull-down resister connected to the DualPHY 1G device's TRSTB pin is recommended to assure that the JTAG TAP Controller remains in a reset state during normal operation of the device.

14 Functional Timing

This section outlines the functional timing for the MDC/MDIO serial port. The functional timing for the receive and transmit parallel ports is described in detail in Sections 10.2.3 and 10.2.4.

14.1 MDC/MDIO Interface

The MDC/MDIO interface is a two-wire single-master, multi-slave protocol. The master device sources the clock (MDC) to all slaves. The tri-state data (MDIO) wire is attached to all devices and is used for reading and writing. Figure 25 contains functional timing for an MDC/MDIO write cycle. A 32-bit preamble (PRE) can optionally be skipped if the STA determines that all PHY devices can handle management frames without it.

Figure 25 MDC/MDIO Write Cycle

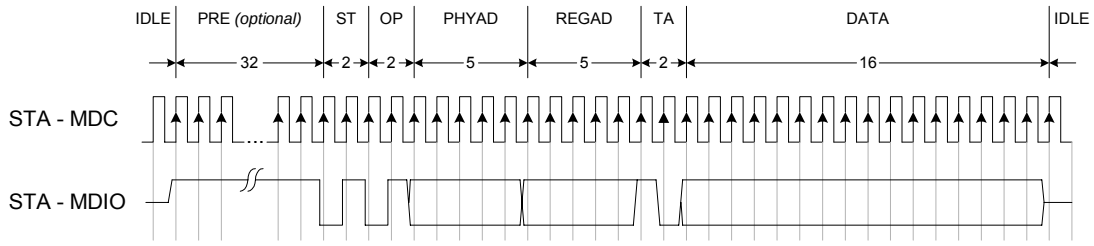
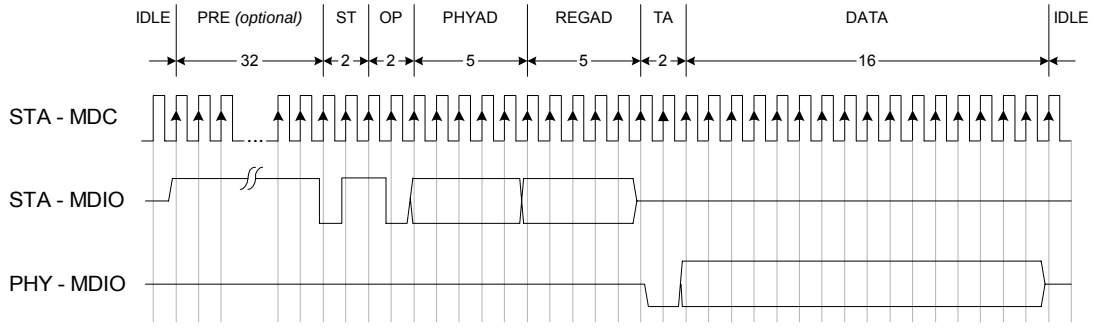


Figure 26 demonstrates an MDC/MDIO read cycle. Again, the 32-bit preamble can be optionally skipped if the STA determines that all the PHY devices can handle management frames without it.

Figure 26 MDC/MDIO Read Cycle



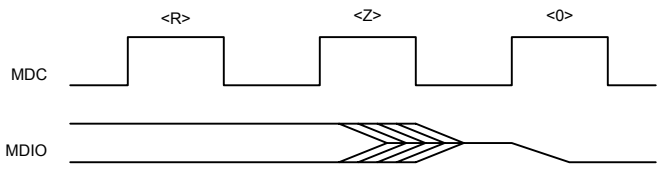
A preamble must be applied to the MDC/MDIO interface whenever an error has occurred during an access. This allows the interface to recover from the error. In the case of a free-running MDC clock, this can be accomplished by having a pause in the interface, since the MDIO pin is pulled-up when not in use.

Notes:

1. IDLE – Idle. The period when data transfer on MDIO is inactive. The MDC clock may stall until the next transfer or continue to run.
2. PRE[31:0] – Preamble. An optional stream of 32 - 1's which assures the receive logic that a transfer is about to occur.
3. ST[1:0] – Start bits. This is always a 0b01.
4. OP[1:0] – Operation Code. A read is an 0b10 and a write is an 0b01.
5. PHYAD[[4:0] – PHY Address. This is the 5 bit address in which this device compares to its internal address.
6. REGAD[4:0] – Register Address. This is the specific register within the selected address.
7. TA[1:0] – Turn Around Cycle. This is a 2 bit time spacing interval which exists to avoid contention on the MDIO net during a read cycle.
8. DATA[15:0] – Data. This is either read data supplied by the slave or write data supplied by the master.

Figure 27 shows how the MDIO signal transitions during the turn around cycles of a read transaction. These turn around cycles are necessary to avoid contention on the MDIO net.

Figure 27 Behavior of MDIO During TA Field of a Read Transaction



15 Absolute Maximum Ratings

Maximum ratings are the worst case limits that the device can withstand without sustaining permanent damage. They are not indicative of normal mode operation conditions.

Table 23 Maximum Ratings

Case Temperature Under Bias	-40 C to +125 C
Storage Temperature	-40 C to +125 C
1.8V Supply Voltage (VDDI)	-0.3 V to +2.20 V
2.5V Supply Voltage (VDDQ)	-0.3 to +3.12 V
Input pad tolerance	-2 V < Vpin < VDDQ +2 V for 10 ns, 100 mA max
Output pad overshoot limits	-2 V < Vpin < VDDQ +2 V for 10 ns, 100 mA max
Voltage on Digital Input or Bidirectional Pin w/VDDQ at 2.5V	-0.3 V to 3.7 V
Voltage on Digital Input or Bidirectional Pin w/VDDQ at 1.8V	-0.3 V to 3.0 V
Voltage on any Digital Output Pin	-0.3 V to V_{DDQ} + 0.3 V
Voltage on any Differential Pin	-0.3 V to V_{DD} + 0.3 V
Static Discharge Voltage	±1000 V
Latch-Up Current	±100 mA
DC Input Current	±20 mA
Lead/Ball Temperature	+225 +0 -5 °C
Absolute Maximum Junction Temperature	+150 °C

16 Power Information

16.1 Power Requirements

Table 24 Power Requirements

Conditions	Parameter	Typ	Power for Thermal Calculations	Max Current	Units
1 Ports Enabled VDDQ = 1.8 V mode 125 Mhz	IDD	176	-	252	mA
	IDDA	59	-	99	mA
	IDDQ (10% data transition density)	61	-	209	mA
	Total Power	**0.5328**	**0.77301**	**-**	**W**
1 Ports Enabled VDDQ = 2.5 V mode 125 Mhz	IDD	176	-	252	mA
	IDDA	59	-	99	mA
	IDDQ (10% data transition density)	100	-	308	mA
	Total Power	**0.673**	**1.00086**	**-**	**W**
2 Ports Enabled VDDQ = 1.8 V mode 125 Mhz	IDD	225	-	318	mA
	IDDA	61	-	102	mA
	IDDQ (50% data transition density)	83	-	213	mA
	Total Power	**0.6642**	**0.9631**	**-**	**W**
2 Ports Enabled VDDQ = 2.5 V mode 125 Mhz	IDD	225	-	318	mA
	IDDA	61	-	102	mA
	IDDQ (50% data transition density)	133	-	310	mA
	Total Power	**0.8473**	**1.1350**	-	W
1 Ports Enabled VDDQ = 1.8 V mode 100 Mhz	IDD	155	-	224	mA
	IDDA	54	-	95	mA
	IDDQ (10% data transition density)	87	-	290	mA
	Total Power	**0.5328**	**0.7995**	**-**	**W**

Conditions	Parameter	Typ	Power for Thermal Calculations	Max Current	Units
1 Ports Enabled VDDQ = 2.5 V mode 100 Mhz	IDD	155	-	224	mA
	IDDA	54	-	95	mA
	IDDQ (10% data transition density)	138	-	421	mA
	Total Power	**0.7212**	**1.1489**	**-**	**W**
2 Ports Enabled VDDQ = 1.8 V mode 100 Mhz	IDD	199	-	283	mA
	IDDA	57	-	98	mA
	IDDQ (50% data transition density)	106	-	242	mA
	Total Power	**0.6516**	**0.7339**	**-**	**W**
2 Ports Enabled VDDQ = 2.5 V mode 100 Mhz	IDD	199	-	283	mA
	IDDA	57	-	98	mA
	IDDQ (50% data transition density)	169	-	395	mA
	Total Power	**0.8833**	**1.0831**	**-**	**W**
1 Ports Enabled VDDQ = 1.8 V mode 93 Mhz	IDD	150	-	218	mA
	IDDA	53	-	88	mA
	IDDQ (10% data transition density)	90	-	351	mA
	Total Power	**0.5274**	**0.8051**	**-**	**W**
1 Ports Enabled VDDQ = 2.5 V mode 93 Mhz	IDD	150	-	218	mA
	IDDA	53	-	88	mA
	IDDQ (10% transition)	138	-	453	mA
	Total Power	**0.7104**	**1.1675**	**-**	**W**
2 Ports Enabled VDDQ = 1.8 V mode 93 Mhz	IDD	192	-	276	mA
	IDDA	56	-	91	mA
	IDDQ (50% data transition density)	111	-	268	mA
	Total Power	**0.6462**	**0.8436**	**-**	**W**

Conditions	Parameter	Typ	Power for Thermal Calculations	Max Current	Units
2 Ports Enabled VDDQ = 2.5 V mode 93 Mhz	IDD	192	-	276	mA
	IDDA	56	-	91	mA
	IDDQ (50% data transition density)	168	-	395	mA
	Total Power	**0.8664**	**1.1462**	**-**	**W**

Note:

1. Outputs loaded with 30 pF (unless otherwise specified), and a normal amount of traffic or signal activity. Power values are calculated using the formula:
   Power = ∑i(VDD x IDD)
   Where i denotes all of the various power supplies on the device, VDD is the voltage for the supply i, and IDD is the current for the supply, i.

16.2 Power Sequencing

Due to ESD protection structures in the pads it is necessary to exercise caution when powering a device up or down. ESD protection devices behave as diodes between power supply pins and from I/O pins to power supply pins. Under extreme conditions, incorrect power sequencing may damage these ESD protection devices or trigger latch up.

The recommended power supply sequencing is as follows:

1. This part does not have any power sequencing restrictions.

16.3 Power Supply Filtering

1. Use a single plane for both digital and analog grounds.

2. Provide separate analog transmit, analog receive, and digital supplies, but otherwise connect the supply voltages together at one point close to the connector where the voltage is brought to the card.

3. Ferrite beads are not advisable in digital switching circuits because inductive spiking (di/dt noise) is introduced into the power rail. Simple RC filtering is probably the best approach provided care is taken to ensure the IR drop in the resistance does not lower the supply voltage below the recommended operating voltage.

16.4 Power Supply Decoupling

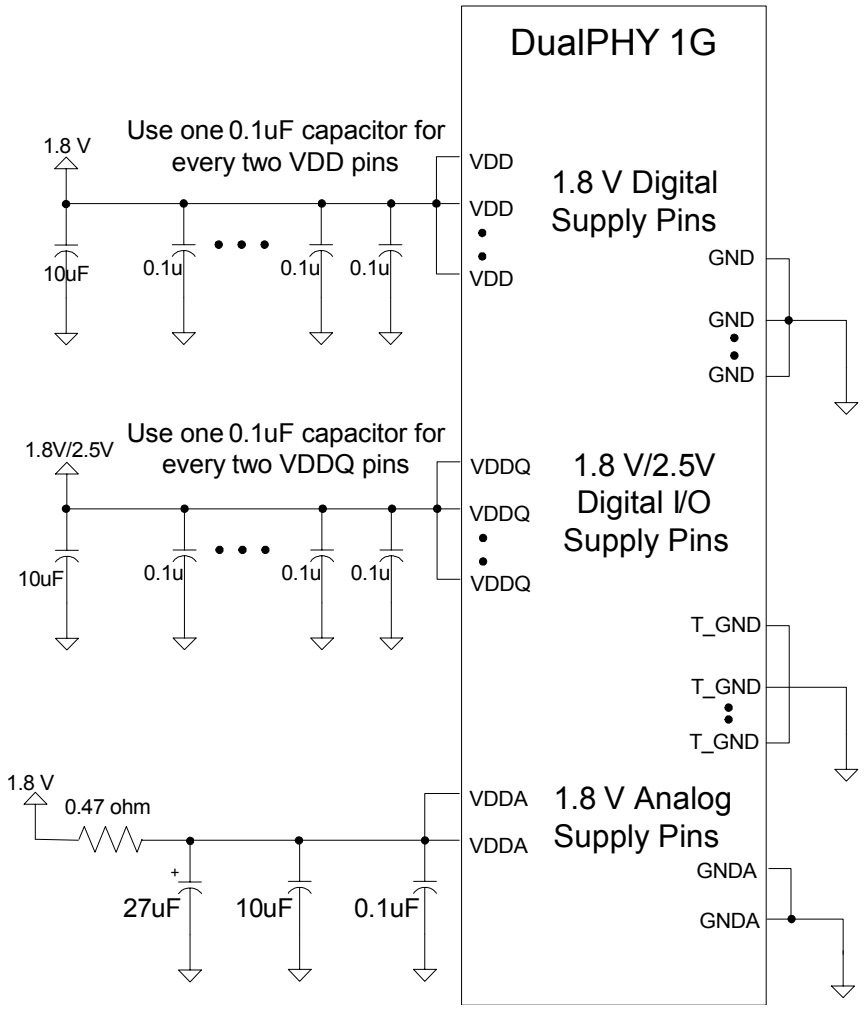
V_{DD} should be decoupled as close to the pins as possible. The recommended decoupling capacitor size is 0402 or 0603. The ground for the capacitors should be a solid ground plane.

One 0.1 µF decoupling capacitor should be used for every two VDD and VDDQ pins

One 10 µF filtering cap should be used on each of the VDD and VDDQ power rails. Taiyo Yuden PN # LMK325BJ106MN or Panasonic PN # ECJ-3YB0J106K are the recommend components.

In order to minimize the intrinsic jitter on the TDO outputs, RC filtering of the VDDA supply voltage is required. The values shown in Figure 28 were chosen to minimize the IR drop on the VDDA supply voltage, yet provide sufficient filtering of power supply noise at low frequencies.

Figure 28 Recommended Power Supply Decoupling



17 D.C. Characteristics

Unless otherwise stated, the following parameters are provided given the following conditions: Ta = -40° C to Tj = 125° C, V_{DD} = 1.8 V ±5%, $V_{DD}Q$ = 1.8 V ±5% or 2.5 V ±5%, $V_{DD}A$ = 1.8 V ±5%

Table 25 D.C. Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Core power supply	1.71	1.80	1.89	V	
V_{DDQ}	I/O power supply VDDQ = 1.8 V VDDQ = 2.5 V	 1.71 2.375	 1.8 2.5	 1.89 2.625	 V	
V_{VDDA}	Analog power supply	1.71	1.80	1.89		
V_{IL}	Input Low Voltage VDDQ = 1.8 V VDDQ = 2.5 V			 0.59 0.87	 V	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage VDDQ = 1.8 V VDDQ = 2.5 V	 1.24 1.63			 V	Guaranteed Input HIGH Voltage (note 6)
V_{OL}	Output or Bidirectional Low Voltage VDDQ = 1.8 V VDDQ = 2.5 V			 0.3 0.4	V	I_{OL} = -1.0 mA all outputs
V_{OH}	Output or Bidirectional High Voltage VDDQ = 1.8 V VDDQ = 2.5 V	 VDDQ – 0.2 VDDQ – 0.3			V	I_{OH} = 0.5 mA all outputs
I_{ILPU}	Input Low Current (pull-up terminals)			50	µA	V_{IL} = 0 V (note 1)
I_{IHPU}	Input High Current (pull-up terminals)			10	µA	$V_{IH} = V_{DDQ}$ (note 1)
I_{ILPD}	Input Low Current (pull-down terminals)			20	µA	V_{IL} = 0 V (note 3)
I_{IHPD}	Input High Current (pull-down terminals)			50	µA	$V_{IH} = V_{DDQ}$ (note 3)
I_{IL}	Input Low Current			100	µA	V_{IL} = 0 V (note 2)
I_{IH}	Input High Current			100	µA	$V_{IH} = V_{DDQ}$ (note 2)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance (parallel interface and control terminals)	—	1.5	—	pF	T_A = 25 C, f = 1 MHz (note 6)
C_{IO}	Output and Bidirectional Capacitance (parallel interface and control terminals)	—	1.8	—	pF	T_A = 25 C, f = 1 MHz (note 5)
C_{INHS}	Input Capacitance (RDI terminals)	—	1.0	—	pF	T_A = 25 C, f = 1 MHz (note 5)
C_{OUTHS}	Output Capacitance	—	1.0	—	pF	T_A = 25 C, f = 1 MHz (note 5)
L_{PIN}	Pin Inductance	—	2.5	—	nH	T_A = 25 C, f = 1 MHz (note 5)

Notes:

1. Input pin or bi-directional pin with internal pull-up resistor.
2. Input pin or bi-directional pin without internal pull-up resistor.
3. Input pin or bi-directional pin with internal pull-down resistor.
4. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).
5. Typical values are given as a design aid. The product is not tested to the typical values given in the data sheet.
6. Input pin is 3.3 V tolerant when VDDQ = 2.5 V.
7. The parallel output data drivers and the clock drivers (RXDx[9:0], RBCx0, RBCx1) have an integrated source series termination. These buffers are designed to drive a 50 Ω unterminated line (maximum recommended length <= 6 inches long).

18 Interface Timing Characteristics

Unless otherwise stated, the following parameters are provided given the following conditions: Ta = -40° C to Tj = 125° C, V_{DD} = 1.8 V ±5%, $V_{DD}Q$ = 1.8 V ±5% or 2.5 V ±5%, $V_{DD}A$ = 1.8 V ±5%

18.1 Reference Clock

Table 26 Reference Clock Timing

Symbol	Description	Min	Typ	Max	Units
REFCLK	REFCLK frequency for 933 Mbit/s operation.	93.2907	–	93.3093	MHz
REFCLK	REFCLK frequency for 1.0 Gbit/s operation.	99.9900	–	100.0100	MHz
REFCLK	REFCLK frequency for 1.25 Gbit/s operation.	124.9875	–	125.0125	MHz
DCrefclk	REFCLK duty cycle	40	–	60	%
Peak to peak jitter on REFCLK	Wideband Peak to peak jitter on REFCLK (10 Hz–20 MHz) (RMS jitter is peak to peak jitter divided by 7) Narrowband peak to peak jitter on REFCLK (12 kHz –20 MHz)	– –	–	50 20	ps
T_r/T_f, Refclk	REFCLK rise/fall time, 10% - 90% (maximum)	–	1000		ps
REFCLK to TXCKy phase deviation	Maximum phase deviation between REFCLK and TXCKy [1]	- 500		500	ps
F_lock	Frequency lock after reset	–		5.0	ms

Note:

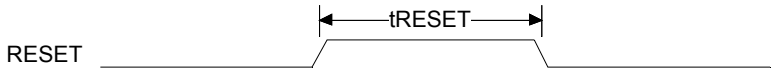
1. The TXCKy and the REFCLK must be synchronous. Once an arbitrary phase relationship is established, the phase deviation must not vary by more than ±500 ps. Should the phase change more than ±500 ps, momentary corruption of data may occur.

18.2 Asynchronous Reset

Table 27 DualPHY 1G Reset Timing

Symbol	Description	Min	Max	Units
t_{RES}	RESET High Pulse Width	500	—	ns
$t_{RESFALL}$	RESET Fall Time	—	10	ns

Figure 29 DualPHY 1G Reset Timing



18.3 MII Management Interface (MDC/MDIO)

Table 28 MDIO Timing

Symbol	Description	Min	Max	Units
f_{MDCMAX}	Clock Frequency (MDC)	0	10	MHz
$t_{MDCHIGH}$	MDC High Pulse Width	45	—	ns
t_{MDCLOW}	MDC Low Pulse Width	45	—	ns
$t_{MDCRISE}$	MDC Rise Time [1]	—	5	ns
$t_{MDCFALL}$	MDC Fall Time [1]	—	5	ns
$t_{MDIORISE}$	MDIO Input Rise Time [1]	—	5	ns
$t_{MDIOFALL}$	MDIO Input Fall Time [1]	—	5	ns
t_{MDIO_S}	MDIO Setup Time	10	—	ns
t_{MDIO_H}	MDIO Hold Time	10	—	ns
t_{pMDIO}	MDC to MDIO valid data	0	10	ns
t_{zMDIO}	MDC to MDIO high-impedence	—	10	ns

Notes:

1. MDC or MDIO rise times and fall times are measure from 10% to 90%.
2. For proper operation at the specified maximum MDC frequency, the MDIO load capacitance must not exceed 470 pf while operating up to 2.5 MHz, and 100 pF while operating up to 10 MHz.

Figure 30 MDIO Timing Diagram

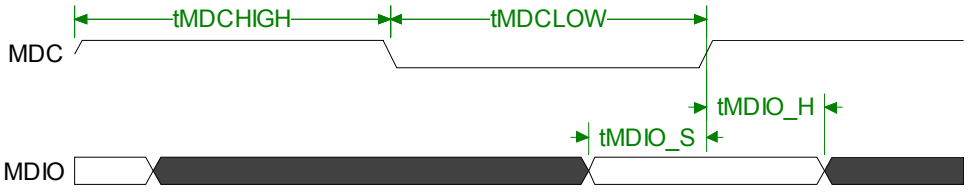
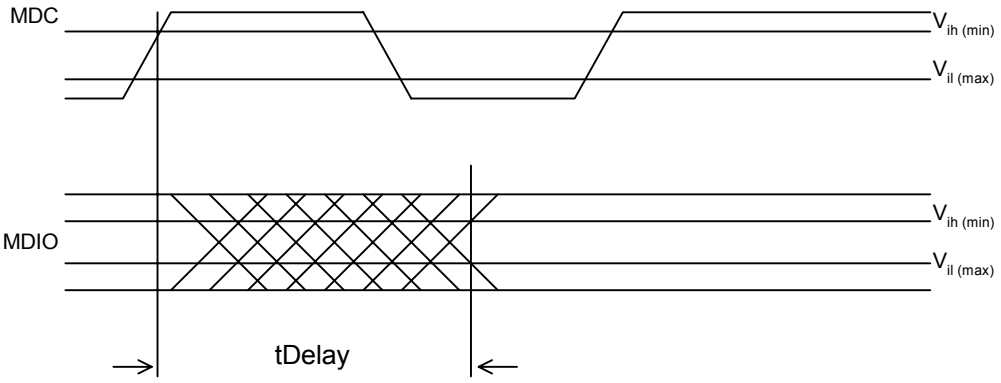


Figure 31 MDIO Sourced by PHY

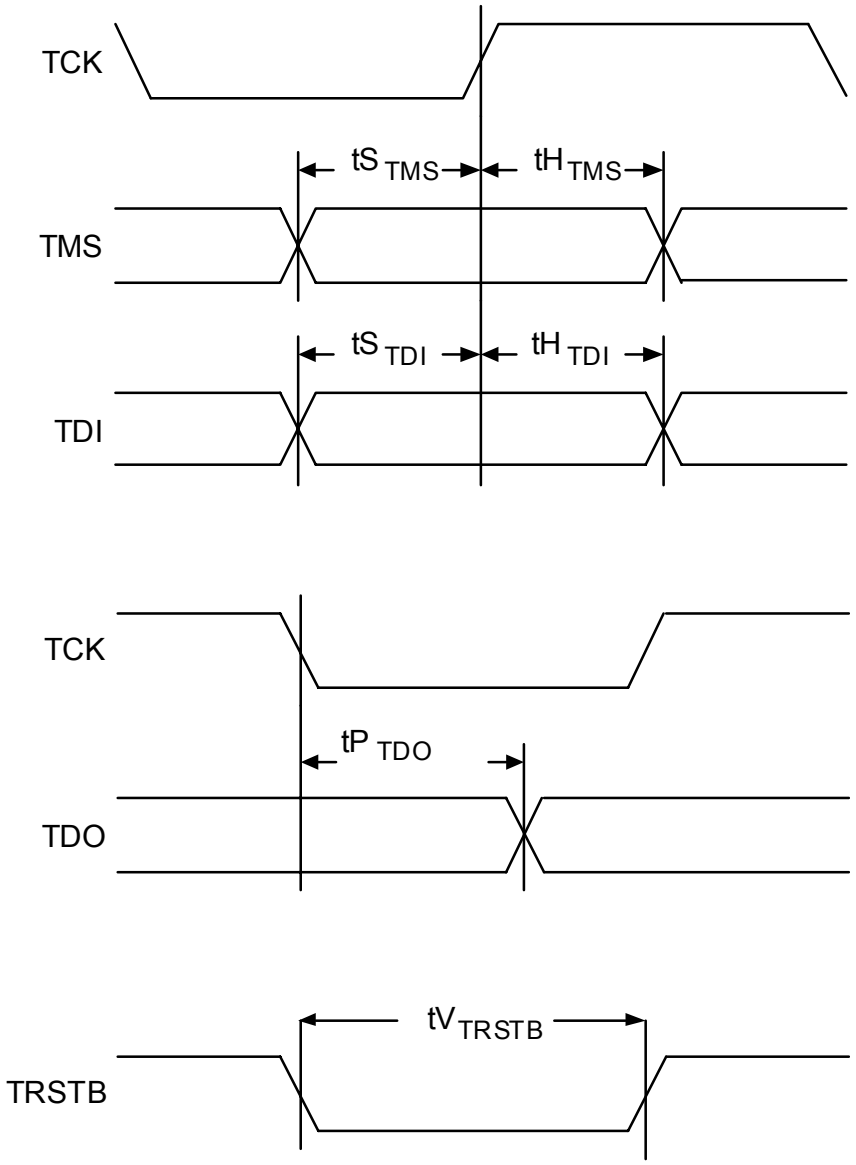


18.4 JTAG

Table 29 JTAG Port Interface

Symbol	Description	Min	Max	Units
—	TCK Frequency	—	1	MHz
—	TCK Duty Cycle	40	60	%
t_{STMS}	TMS Set-up time to TCK	50	—	ns
t_{HTMS}	TMS Hold time to TCK	50	—	ns
t_{STDI}	TDI Set-up time to TCK	50	—	ns
t_{HTDI}	TDI Hold time to TCK	50	—	ns
t_{PTDO}	TCK Low to TDO Valid	2	50	ns
t_{VTRSTB}	TRSTB Pulse Width	100	—	ns
$t_{TRSTBRISE}$	TRSTB Rise Time	—	10	ns

Figure 32 JTAG Port Interface Timing



Notes on Input Timing

1. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the VDD/2 Volt point of the input to the VDD/2 Volt point of the clock.
2. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the $V_{DD}/2$ Volt point of the clock to the $V_{DD}/2$ Volt point of the input.

Notes on Output Timing

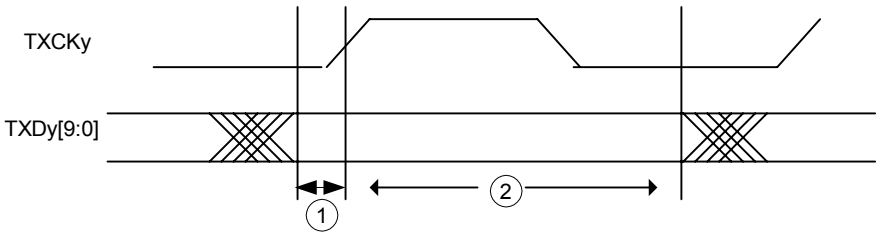
1. Output propagation delay time is the time in nanoseconds from the VDD/2 Volt point of the reference signal to the VDD/2 Volt point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the outputs

18.5 Transmit Timing

Table 30 Transmit Timing

Number	Symbol	Parameter	Min	Typ	Max	Unit
1	t_{TS}	TXD setup time to TXCK (93.3 MHz)	1.4	—	—	ns
		TXD setup time to TXCK (100 MHz)	1.4	—	—	ns
		TXD setup time to TXCK (106 MHz)	1.4	—	—	ns
		TXD setup time to TXCK (125 MHz)	1.4	—	—	ns
2	t_{TH}	TXD hold time from TXCK (93.3 MHz)	0.0	—	—	ns
		TXD hold time from TXCK (100 MHz)	0.0	—	—	ns
		TXD hold time from TXCK (106 MHz)	0.0	—	—	ns
		TXD hold time from TXCK (125 MHz)	0.0	—	—	ns

Figure 33 Parallel Transmit Timing (All Modes)



18.6 Receive Timing

Table 31 Receive Timing

Number	Symbol	Parameter	Min	Typ	Max	Unit
3	t_{RDV}	RXD valid before RBCA, RBCB				
		LRRC Mode (93.3 MHz)	2.5	—	—	ns
		LRRC Mode (100 MHz)	2.5	—	—	ns
		LRRC Mode (106 MHz)	2.5	—	—	ns
		LRRC Mode (125 MHz)	2.5	—	—	ns
		RXD valid before RBC				
		RRRC Mode (93.3 MHz)	2.5	—	—	ns
		RRRC Mode (100 MHz)	2.5	—	—	ns
		RRRC Mode (106 MHz)	2.5	—	—	ns
		RRRC Mode (125 MHz)	2.5	—	—	
4	t_{HRDV}	RXD valid before RBC				
		HRRC Mode (93.3 MHz)	2.5	—	—	ns
		HRRC Mode (100 MHz)	2.5	—	—	ns
		HRRC Mode (106 MHz)	2.5	—	—	ns
		HRRC Mode (125 MHz)	2.5	—	—	ns
5	t_{RDH}	RXD hold after RBCA, RBCB				
		LRRC Mode (93.3 MHz)	0.5	—	—	ns
		LRRC Mode (100 MHz)	0.5	—	—	ns
		LRRC Mode (106 MHz)	0.5	—	—	ns
		LRRC Mode (125 MHz)	0.5	—	—	ns
		RXD hold after RBC				
		RRRC Mode (93.3 MHz)	0.5	—	—	ns
		RRRC Mode (100 MHz)	0.5	—	—	ns
		RRRC Mode (106 MHz)	0.5	—	—	ns
		RRRC Mode (125 MHz)	0.5	—	—	ns
6	t_{HRDH}	RXD hold after RBC				
		HRRC Mode (93.3 MHz)	1.5	—	—	ns
		HRRC Mode (100 MHz)	1.5	—	—	ns
		HRRC Mode (106 MHz)	1.5	—	—	ns
		HRRC Mode (125 MHz)	1.5	—	—	ns
—	t_{RDR}	Output rise time, 10%–90%, 10pF load for RBC[B:A] (Note 9)	—	—	1.0	ns
—	t_{RDF}	Output fall time, 90%–10%, 10pF load for RBC[B:A] (Note 9)	—	—	1.0	ns
—	t_{duty}	Output RBC[B:A] Duty Cycle	40	—	60	%
—	B_sync	Receive data phase-lock time	—	—	500	Bit times

—	t_{RXFTOL}	REFCLK/input data frequency difference	-200	—	200	ppm

Notes:

1. The outputs are 50 ohm source series internally terminated and are designed to drive a 50 ohm unterminated transmission line. The specifications are provided for reference when driving capacitive loads. Capacitive loads should be consistent across all data and clock pins on the Receive interface. PMC-Sierra strongly recommends that all trace lengths be matched on the Receive interface.
2. B_sync has been verified by design. Please refer to Clock and Data Recovery description in section 10.2.4 for conditions which impact B_sync.

Figure 34 Parallel Receive Timing Diagram for LRRC and RRRC Mode

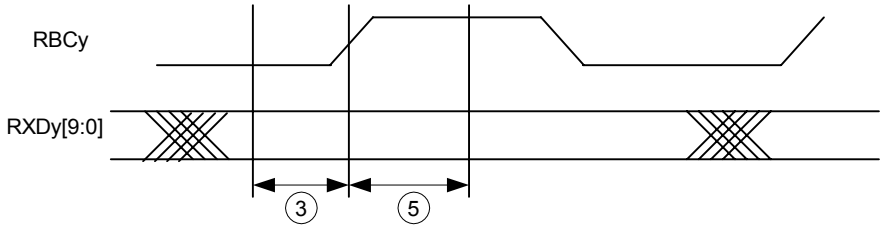
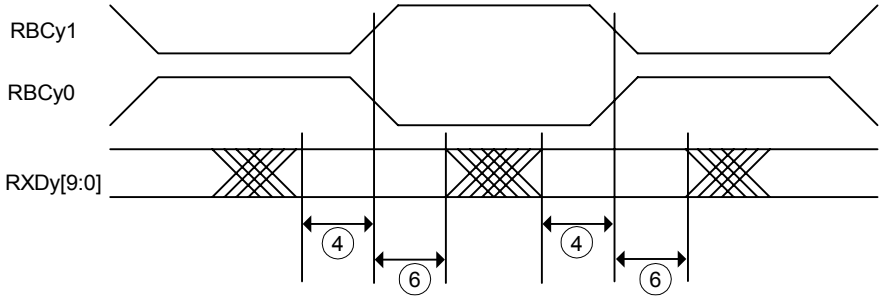


Figure 35 Parallel Receive Timing Diagram for HRRC Mode



18.7 Receive Latency

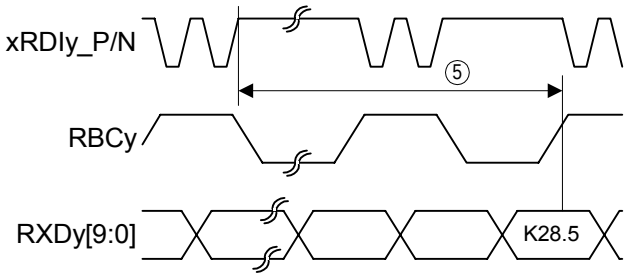
Table 32 Receive Latency Timing

Number	Symbol	Parameter	Min	Typ	Max	Unit
5	t_{RXLAT}	Receiver latency				
		LRRC w/ decoder enabled – PCS off and GEMOD off	105	—	285	Bits
		LRRC w/ decoder enabled – PCS off and GEMOD on	125	—	305	Bits
		LRRC w/ decoder enabled - PCS on	165	—	345	Bits
		LRRC w/ decoder disabled	95	—	275	Bits
		RRRC decoder enabled, PCS off	30	—	50	Bits
		RRRC decoder enabled, PCS on	100	—	120	Bits
		HRRC/RRRC decoder disabled, PCS off	20	—	40	Bits

Note:

1. The receiver latency as shown in Figure 36 is defined as the time between receiving the first serial bit of a word and the clocking out of that parallel word (Defined by the rising edge of REFCLK) when in RRRC Mode. If the FIFO is used, latency may increase.

Figure 36 Receive Latency



18.8 Transmit Latency

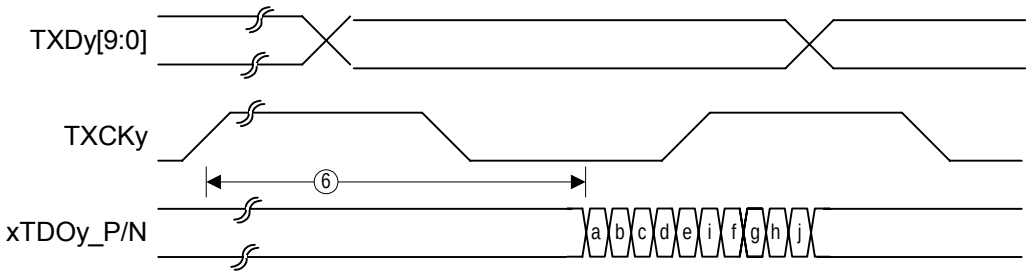
Table 33 Transmit Latency Timing

Number	Symbol	Parameter	Min	Typ	Max	Unit
6	t_{TXLAT}	Transmitter latency[6]				
		- encoder disabled, PCS off	55	—	80	Bits
		- encoder enabled, PCS off	75	—	100	Bits
		- encoder enabled, PCS on	81	—	116	Bits

Note:

1. The transmitter latency, as shown in Figure 37, is defined as the time between the latching in of the parallel data word and the transmission of the first serial bit of that parallel word (defined byte the leading edge of the first bit transmitted.

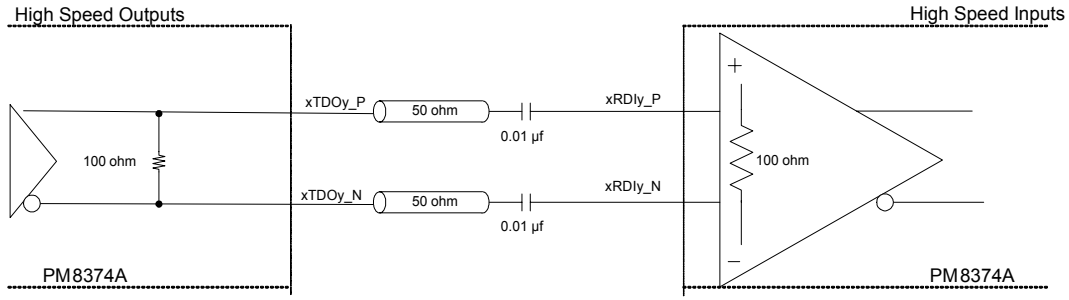
Figure 37 Transmit Latency



[6] independent of operating mode

18.9 High-speed Serial Timing Characteristics

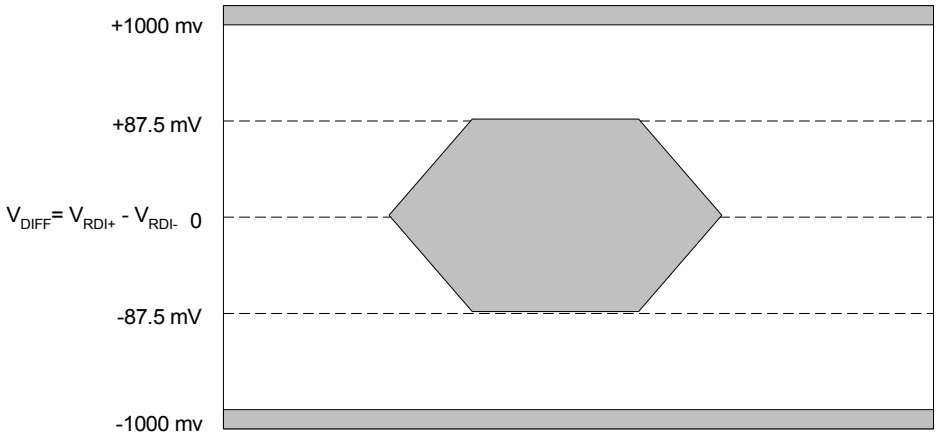
Figure 38 933 Mbit/s to 1.25 Gbit/s Serial I/O Block Diagram



Note:

1. The differential (100 Ω) terminating resistors have been implemented on-chip within the high-speed input buffer and should not be placed on the PC board. The capacitors are DC blocking caps. The TDO and RDI do not have the same common mode bias.

Figure 39 Differential Peak-Peak Receiver Eye Diagram



Note:

1. Minimum differential sensitivity (peak to peak) is 2x the magnitude of the minimum physical potential that can be expected across the differential pair.

V_{DIFF} can be +175 mV for logic 1 or –175 mV for logic 0.

When viewing a data eye on an oscilloscope using a differential probe across terminals A and B, the top and bottom of the eye will have a maximum separation of $V_{diff\ peak\ to\ peak}$. If the same signal is measured using a single ended probe attached to terminal A and referenced to GND, the top and bottom of the eye will have a maximum vertical separation of $|V_{diff}|$. The single ended measurement technique will yield a vertical eye opening equal to ½ the vertical eye opening of the differential measurement technique.

Definitions

Vdiff	Voltage of terminal A – Voltage of terminal B. Vdiff swings both positive and negative in value.
|Vdiff|	The magnitude of Vdiff. Vdiff is always a positive number and represents the maximum voltage that can exist between terminals A and B.
Vdiff peak-to-peak	Represents the peak to peak difference of the differential voltage Vdiff. Vdiff p-p will always be twice the magnitude of the maximum voltage that can exist between terminals A and B.

Table 34 High-speed I/O Characteristics (V_{DD} = 1.8 V)

Symbol	Parameter	Min	Typ.	Max	Unit
$\|V_{RDI+} – V_{RDI-}\|$	High-speed input differential voltage magnitude	87.5	—	1000	mV pk differential
$V_{ID(ppk)}$	High-speed input peak-peak differential voltage	175	—	2000	mV pk – pk differential
$V_{OD(ppk)}$	High-speed output peak-peak differential voltage (High Amplitude Mode)	1070	—	1405	mV pk – pk differential
$V_{OD(ppk)}$	High-speed output peak-peak differential voltage (Low Amplitude Mode)	646	—	839	mV pk – pk differential
t_r, t_f	High-speed output rise and fall times, 20 % – 80 %	100	—	200	ps
t_{SKEW}	Differential Output Skew between high-speed output terminals TDOx_P/_N	—	—	30	ps

Table 35 Gigabit Ethernet Jitter Specifications[2]

T_J	Total output jitter	—	—	0.240	UI pk-pk
T_{DJ}	Deterministic output jitter	—	—	0.100	UI pk-pk
R_{RJT}[1]	Total Jitter Tolerance	—	—	0.749	UI pk-pk
R_{DJT}	Deterministic Jitter Tolerance	—	—	0.462	UI pk-pk

Table 36 Fibre Channel Jitter Specifications[3]

T_J	Total output jitter	—	—	0.21	UI pk-pk
T_{DJ}	Deterministic output jitter	—	—	0.10	UI pk-pk
R_{RJT}	Total Jitter Tolerance	—	—	0.70	UI pk-pk
R_{DJT}	Deterministic Jitter Tolerance	—	—	0.38	UI pk-pk
R_{SJT}	Sinusoidal Jitter Tolerance	—	—	0.10	UI pk-pk

Notes:

1. Total jitter is composed of both deterministic and random components. The allowed random jitter equals the allowed total jitter minus the actual deterministic jitter.
2. The jitter values that are specified in Table 35 assume the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For the Gigabit Ethernet Standard the lower cutoff frequency for jitter is 750 kHz.
3. The jitter values that are specified in Table 36 assume the presence of only high-frequency jitter components that are not tracked by the clock recovery circuit. For the Fibre Channel Standard the lower cutoff frequency for jitter is 637 kHz for 1.0625Gbit/s operation.
4. The Fibre Channel jitter values that are specified in Table 36 are applicable to 933Mbit/s operation.

18.10 Terminal Input Capacitance

Symbol	Parameter	Min	Typ.	Max	Units
Cin	Input capacitance on low-speed input terminals		1		pF

19 Thermal Information

This product is designed to operate over a wide temperature range and is suited for outside plant equipment.

Table 37 Outside Plant Thermal Information

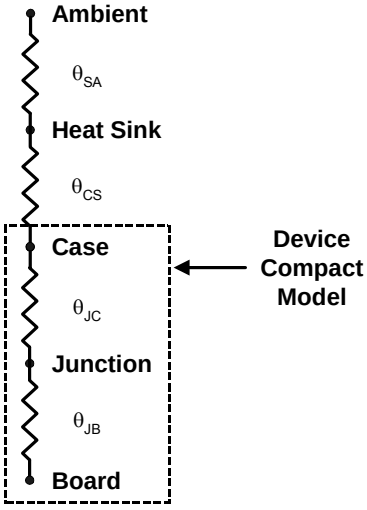
Maximum long-term operating junction temperature (T_J) to ensure adequate long-term life.	105 °C
Maximum junction temperature (T_J) for short-term excursions with guaranteed continued functional performance[2]. This condition will typically be reached when the local ambient temperature reaches 85 °C.	125 °C
Minimum ambient temperature (T_A)	-40 °C

Table 38 Device Compact Model

Junction-to-Case Thermal Resistance, θ_{JC}	7 °C/W
Junction-to-Board Thermal Resistance, θ_{JB}	14.3 °C/W

Table 39 Heat Sink Requirements

θ_{SA}+ θ_{CS}[4]	The sum of θ_{SA} + θ_{CS} must be less than or equal to: $[(105 - T_A) / P_D] - \theta_{JC}$] °C/W where: T_A is the ambient temperature at the heatsink location P_D is the operating power dissipated in the package
θ_{SA} and θ_{CS} are required for long-term operation[5]	



Operating power depends upon the operating mode. Please refer to Table 29 D.C Characteristics to determine operating power..

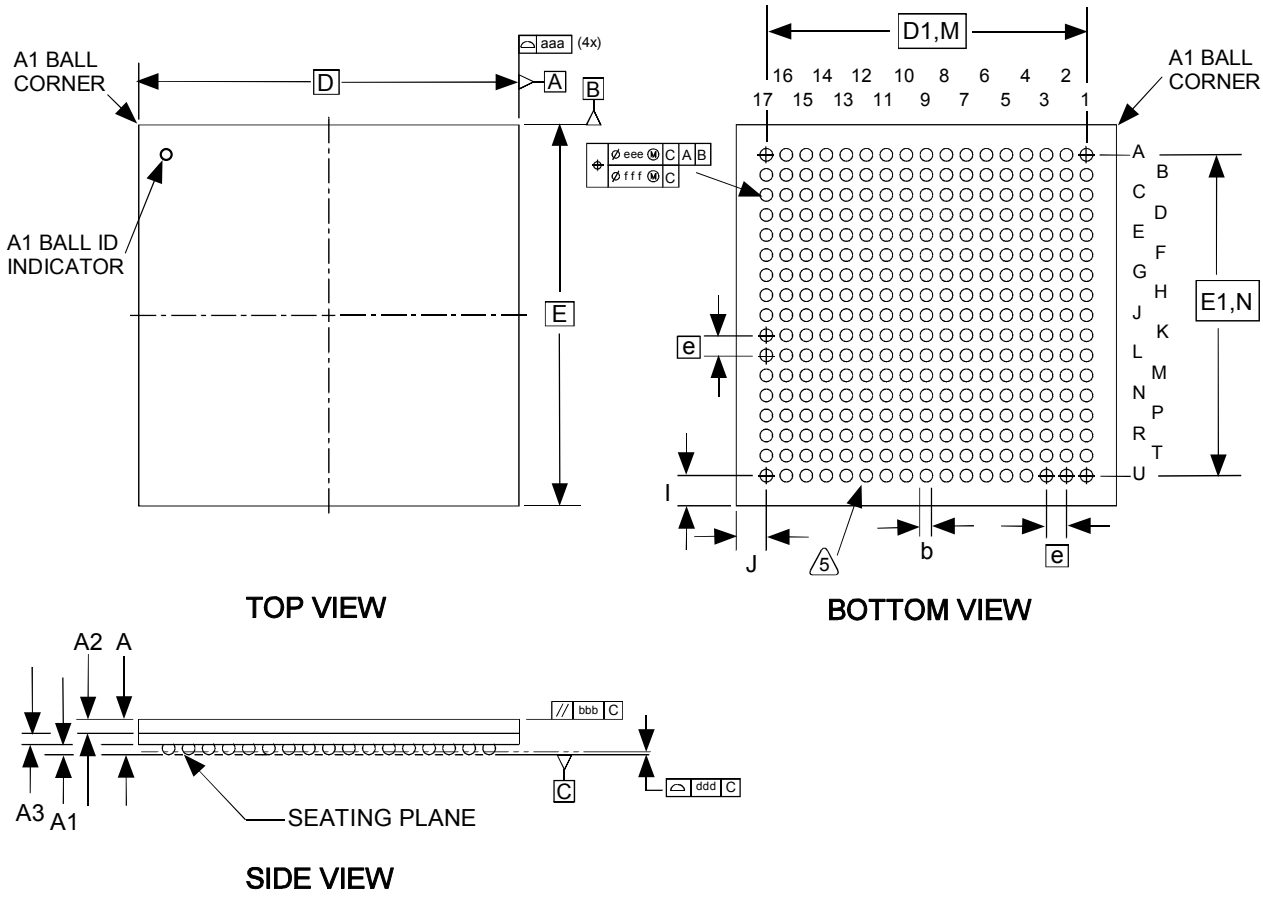
Notes:

1. The minimum ambient temperature requirement for Outside Plant Equipment approximates the minimum ambient temperature requirement for Industrial Equipment
2. Short-term is used as defined in Telcordia Technologies Generic Requirements GR-63-Core
3. The junction-to-case thermal resistance, θJC, is a measured nominal value plus two sigma. The junction-to-board thermal resistance, θJB, is obtained by simulating conditions described in JEDEC Standard JESD 51-8
4. θSA is the thermal resistance of the heat sink to ambient. θCS is the thermal resistance of the heat sink attached material. The maximum θSA required for the airspeed at the location of the device in the system with all components in place.
5. The actual θSA required may vary according to the air speed at the location of the device in the system with all the components in place.

20 Mechanical Information

The DualPHY 1G device is packaged in a 289-pin CABGA Package, as shown in Figure 40. After assembly, the device is tested to meet or exceed a 0.15mm (5.9mil) coplanarity specification.

Figure 40 Mechanical Drawing 289-Pin CABGA



NOTES: 1) ALL DIMENSIONS IN MILLIMETER.
2) DIMENSION aaa DENOTES PACKAGE BODY PROFILE.
3) DIMENSION bbb DENOTES PARALLEL.
4) DIMENSION ddd DENOTES COPLANARITY.
5) SOLDER MASK OPENING 0.40 +/- 0.03 MM DIAMETER (SMD).
6) PACKAGE COMPLIANT TO JEDEC REGISTERED OUTLINE MO-205, VARIATION BD.

PACKAGE TYPE : 289 CHIP ARRAY BALL GRID ARRAY - CABGA																		
BODY SIZE : 19 x 19 x 1.76 MM																		
Dim.	A	A_1	A_2	A_3	D	D_1	E	E_1	M,N	I	J	b	e	aaa	bbb	ddd	eee	f f f
Min.	1.61	0.40	0.65	0.56	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Nom.	1.76	0.50	0.70	0.56	19.00 BSC	16.00 BSC	19.00 BSC	16.00 BSC	17x17	1.50	1.50	0.50	1.00 BSC	-	-	-	-	-
Max.	1.91	0.60	0.75	0.56	-	-	-	-	-	-	-	-	-	0.20	0.25	0.15	0.25	0.10

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