PHAST-12 Device

Programmable, High-Performance ATM, SONET/SDH Terminator for Level 12

TXC-06112

TECHNICAL OVERVIEW

PRODUCT PREVIEW

FEATURES

- Integrated clock recovery and synthesis for four OC-3c/STM-1 signals or one OC-12/OC-12c/ STM-4/STM-4c signal
- OC-12/STM-4 or quad OC-3c/STM-1 framing and performance monitoring
- Expansion port for OC-48/STM-16 operation
- Complete Transport/Section Overhead processing and generation per Bellcore and ITU-T standards
- Complete Path Overhead processing and generation for one STS-12c/STM-4c signal or for four STS-3c/STM-1 signals for ATM/PPP
- VC-4 cross-connect, APS for ATM/PPP payloads using the UTOPIA port(s)
- Cell or frame delineation function for four 155 Mbit/s signals or one (concatenated or unconcatenated) 622 Mbit/s signal
- "PPP" octet stuffing and mapping per RFC1662 and RFC1619 for four 155 Mbit/s signals or one unconcatenated multi-PHY 622 Mbit/s signal or one concatenated single-PHY 622 Mbit/s signal
- One UTOPIA L2+ (cell/frame) 16-bit interface at 50 MHz or two UTOPIA L1 8-bit at 25 MHz
- Quad byte-parallel Telecom Bus at 19.44 MHz
- Access to Line or Section DCC via a port
- Ring port for USHR/P support
- Selectable Intel/Motorola-compatible microprocessor interface
- Boundary scan capability (IEEE 1149.1)
- 0.35 micron CMOS technology
- Single +3.3 V, ±5% power supply
- 5 V tolerant input/output interfaces (except to line)
- Approx. 4.1 W typ. (four 155 Mbit/s interfaces), approx. 3.3 W typ. (one interface at 622 Mbit/s)
- 474-lead ceramic ball grid array package initially
- Plastic ball grid array package in future

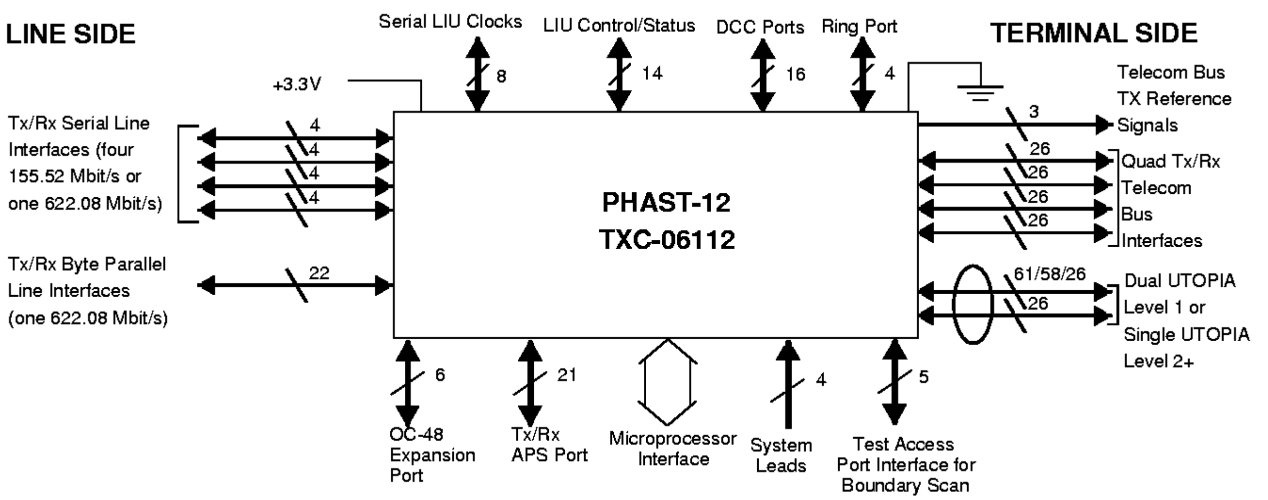
DESCRIPTION

The PHAST-12 is a highly integrated SONET/SDH terminator device designed for ATM cell, frame, higher order multiplexing, and transmission applications. A single PHAST-12 device can terminate four individual STS-3c or STM-1 lines or a single OC-12/12c or STM-4/4c line. Each SONET/SDH terminator has an associated line interface block that performs clock synthesis and clock recovery for four 155.52 Mbit/s signals or single 622.08 Mbit/s serial operation. A parallel line interface port and an expansion port allow four PHAST-12 devices to operate in unison for OC-48/STM-16 applications.

The PHAST-12 can terminate ATM payloads from any of the above signals into either a single 16-bit or 8-bit UTOPIA Level 2 PHY interface, or two 8-bit UTOPIA Level 1 PHY interfaces. PPP payloads are terminated into a 16-bit wide UTOPIA Level 2+ interface. STM (VT/TU) payloads can be terminated into four 8-bit wide Telecom Bus interfaces. When terminating concatenated payloads, the four Telecom Bus interfaces act in concert as a single 32-bit wide Telecom Bus interface. Single-device APS switching or 1:N APS between multiple PHAST-12 devices is also provided for ATM and PPP payloads.

APPLICATIONS

- SONET/SDH add/drop or higher order terminal multiplexers
- Transport of ATM/PPP or VT/TU payloads over SONET/SDH
- Transmission of E1/DS1, E3/DS3 or E4 over SONET/SDH
- ATM switches



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PRODUCT PREVIEW

TABLE OF CONTENTS

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LIST OF FIGURES

PRODUCT PREVIEW

APPLICABLE STANDARDS DOCUMENTATION

Standards documents applicable to the functions of the PHAST-12 device are listed in the table below.

Document No.	Description
I.361	ITU-T, Integrated Services Digital Network (ISDN) - Overall Network Aspects and Functions, (11/95)
I.432.1	ITU-T, B-ISDN User-Network Interface - Physical Layer Specification, (08/96)
G.707	ITU-T, Network Node Interface for the Synchronous Digital Hierarchy, (03/96)
G.781	ITU-T, Structure of Recommendations on Equipment for the Synchronous Digital Hierarchy (SDH), (11/92)
G.782	ITU-T, Types and Characteristics of Synchronous Digital Hierarchy (SDH) Equipment, (01/94)
G.783	ITU-T, Characteristics of Synchronous Digital Hierarchy (SDH) Equipment Functional Blocks, (04/97)
G.803	ITU-T, Architectures of Transport Networks Based on the Synchronous Digital Hierarchy (SDH), (03/93)
GR-253	Bellcore, GR-253-CORE, Synchronous Optical Network (SONET) Transport Systems: Common Generic Criteria, Issue 2, (12/95)
GR-499	Bellcore, GR-499-CORE, Transport Systems Generic Requirements (TSGR): Common Requirements, Issue 1, (December 1995)
TR-NWT-000496	Bellcore, TR-NWT-000496, SONET Add-Drop Multiplex Equipment (SONET ADM) Generic Criteria, Issue 3, (May 1992)
UL1	ATM Forum, UTOPIA - An ATM PHY Interface Specification, Level 1, Version 2.01, (03/94)
UL2v1	ATM Forum, UTOPIA Level 2, Version 1.0, (06/95)
RFC1662	IETF, PPP in HDLC-like Framing, (07/94)
RFC1619	IETF, PPP Over SONET/SDH, (05/94)
T1.105-1995	ANSI, Synchronous Optical Network (SONET) - Basic Description including Multiplex Structure, Rates, and Formats, (1995)
T1X1.5/97-127	ANSI, Contribution to the T1 Standards Project, Enabling Transparency for the PPP over SONET/SDH Mapping, (12/97)
T1X1.5/97-129	ANSI, Contribution to the T1 Standards Project, Scramblers for PPP over SONET/SDH: Consideration and Analysis, (12/97)
ISO13239.2	ISO/IEC, Draft Information Technology - Telecommunications and information exchange between systems - HDLC procedures, (1996)
IEEE 1149.1	IEEE Standard Access Port and Boundary Scan Architecture (1990, supplement a 1993, and supplement b 1994)

PRODUCT PREVIEW

SCOPE

This document provides a technical overview of the TranSwitch PHAST-12 (Programmable, High-performance ATM, SONET/SDH Terminator for Level 12) device, describing its features, capabilities and leading parameters. The primary applications of the PHAST-12 are transport of ATM/PPP payloads over SONET/SDH, higher order muxes, and add/drop muxes.

More detailed information, suitable for designing applications of the PHAST-12 device, will be provided in the device Data Sheet, document number TXC-06112-MB, which is now in preparation.

OVERVIEW

The PHAST-12 is a highly integrated SONET/SDH terminator device designed for transmission, cell, and frame applications. It contains four independent SONET/SDH terminators, which can either terminate ATM/PPP payloads into a UTOPIA Level 2 PHY or Level 2+ interface, or two Level 1 PHY interfaces, or it can interface the SONET/SDH frames to four Telecom Bus interfaces. It is a 3.3 volt device with 5 volt tolerant inputs and outputs for its non-Line Interface signals. Several other interfaces are provided to facilitate DCC channel connection to an external HDLC controller, APS, ring operation, and OC-48/STM-16 operation. The PHAST-12 is being provided initially in a 474-lead ceramic ball grid array package, but a plastic ball grid array package is being planned for future manufacture.

A single PHAST-12 device can terminate four individual STS-3c or STM-1 lines or a single OC-12/12c or STM-4/4c line. Each SONET/SDH terminator has an associated line interface block that performs clock synthesis and clock recovery for four 155.52 Mbit/s serial signals. The first line interface block can also perform clock synthesis and clock recovery for a single 622.08 Mbit/s serial signal. A parallel line interface port and an expansion port allow four PHAST-12 devices to operate in unison for OC-48/STM-16 applications.

The PHAST-12 can terminate ATM payloads from any of the above signals into either a single 16-bit or 8-bit UTOPIA Level 2 PHY interface, or two 8-bit UTOPIA Level 1 PHY interfaces. PPP payloads are terminated into a 16-bit wide UTOPIA Level 2+ interface. STM (VT/TU) payloads can be terminated into four 8-bit wide Telecom Bus interfaces. When terminating concatenated payloads, the four Telecom Bus Interfaces act in concert as a single 32-bit wide Telecom Bus interface. Single-device APS switching or 1:N APS between multiple PHAST-12 devices is also provided for ATM and PPP payloads.

Please see the following Features and Functional Description sections of this document for additional details on the capabilities and internal organization of the PHAST-12 device.

PRODUCT PREVIEW

FEATURES

Reference to the block diagram in Figure 2 will be helpful while reading this section.

LINE INTERFACES

- Four serial line interfaces with differential input/output and integrated clock recovery and synthesis are provided for STM-1/4/4c or STS-3c/STS-12-3c/12c applications.
    - Line Interface #1 can handle 622.08 Mbit/s or 155.52 Mbit/s data rates.
    - Line interfaces #2 - #4 handle 155.52 Mbit/s data rates.
    - Either of two reference clock sources (TTL or differential LPECL) for TX clock synthesis can be selected via a control bit.
- A byte-parallel interface is provided for STM-16/STS-48 multi-device applications as well as byte-parallel STM-4/4c/STS-12-3c/12c single device applications. External byte clock recovery and synthesis are required when using the byte-parallel interface.
    - An active high Lock Detect status input is provided to monitor the external clock recovery circuitry.
    - An Out Of Frame (OOF) control signal is provided for controlling the byte and frame synchronization for an external deserializer device.
    - A frame pulse input is provided to monitor an external deserializer.
    - A reset control output is provided to reset an external clock recovery device via a control bit in the PHAST-12's memory map.
- Additional functions:
    - Four active high status inputs to indicate a low power status from external optical transceivers. Event and interrupt mask bits are provided.
    - Four output control signals under control bit command to control each individual external optical transceiver.
    - Four active high status inputs to monitor external optical transceiver(s) for loss of signal status. Event and interrupt mask bits are provided.

SONET/SDH FRAME HANDLER

- Four SONET/SDH Macros.
    - Individual (up to 4 x) STM-1/STS-3c applications.
    - STS-12-3c/12c or STM-4/4c applications.
- OC-48/STM-16 expansion port is provided for STS-48/STM-16 applications.
    - B1 code transfer to ensure correct B1 byte.
    - B2 error information to ensure correct M1/ Z23 byte processing.
    - AIS indication is also passed.
    - Frame synchronous scrambler is synchronized across the four PHAST-12 devices via the OC-48/STM-16 expansion port.
- Four DCC channel interfaces are provided.
- A Ring Port is provided for Ring Applications where line and path information need to be passed between PHAST-12 devices.
    - Path RDI and FEBE.
    - Line RDI indication and FEBE.

PRODUCT PREVIEW

- Debounced K1 byte.
- Debounced K2 byte and New APS Indication.
- Debounced K3 byte and New K3 byte indication.
- TX Regenerator Section Layer Functions provided by each SONET/SDH macro:
    - All RSOH (Regenerator Section Overhead) bytes are stored in on-chip RAM where they are retrieved for transmission or for access by a microprocessor.
    - Scrambling is performed using a frame synchronous scrambler with polynomial $1+X^6+X^7$.
    - 16-byte SAPI message can be transmitted from the on-chip RAM in the J0 byte position.
    - Alternatively, C1 byte transmission can be performed for STS slot identification purposes.
    - B1 byte calculation is performed.
    - The three TX DCC bytes (D1-D3) can be sourced through external interface via an external HDLC controller or from on-chip RAM.
    - No processing is performed on the RSOH bytes that are reserved for national use or international standardization.
    - B1 calculation for OC-48/STM-16 operation.
- RX Regenerator Section Layer Functions provided by each SONET/SDH macro:
    - All RSOH (Regenerator Section Overhead) bytes are stored in on-chip RAM where they can be observed by a microprocessor.
    - Loss of Signal (LOS) from input leads are reported via event bits with maskable interrupts.
    - OOF condition is detected and then reported via event bits with maskable interrupts.
    - Programmable timers for entering and leaving LOF alarm state.
    - Descrambling is performed using a frame synchronous scrambler with polynomial $1+X^6+X^7$.
    - Check of received SAPI message (J0 bytes) against a programmable on-chip message and report RS-TIM (Regenerator Section Trace Identifier Mismatch) if a mismatch occurs.
    - B1 errors are counted.
    - RX DCC bytes D1 - D3 are stored in on-chip RAM and also provided to an external interface for use by an external HDLC controller.
    - Line AIS is automatically generated within two frames of the detection of LOS or LOF.
    - No processing is performed on the RSOH bytes that are reserved for national use or international standardization.
- TX Multiplex Section Layer Functions provided by each SONET/SDH macro:
    - All MSOH (Multiplex Section Overhead) bytes are stored in on-chip RAM where they are retrieved for transmission or for access by a microprocessor.
    - B2 byte generation is performed.
    - The nine TX DCC bytes (D4 - D12) can be sourced through external interface via an external HDLC controller or from on-chip RAM. Either D4 - D12 or D1 - D3 are available at the interface.
    - MS-RDI generation.
    - MS-RDI can be forced via software control.
    - MS-AIS can be forced via software control.
    - No processing is performed on the MSOH bytes that are reserved for national use or international standardization.
    - MS-REI (M1/Z23 byte) generation.

- RX Multiplex Section Layer Functions provided by each SONET/SDH macro:
  - All RX MSOH (Multiplex Section Overhead) bytes are stored in on-chip RAM where they can be observed by a microprocessor.
  - B2 error counts and B2 block errors are provided in 16-bit counters.
  - Two programmable threshold flags are provided for each B2 error counter: one for signal fail and one for signal degradation interrupts.
  - B2 error counts are turned around as a MS-REI in the TX M1/Z23 byte.
  - MS-AIS detection.
  - MS-RDI detection.
  - RX DCC bytes D4 - D12 are stored in on-chip RAM and can also be provided to an external interface in lieu of the D1 - D3 bytes.
  - Received MS-REI are counted in 16-bit counters.
  - MS-RDI or excessive error defects are translated into MS-RDI in the TX direction within two frames.
  - Persistency check and associated interrupt is provided for RX S1.
  - No processing is performed on the MSOH bytes that are reserved for national use or international standardization.
- TX and RX Multiplex Section Protection Options:
  - Protection for VC-4/C-4
  - For single device operation there is 1:3 multiplex section trail protection.
  - For multi-device operation, 1:N multiplex section trail protection is provided via an external bidirectional APS interface ($N \leq 14$).
  - Integrated 5 x 5 cross connects for TX and RX to facilitate APS.
  - Parity protection on the external APS interface.
- TX and RX Multiplex Section Adaptation Layer Options:
  - For TX ATM/PPP applications the AU-4 pointer offset can be fixed to 0.
  - Optional TX pointer retiming for TX Telecom Bus, ATM or PPP applications.
  - Path AIS can be forced in the TX direction under software control or by an external lead.
  - Outgoing pointer adjustment events and NDF events are counted in 8-bit counters.
  - LOP and Path AIS are detected in the RX direction.
  - Pointer processing is performed per G.783, G.707 and GR-253 standards.
  - AU-4 pointer adjustments are counted in 8-bit counters.
  - NDF events and pointer defect events are counted in 8-bit counters.
- TX/RX Higher Order Path Connection Function Layer Options:
  - Ability to fold back RX VC-4 from any of the four SONET/SDH Frame Handler Macros and assign them to any TX VC-4 via software control. For instance, the RX VC-4 from STM-1 #1 can be folded back and applied to TX VC-4 of STM-1#3. In short, only the logical order of the VC-4 is changed.
  - The higher order path connection function can also be performed under software control at the Transmission Convergence Sublayer Function where only the C-4 s are folded back. This applies only to ATM-PPP Mode.
- TX Higher-Order Path Termination (HPT) Layer Options:
  - The HPT functions are only performed in the ATM/PPP modes of operation.

PRODUCT PREVIEW

- All POH (Path Overhead bytes) are stored in on-chip RAM where they are retrieved for transmission or for access by a microprocessor.
- J1 path trace can be written by the microprocessor into on-chip RAM for transmission.
- B3 calculation is performed.
- C2 bytes can be written to on-chip RAM by a microprocessor for transmission.
- F2, F3, H4, K3, and N1 bytes can be written to the on-chip RAM by a microprocessor for transmission.
- Path FEBE is based on received B3 errors and is automatically inserted into the TX G1 byte.
- Path RDI generation per GR-253 and G.707 standards is performed based on mode (SONET or SDH).
- TX Unequipped condition can be transmitted via software control.

- RX Higher-Order Path Termination Layer Options:
  - The HPT functions are only performed in the ATM/PPP modes of operation.
  - All POH (Path Overhead) bytes are stored in on-chip RAM where they can be observed by a microprocessor.
  - RX 64-byte free form or 16-byte ITU-T G.831 style messages are stored in on-chip RAM.
  - Comparison of microprocessor-written expected 16-byte J1 message against received J1 message is performed. A Trace Identifier Mismatch alarm is raised if no match occurs.
  - 16-bit counters are provided for B3 errors and B3 block errors.
  - Unequipped defect detection is performed on the received C2 bytes.
  - Path Signal Label mismatch detection is performed against a microprocessor-written expected C2 byte and an internal 01 Hex value.
  - 16-bit counter for counting received FEBEs (HP-REI).
  - HP-RDI detection/generation based on GR-253 for SONET payloads or G.707 for SDH payloads.
- TX/RX Lower-order Path Adaptation Functions:
  - In ATM/PPP mode the TX ATM/PPP streams are mapped into a C-4 or C-4-4c and the RX ATM/PPP streams are extracted from the C-4 or C-4-4c.

ATM/PPP HANDLER

- TX ATM Transmission Convergence Sublayer Functions (TCSF):
  - Four individual 155.52 Mbit/s data streams are supported, such as in an STM-4 or four individual STM-1 frames. 4 x STM-1 looks just like 1 x STM-4 to the PHAST-12's ATM/PPP Handler.
  - A single 622.08 Mbit/s stream with a concatenated payload can be handled, such as would be found in an STM-4c frame.
  - Four-cell deep elastic store is provided between UTOPIA Level 1/2/2+ Interface and the TCSF.
  - Idle cells per I.432 or unassigned cells per I.361 are provided towards the MSA Layer when no ATM Cells are available.
  - Generation of Idle/Unassigned cells can be enabled or disabled.
  - Header of Idle/Unassigned Cells can be programmed via on-chip registers.

- Payload of Idle/Unassigned Cells can be programmed such that:
    - each payload byte of a cell is the same value in the range 0-255, and is configured through the microprocessor interface.
    - an incrementing pattern is placed in each payload byte where a specific start value can be defined for each cell or the first cell.
- HEC calculation for Idle/Unassigned or ATM layer Cells can be enabled or disabled.
- HEC can be corrupted under microprocessor control via on-chip mask registers.
- Self-synchronous scrambler of polynomial $1+X^{43}$.
- 24-bit counter is provided to count generated idle/unassigned cells.
- 24-bit counter is provided to count ATM Layer cells read from the elastic store.
- 8-bit counter for counting corrupted ATM Layer cells read from the elastic store.

- RX ATM Transmission Convergence Sublayer Functions (TCSF):
    - Four individual 155.52 Mbit/s data streams are supported, such as in an STM-4 or four individual STM-1 frames. 4 x STM-1 looks just like 1 x STM-4 to the PHAST-12's ATM/PPP Handler.
    - A single 622.08 Mbit/s stream with a concatenated payload can be handled, such as would be found in an STM-4c frame.
    - Four-cell deep elastic store is provided between UTOPIA Level 1/2/2+ Interface and the TCSF.
    - The ATM TCSF are implemented per I.432.
        - ATM cell delineation is performed according to the algorithm in section 4.5.1 of I.432.
            - Programmable ALPHA and DELTA.
            - LOC (Loss of cell delineation) detection is performed.
            - Transmission Path FERF (TP-FERF) is generated in the TX direction when LOC is detected and sustained.
        - Self-synchronizing cell descrambling is performed per section 4.5.3.1 of I.432.
        - ATM cell header check and error detection are performed according to section 4.3 and 4.4 in I.432.
        - Idle or Unassigned cell filter.
        - 16-bit counter is provided for counting HEC errors.
    - 16-bit counter to count ATM Cells that were discarded due to the ATM Cell FIFO being full. When an RX loopback is enabled, no counting is performed.
    - 24-bit counter to count the number of cells forwarded to the ATM cell FIFO.
    - 24-bit counter to count the number of idle cells received from the LPA function.
- PPP Handler Features:
    - Four Independent PPP macros can be used to map PPP into SONET/SDH Frames per RFC1619 and RFC1662.
        - STM-1, STS-3c, STM-4, STS-12, STM-4c and STS-12c applications.
    - Frame interface based on existing UTOPIA 2:
        - Modified 16-bit UTOPIA 2 interface used for Frame Interface.
        - Frames are transferred across modified UTOPIA 2 interface in programmable length chunks.

- SONET/SDH processing as required in RFC1619:
    - TX C2 set to any value between 00 and FF Hex via an on-chip register.
    - TX H4 set to any value between 00 and FF Hex via an on-chip register.
- Mapping:
    - Byte level mapping.
    - Implements byte-stuffing format as in RFC1662 of control characters embedded in payload.
    - Inserts Flag (7E Hex), abort (7D7E Hex), control-escape (7D Hex) and inter-frame fill (7E Hex) as needed.
    - All frames begin and end with 7E Hex.
    - Minimum one or two 7E Hex flags between frames.
    - Separate user-selectable 16/32-bit FCS per RFC1662, no FCS, or transparent mode processing control for TX or RX.
    - Option to directly map/extract chunks directly into/from SONET/SDH frames without any processing (i.e., transparent mode).
- Optional user-selectable scrambler/descrambler ($1+X^{43}$ polynomial).
- Programmable minimum and maximum frame length thresholds.
- Optionally discard frames below minimum frame length threshold.
- Always discard frames that are larger than the maximum frame length threshold.
- In the TX direction, all control octets between the frame delimiting flags are converted to two octets per RFC 1662.
- Per macro programmable address.
- Per macro counters for short frame, long frame, and frames received with Abort character or FCS Error.
- Frame chunks that are transferred across the PPP interface are programmable to be 16, 32, 48, or 64 bytes.

UTOPIA LEVEL 2+ BLOCK

- UTOPIA Interface ATM Functions:
    - PHY Layer with cell level handshaking for ATM applications.
        - two independent UTOPIA Level 1 interfaces, or
        - one UTOPIA Level 2 interface.
    - UTOPIA Level 1 interface parameters:
        - 8-bit data bus.
        - support for a single 155.52 Mbit/s cell stream.
        - 2 - 25 MHz clocking.
    - UTOPIA Level 2 interface parameters:
        - 8 or 16-bit data bus.
        - single or multi-PHY operation.
        - support for up to four 155.52 Mbit/s cell streams (STM-1/4, STS-3c/12) or a single concatenated 622.08 Mbit/s cell stream (STM-4c, STS-12c).
        - polling/selection can be controlled by one or four CLAV signals.
        - 2 - 50 MHz clocking.

PRODUCT PREVIEW

        - four on-chip registers for assigning unique port addresses to each of the ATM/PPP Handler macros.
- UTOPIA Level 2+ Interface PPP Functions:
    - PHY layer with "chunk" level handshaking for PPP applications.
        - one modified UTOPIA Level 2 interface.
    - Modified UTOPIA level 2 interface parameters:
        - 16-bit data bus.
        - single or multi-PHY operation.
        - single-PHY operation is similar to multi-PHY operation, but only one PHY is used.
        - support for up to four 155.52 Mbit/s streams (STM-1/4, STS-3c/12) or a single concatenated 622.08 Mbit/s stream (STM-4c, STS-12c).
        - polling/selection controlled by one multiplexed chunk available signal.
        - 2 - 50 MHz clocking.
        - four on-chip registers for assigning unique port addresses to each of the PPP Handler macros.
        - frames are transferred in programmable size chunks of 16, 32, 48, or 64 bytes.
        - additional handshaking and status signals are provided to indicate start and end of frame, FCS error, abort, last byte of frame is in the most significant byte position, start of chunk.

TELECOM BUS INTERFACE

- TX Telecom Bus Interface:
    - Telecom Bus interface provides four parallel 19.44 MHz interfaces to path terminating and line terminating devices.
        - Each Telecom Bus can support an individual STM-1/STS-3c or all four Telecom Buses can act together as one to support an STM-4c/STS-12c.
    - Handshaking signals for identifying C1 byte, J1 byte, and SPE/VC-4.
    - Parity checking over data only or over data plus control signals. Event bit is provided with an interrupt mask bit for optionally reporting parity errors via an interrupt.
    - Configurable odd or even parity selection.
    - Failure input for forcing TX path AIS generation.
    - POH processing is not performed when the Telecom Bus is being used.
    - Ability to accept VC-4 or AU-4 formatted signals on a per TX Telecom Bus basis:
        - When AU-4 signals are accepted, data from an external device must be aligned to the PHAST-12's framing pulse.
        - When VC-4 signals are accepted, the PHAST-12 performs pointer calculation based on phase differences between the TX Line signal and the TX Telecom Bus signal.
- RX Telecom Bus Interface:
    - Telecom Bus interface provides four parallel 19.44 MHz interfaces to path terminating and line terminating devices.
        - Each Telecom Bus can support an individual STM-1/STS-3c or all four Telecom Buses can act together as one to support an STM-4c/STS-12c.

PRODUCT PREVIEW

- Handshaking signals for identifying C1 byte, J1 byte, and SPE/VC-4.
    - Option to provide A23 byte identifying pulse instead of C1/J1 byte identifying pulses.
- Parity generation over data only or over data plus control signals.
- Failure output for forcing downstream path AIS generation in external device.
- No POH processing is performed when the Telecom Bus is being used.
- Output signal clock edge selection is provided.

MICROPROCESSOR INTERFACE

- Selectable for Motorola 68360 processor bus type interface (QUICC bus type) or Intel-compatible bus interface with the following specifications:
    - Asynchronous interface with maximum clock frequency of 50 MHz.
    - Synchronous interface with maximum clock frequency of 33.3 MHz; the interface runs with the processor clock in this case.
    - Synchronous/asynchronous mode selectable with separate lead.
    - Adaptable to other processor types that allow unlimited wait state insertion.
    - Adaptable to processors that allow only a limited number of wait states with restrictions on internal clock frequencies.
    - Bidirectional data bus width of 8 bits.
    - Address bus width of 14 bits.
    - Control lines: R/W, Device Select, Data Strobe, Data Acknowledge (Ready).
    - Interrupt request capability.
    - Software resets.
    - Memory-mapped device accesses.
    - Watchdog timer for GPP access time-out (programmable period).
    - Interrupt on time-out or handshaking errors.

BOUNDARY SCAN

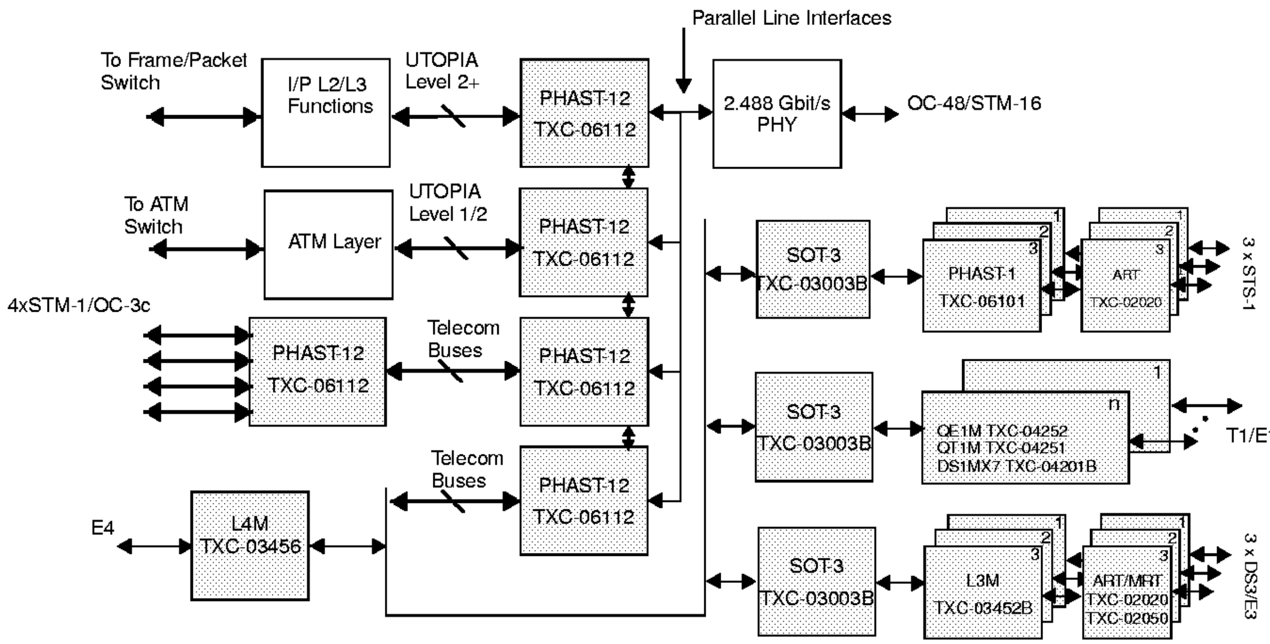
- Boundary scan interface is fully compliant with IEEE Standard 1149.1-1994 (JTAG).

POWER REQUIREMENTS AND PACKAGE INFORMATION

- Separate power supplies for digital and analog sections (3.3 volts ± 5%).
- All input/output signals, with the exception of special LPECL clock leads and analog signal leads, are fully 5.0 volt TTL compatible.
- 474-lead ceramic ball grid array package with direct lid attach feature.
- Ambient air temperature range is -40°C to +85°C (0 ft/min air flow).
- Maximum power dissipation is currently estimated as approximately 4.6 watts in 4 x 155 Mbit/s operation and approximately 3.6 watts in 1 x 622.08 Mbit/s operation.
- Linear airflow at TBD ft/min or more is required for 4 x STS-3c/STM-1 operation above 70°C ambient air temperature.

APPLICATION EXAMPLE

Some example ATM cell, "HDLC-like framing", and transmission applications are shown in Figure 1.



Note: Instead of connecting to the 2.488 Gbit/s PHY device, the serial interfaces of each PHAST-12 device can be connected to a 622 Mbit/s fiber optic transceiver for OC-12/OC-12c/STM-4/STM-4c operation. Alternatively, four 155 Mbit/s fiber optic transceivers can be connected to the line interfaces of each PHAST-12 device for quad OC-3c/STM-1 applications.

Figure 1. Example PHAST-12 TXC-06112 Applications

PRODUCT PREVIEW

FUNCTIONAL DESCRIPTION

A simplified high-level block diagram of the PHAST-12 is shown in Figure 2. It shows the principal blocks that comprise the PHAST-12. These blocks, and other functional units, are listed below:

- Four Line Interface Unit (LIU) blocks
- Four SONET/SDH Frame Handler (SFH) blocks, which consist of the sub-blocks SDB (SONET/SDH Data Buffer) and TX/RX OFP (Overhead Frame Processor). These sub-blocks are not shown In Figure 2.
- Four ATM/PPP Handler (APH) blocks, which consist of the sub-blocks: ACB (ATM Cell / PPP Chunk Buffer) and ACH (ATM Cell Handler / PPP Handler), which performs HDLC-like encapsulation. These sub-blocks are not shown in Figure 2.
- TX/RX APS Cross-Connect (TACC/RACC) block, which is actually a part of the ACH block within the APH. It is shown separately in the block diagram to illustrate its functional relationship to the other blocks.
- UTOPIA Interface block, which contains the ACI sub-block
- TX/RX Telecom Bus Interface block
- TX/RX DCC Port (included in SFH block)
- Microprocessor Interface
- TX/RX Ring Port (included in SFH block)
- OC-48/STM-16 Expansion Port (included in SFH block)
- Boundary Scan Port

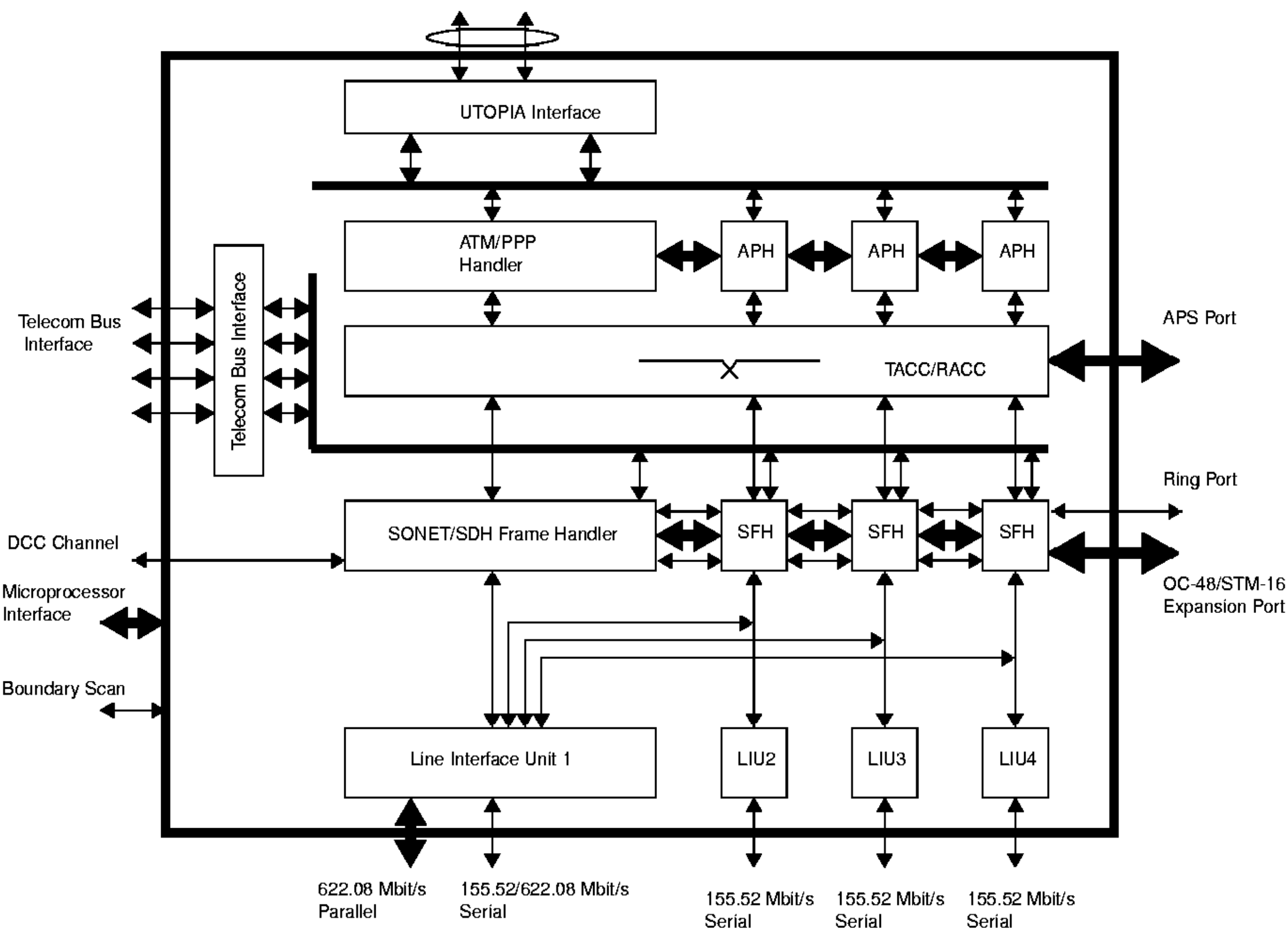


Figure 2. PHAST-12 TXC-06112 Block Diagram

PRODUCT PREVIEW

The PHAST-12 can extract ATM/PPP traffic from up to four individual STM-1/STS-3c streams or a single STM-4/4c or STS-12/12c stream and supply them to its RX UTOPIA Level 2 or Level 2+ interface. Conversely, the PHAST-12 can accept ATM/PPP traffic on its TX UTOPIA Level 2 or Level 2+ interface and map the ATM/PPP streams into up to four individual STM-1/STS-3c streams or a single STM-4/4c or STS-12/12c. Other payloads can be handled via the TX and RX Telecom Bus Interfaces.

The four SONET/SDH terminators can be configured for operation as either:

- four individual terminators for STM-1 or STS-3c applications
- a 4:1 Mux/Demux for STM-4 or STS-12 applications
- a single STM-4c or STS-12c terminator
- An STM-16/STS-48 interface where four PHAST-12 devices are connected in parallel. An external mux/demux device is required for this function.

Each SONET/SDH terminator has a Line Interface Unit (LIU) block associated with it that performs clock synthesis and clock recovery for 155.52 Mbit/s serial operation. The first Line Interface Unit block can also perform clock synthesis and clock recovery for 622.08 Mbit/s serial operation. When STM-16/OC-48 operation is enabled, the external mux/demux is required to perform the clock recovery/synthesis. In this case the 8-bit parallel SONET/SDH Line Interface will be used at 77.76 MHz.

The Line Interfaces are connected to corresponding SONET/SDH Frame Handler (SFH) blocks. These blocks provide the Regenerator Section Overhead (RSOH) and Multiplex Section Overhead (MSOH) functions, i.e. TOH functions. All RX and TX RSOH, MSOH, and Path Overhead (POH) bytes are stored in the on-chip RAM from where they can be observed/transmitted and also accessed via the microprocessor interface. The four SONET/SDH Frame Handler blocks can operate independently for STM-1/STS-3c applications or can operate together for STM-4/STS-12[1] or STM-4c/STS-12c applications. For STM-16/STS-48 applications, an OC-48/STM-16 Expansion Port is provided for synchronizing operation between multiple PHAST-12 devices. Four individual interfaces are provided for each DCC channel (regenerator or multiplex section) for connection to an external HDLC controller. The DCC bytes can optionally be inserted via the microprocessor interface. A Ring Port is provided that is used to communicate Line FEBE and RDI, K1 and K2 bytes plus associated alarms (and, when ATM or PPP processing is performed, K3 byte and associated indications as well as path FEBE and RDI information) between PHAST-12 devices. The SONET/SDH Frame Handlers can interface to either the external Telecom Bus Interfaces or the ATM/PPP blocks.

The PHAST-12 has four individual and independent Telecom Bus Interfaces which provide an alternative interface to the UTOPIA Level 2+ style interface. The Telecom Bus Interface is a byte-wide interface with control signals for identification of the VC-4 and TOH time slots as well as the location of the J0 and J1 bytes. There is one Telecom Bus Interface associated with each SONET/SDH Frame Handler. However, as is the case with the SONET/SDH Frame Handlers, the four Telecom Bus Interfaces can operate in concert with each other as one 32-bit wide Telecom Bus Interface when STM-4c/STS-12c frames are being processed. The PHAST-12 is not restricted to ATM or PPP in "HDLC-like framing" payloads due to the general nature of the Telecom Bus Interface. However, when the Telecom Bus Interface is used, the PHAST-12 does not provide POH processing. TX Retiming is programmable on a per Telecom Bus basis. RX retiming is not available. For devices where TX retiming is not used, a reference clock and frame signal are provided by the PHAST-12 to be used by external devices that are supplying data to the TX Telecom Bus Interfaces. Failure input and outputs are provided for

1. Already for STM-4 operation, the OFPs have to jointly calculate the B1 and perform frame scrambling over the entire frame. STM-4c, in addition, requires joint B3 calculation, etc.

PRODUCT PREVIEW

each Telecom Bus Interface. In the RX direction these leads signal to a downstream device that conditions for generating Path AIS have been detected by the PHAST-12. In the TX direction these leads signal to the PHAST-12 to generate Path AIS in the transmit direction.

There are four individual ATM/PPP Handler blocks. These process the ATM/PPP data and interface to the TX APS Cross Connect (TACC) and RX APS Cross Connect (RACC) blocks. When processing ATM Cells or PPP data, each ATM/PPP block provides a four-cell deep FIFO for clock separation in each direction. Cell rate decoupling is also performed where idle or unassigned cells can be generated. The header and payload bytes of the idle or unassigned cells in the TX direction can be programmed via the microprocessor interface. A $1+X^{43}$ polynomial payload scrambler/descrambler function can be enabled via a global control bit for PPP operation. The scrambler/descrambler is always activated when ATM processing is performed.

When the ATM/PPP Handler blocks are processing PPP data they perform octet stuffing of flag characters (7E Hex) and control escape characters (7D Hex) in the TX direction, and in the RX direction all control escape characters are destuffed. These blocks can optionally perform 16- or 32-bit FCS generation/calculations as selected via global control bits. Frame delimiting and inter-frame flag fill are provided in the transmit direction. An optional $1+X^{43}$ polynomial scrambler/descrambler function can be enabled via a global control bit. Also a Transparent Mode of operation is possible, for applications where the PPP in "HDLC-like framing" processing is performed external to the PHAST-12. Registers for programming maximum and minimum allowable received frame lengths are provided. Received frames that exceed the maximum programmed frame length are always discarded. Received frames that are below the minimum programmed frame length may optionally be discarded.

The ATM/PPP Handlers can work individually or in concert with each other depending upon the type of payload being processed. If four individual STM-1/STS-3c frames are being processed, such as in the case of STM-4/STS-12 or four individual 155 Mbit/s streams, then the ATM/PPP blocks work individually. If a STM-4c/STS-12c is being processed, then all four ATM/PPP blocks work in parallel. The ATM/PPP blocks Interface to the TACC and RACC (TX and RX APS Cross Connect) blocks.

APS functions are facilitated via an APS interface and the TACC/RACC blocks. These blocks consist of two 5 x 5 cross-connects and two bidirectional APS interfaces, one for TX and one for RX. The 5 x 5 cross connects handle the data from the four RX/TX macros plus the RX/TX APS interface. If a single PHAST-12 is used, 1:1, 1:2, and 1:3 APS is supported. If more than one PHAST-12 is used, such as in a multiple STM-1/STS-3c situation, a 1:N (N = 1 - 14) protection scheme can be achieved, provided that the two bidirectional APS interfaces are used. The APS function is not available when the Telecom Bus Interface is used, or when concatenated payloads such as AU-4-4c are being processed.

The UTOPIA Level 2+ block interfaces to the four ATM/PPP Handler macros. ATM cells and PPP in "HDLC-like framing" are handled by this block. For ATM cells the UTOPIA Level 2+ block can provide either two 8-bit TX/RX UTOPIA Level 1 PHY interfaces, or a 16-bit TX/RX UTOPIA Level 2 PHY interface. Only cell level handshaking is provided. For UTOPIA Level 2+ MPHY operation, 5-bit address registers allow addresses to be assigned to the four individual ATM/PPP Handler macros. For PPP operation, the UTOPIA Level 2+ interface is used with some additional handshaking signals to provide a 16-bit MPHY interface for passing PPP data in the form of programmable-size chunks. Chunk sizes can be programmed to be either 16, 32, 48, or 64 bytes in length. Indications for aborted frames and FCS errors are also provided. As is the case for ATM operation, 5-bit address registers allow addresses to be assigned to the four individual ATM/PPP Handler macros. The UTO-

PIA Level 1 interfaces can be operated at frequencies up to 25 MHz, while the UTOPIA Level 2 interface can be operated up to 50 MHz.

Two loopbacks are supported in the TX direction and one is supported in the RX direction for ATM/PPP payloads. All of the loopbacks occur at the TCS (Transmission Convergence Sublayer) Function Boundaries of the ATM/PPP Handler. The first TX loopback is at the ATM Cell Buffer (ACB) interface with the ATM/PPP Handler. As soon as the ACB is not empty, the ACB contents are read and provided to the RX direction. The second TX loopback is at the output of the ATM/PPP Handler before the SONET/SDH Frame Handler. The TX cell stream at the output of the ATM/PPP Handler is looped back to the RX side of the ATM/PPP Handler. This cell stream can contain idle/unassigned cells. Each of the TX loopbacks has two modes. With the first mode, just the loopback is performed and data is not forwarded to the next processing step in addition to being looped back. The second loopback mode allows data to be forwarded to the next processing step. The RX loopback causes RX data provided by the SONET/SDH Frame Handler to be looped back towards the TX direction. There are two modes for the RX loopbacks, one for loopback only (i.e., no data is passed to the ATM/PPP Handlers), and one where data is also passed to the ATM/PPP Handler.

The PHAST-12 provides a microprocessor interface that can be selected to be compatible with the Motorola 68360 processor bus type interface (QUICC bus type), or the Intel style bus. The interface can be selected to be either synchronous or asynchronous. The synchronous interface can be run with a maximum clock frequency of 33.3 MHz, while the asynchronous interface can be run with a 50 MHz clock. Polling or interrupt support, and latching of critical events, are provided to accelerate interrupt processing and reduce the burden on the microprocessor. Alarm masks are provided to enable or disable interrupts. Overflow and programmable threshold interrupts are provided on certain counters. An integrated watchdog timer is provided with a programmable period to force microprocessor accesses to terminate when a timeout occurs. Access to the various configuration registers, counters, and the control and status registers is provided via this microprocessor interface.

There are many features included in the PHAST-12 device that make it well suited for higher order multiplex applications. The integrated APS Cross Connect Circuit reduces external part counts. In STS-48/STM-16 applications the PHAST-12 can support multiplexing of STM-4, STM-4c, STS-12, or STS-12c frames. Telecom Bus, Dual UTOPIA Level 1 and UTOPIA Level 2 interfaces add a high degree of flexibility for connecting to ATM or PPP terminating/switching equipment or other path terminating equipment. On-chip clock recovery and synthesis for the serial 155 Mbit/s or 622 Mbit/s interfaces eliminates the need for additional external clock recovery circuitry. The high degree of integration of complex functional blocks into a single chip with glueless chip-to-chip communication for multi-chip applications makes possible reduced design and debug time and shorter time to market.

The Boundary Scan Port includes a five-lead TAP (Test Access Port) that conforms to the IEEE 1149.1-1994 standard. This TAP provides external boundary scan to read and write the PHAST-12 input and output leads from the TAP for circuit board and component testing.

SELECTED PARAMETER VALUES

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply Voltage	V_{DD},V_{DD2}	3.0	3.6	V	Notes 1,4
Input Voltage (LVTTL)	V_{IN1}	-0.6	5.5	V	Notes 1,3
Input Voltage (LPECL/PPECL)	V_{IN2}	0.0	V_{DD}	V	Note 1
Storage Temperature	T_S	-40	125	^oC	Note 1
Ambient operating temperature range	T_A	-40	85	^oC	0 ft/min linear airflow
Component temperature x time	TI		240 x 60	^oC x s	Notes 1,5
Moisture Exposure level	ME		2	Level	JEDEC A112 Level 2
Relative Humidity, during assembly	RH	5	60	%	up to 1 year (JEDEC A112 level 2) Note 2
Relative Humidity, in-circuit	RH	8	80	%	non-condensing
Relative Humidity, shipment		--	--	%	Note 6
ESD Classification	ESD		3	kV	JEDEC Class 2

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the “CAUTION” label on the drypack bag in which devices are supplied.
3. For this parameter maximum value applies to overshoot, minimum value applies to undershoot.
4. Precautions have to be taken on the card to apply V_{DD} and V_{DD2} simultaneously.
5. This is the maximum temperature and the duration that this maximum temperature can be applied to the PHAST-12 device during solder reflow on a printed circuit board before the PHAST-12 device is damaged. See also the Temperature Limitations / Card Processing section below.
6. Drypack required for shipment.

PRODUCT PREVIEW

TEMPERATURE LIMITATIONS / CARD PROCESSING

The following limitations apply to CBGA-DLA packages:

1. Maximum number of thermal cycles above a particular temperature are cumulative (that is, 1 cycle above 250 °C is also 1 cycle above 220 °C). Five reflow cycles are designated to card processing.
2. The temperature profile limitations during card assembly and rework reflow operations are:

a. Maximum temperature: 260 °C (for one reflow only)

b. Maximum time above 250 °C: 30 seconds (for one reflow only)

c. Maximum temperature for reflows post one 260 °C reflow: 240 °C

d. Maximum time above 220 °C: 60 seconds/cycle (5 cycles maximum)

e. Maximum time above 183 °C: 240 seconds/cycle (5 cycles maximum)

3. Double-sided two-pass assembly is permitted subject to the maximum thermal reflow count.
4. Double-sided two-pass assembly where the second pass is wave solder does not count as a reflow, provided thermal exposure is less than 183 °C.

THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance - junction to ambient	θ_{JA}		9.1	11.6	°C/W	0 ft/min linear airflow

POWER REQUIREMENTS

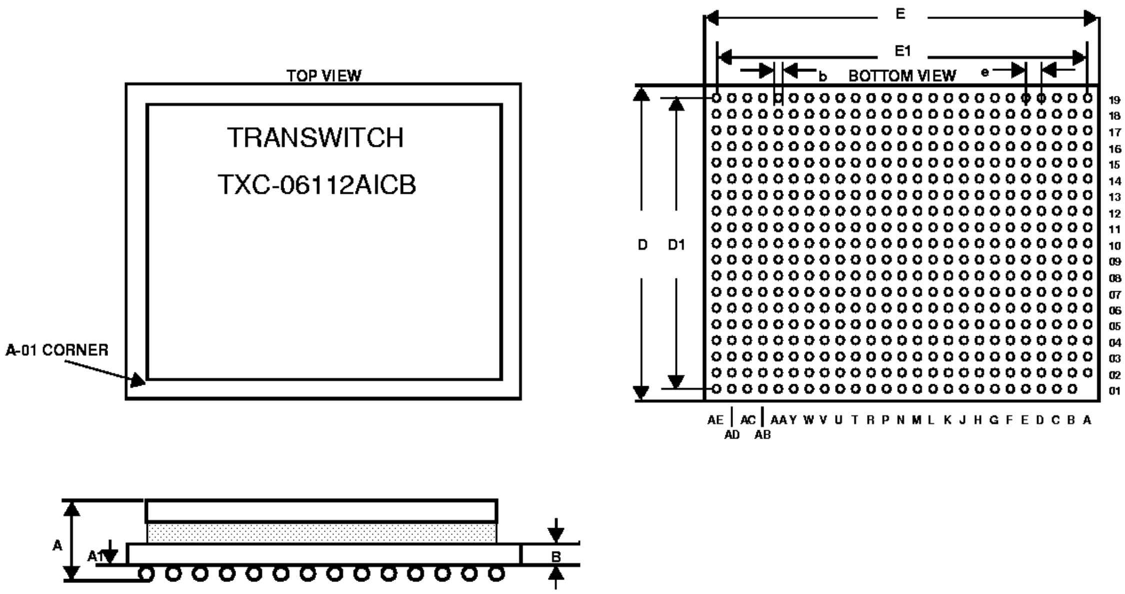
Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	3.15	3.30	3.45	V
Supply Current - 4x STS-3c/STM-1	I_{DD}		1.24	1.33	A
Power Dissipation - 4x STS-3c/STM-1 (see Note 1)	P_{DD}		4.1	4.6	W
Supply Current - STS-12/STS-12c/STM-4/STM-4c	I_{DD}		1.0	1.06	A
Power Dissipation - STS-12/STS-12c/STM-4/STM-4c	P_{DD}		3.3	3.6	W

Note 1:
Linear airflow at TBD ft/min or more is required for 4 x STS-3c/STM-1 operation above 70 °C ambient air temperature.

PRODUCT PREVIEW

PACKAGE INFORMATION

The PHAST-12 device is packaged in a 474-lead Ceramic Ball Grid Array package with Direct Lid Attach (CBGA -DLA) that is suitable for surface mounting, as illustrated in Figure 3 below.



Dimension (Note 1)	Min	Max
A	5.18	5.90
A1	0.80	1.00
B	1.62	1.98
b (nom.)	0.89	
D	24.80	25.20
D1 (nom.)	22.86	
E	32.30	32.70
E1 (nom.)	30.48	
e (nom.)	1.27	

Notes:
1. All dimensions are in millimeters. Values shown are for reference only.
2. Size of array: 19 x 25.
3. Diagram is stylized and not to scale.

Figure 3. PHAST-12 TXC-06112 474-Lead Ceramic Ball Grid Array - Direct Lid Attach Package

ORDERING INFORMATION

Part Number: TXC-06112AICB 474-lead Ceramic Ball Grid Array package with Direct Lid Attach

RELATED PRODUCTS

TXC-02020, ART VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ART performs the transmit and receive line interface functions required for transmission of STS-1 (51.840 Mbit/s) and DS3 (44.736 Mbit/s) signals across a coaxial interface.

TXC-02021, ARTE VLSI Device (Advanced STS-1/DS3 Receiver/Transmitter). ARTE has the same functionality as ART, plus extended features.

TXC-02050, MRT Multi-Rate Line Interface VLSI Device. The MRT provides the functions for terminating ITU-specified 8448 kbit/s (E2) and 34368 kbit/s (E3) line rate signals, or 6312 kbit/s (JT2) line signals specified in the Japanese NTT Technical Reference for High Speed Digital Leased Circuits. An optional HDB3 codec is provided for the two ITU line rates.

TXC-03003, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line and path overhead processing for STM-1/STS-3/STS-3c signals. Compliant with ANSI and ITU-T standards. Not recommended for new designs, use TXC-03003B.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This is a dual-mode device, which can be configured either to emulate the TXC-03003 device or to provide additional capabilities.

TXC-03452 and TXC-03452B, L3M VLSI Device (Level 3 Mapper/Desynchronizer) - L3M maps a DS3 or E3 signal into an SDH/SONET signal formatted for STM-n (VC-3 via TU-3) or STS-n (via STS-1 SPE). The TXC-03452B should be used in new designs instead of the TXC-03452.

TXC-03456 L4M VLSI Device (Level 4 Mapper/Desynchronizer) - L4M Maps a 139.264 Mbit/s asynchronous line signal into an AU-4 VC-4/STS-3c SPE signal. The SONET/SDH signal is transmitted via the add bus with timing derived from the drop bus, add bus or an external source. The L4M provides test features such as line loopback, SONET/SDH loopback and on-chip test pattern generator and analyzer. The L4M meets strict jitter requirements to transport broadcast grade video signals.

TXC-04201 and TXC-04201B, DS1MX7 VLSI Device (DS1 Mapper 7-Channel). The DS1MX7 maps seven DS1 signals into any seven selected asynchronous or byte-synchronous mode VT1.5 or TU-11 tributaries in a SONET/SDH synchronous payload envelope.

TXC-04251, QT1M VLSI Device (Quad DS1 to VT1.5 or TU-11 Async Mapper-Desync). Interconnects four DS1 signals with any four asynchronous mode VT1.5 or TU-11 tributaries carried in SONET STS-1 or SDH AU-3 rate payload interface.

TXC-04252, QE1M VLSI Device (Quad E1 to AU-4/VT2 or TU-12 Async Mapper-Desync). Interconnects four E1 signals with any four asynchronous mode VT2 or TU-12 tributaries carried in SDH AU-4/AU-3 rate payload interface.

TXC-05802, CUBIT-*Pro* VLSI Device. A *CellBus*-based ATM cell switching device that supports unicast and multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing, and outlet cell queuing. This is a successor to the CUBIT device that has enhanced capabilities.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device performs section, line and path overhead processing for STS-1 SONET signals. It has programmable STS-1 or STS-N modes. It operates from a 3.3 volt supply and consumes less power than the SOT-1E TXC-03011 device with similar capability.

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- NOTES -

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