DATA SHEET

NE86C92
Twisted-pair transceiver interface

Product specification

IC19

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Philips Semiconductors

PHILIPS

Twisted-pair transceiver interface | NE86C92

DESCRIPTION

The NE86C92 is a twisted-pair transceiver that implements the IEEE 802.3 10BASE-T Ethernet specification. The circuit provides the connection between the Manchester encoder/decoder and the twisted-pair cable and includes a receiver, transmitter, collision detector, heartbeat generator, jabber timer, link integrity monitor, and control circuits and drivers for five LED status indicators.

The NE86C92 includes receive polarity detection with automatic polarity correction, smart squelch on all signal inputs for improved noise immunity, and a highly reliable crystal oscillator to set pre-distortion timing and the collision signal frequency.

The NE86C92 also allows for automatic selection between AUI and twisted-pair (RJ-45) connections; thus eliminating the need for end-users to remove the interface board and move jumpers to switch between connections. An application note is available which describes implementation of this feature.

The twisted-pair outputs and inputs connect to the twisted-pair cable through transmit and receive filters while the receiver output, collision detector output and transmitter input are connected to the Manchester encoder/decoder through pulse transformers. This interface to the encoder/decoder is, therefore, directly compatible with current 10Base2/10Base5 connections and allows easy expansion of existing interface cards for twisted-pair wiring.

During transmission the jabber timer is initiated to disable the NE86C92 in the event of a longer than legal length data packet. Collision detection circuitry monitors both the transmit path and the receiver input to determine the presence of colliding packets and signals the Manchester encoder/decoder in the event of a collision. At the end of every transmission the heartbeat generator creates a pseudo collision for a short time to ensure that the collision circuitry is functioning correctly. The link integrity monitor emits pulses onto the twisted-pair cable and expects to receive pulses from the twisted-pair cable at regular intervals. If no pulses or packets are received, a link failure has occurred; this is indicated by the RLED status indicator. Both heartbeat and link integrity monitor functions can be disabled.

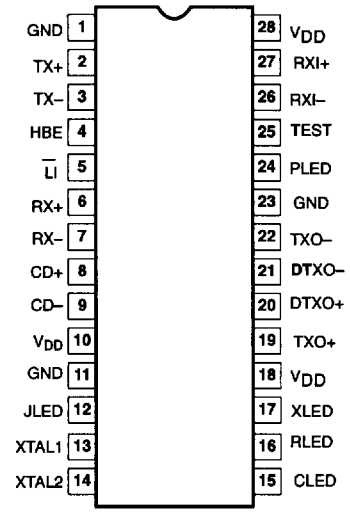
The NE86C92 is normally part of a three chip set for implementing a complete twisted-pair Ethernet network interface. The other chips are the Manchester encoder/decoder, such as the NE502A, and a Network Interface Controller, such as the NE86950.

APPLICATIONS

- 10BASE-T network interfaces for computers and workstations
- External 10BASE-T transceiver units

PIN CONFIGURATION

D and N Packages



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FEATURES

- Compatible with IEEE 802.3 10BASE-T specifications
- Integrates all transceiver functions, with selectable heartbeat and link test generators
- Twisted-pair polarity detection and automatic correction
- Smart squelch on all data inputs
- Internal transmitter pre-distortion generator
- Supports automatic selection between AUI and RJ-45 connections
- Five LED status signals with on-chip drivers for transmit, receive and link integrity, collision, jabber status and twisted pair polarity reversal
- Advanced CMOS process uses single 5V supply
- Extremely low power operation: 24mA typical idle current

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
28-Pin Plastic Dual In-Line Package (DIP) (.600 in. wide)	0 to 70°C	NE86C92N	SOT117-2
28-Pin Plastic Small Outline Large (SOL) Package	0 to 70°C	NE86C92D	SOT136-1

PIN DESCRIPTIONS

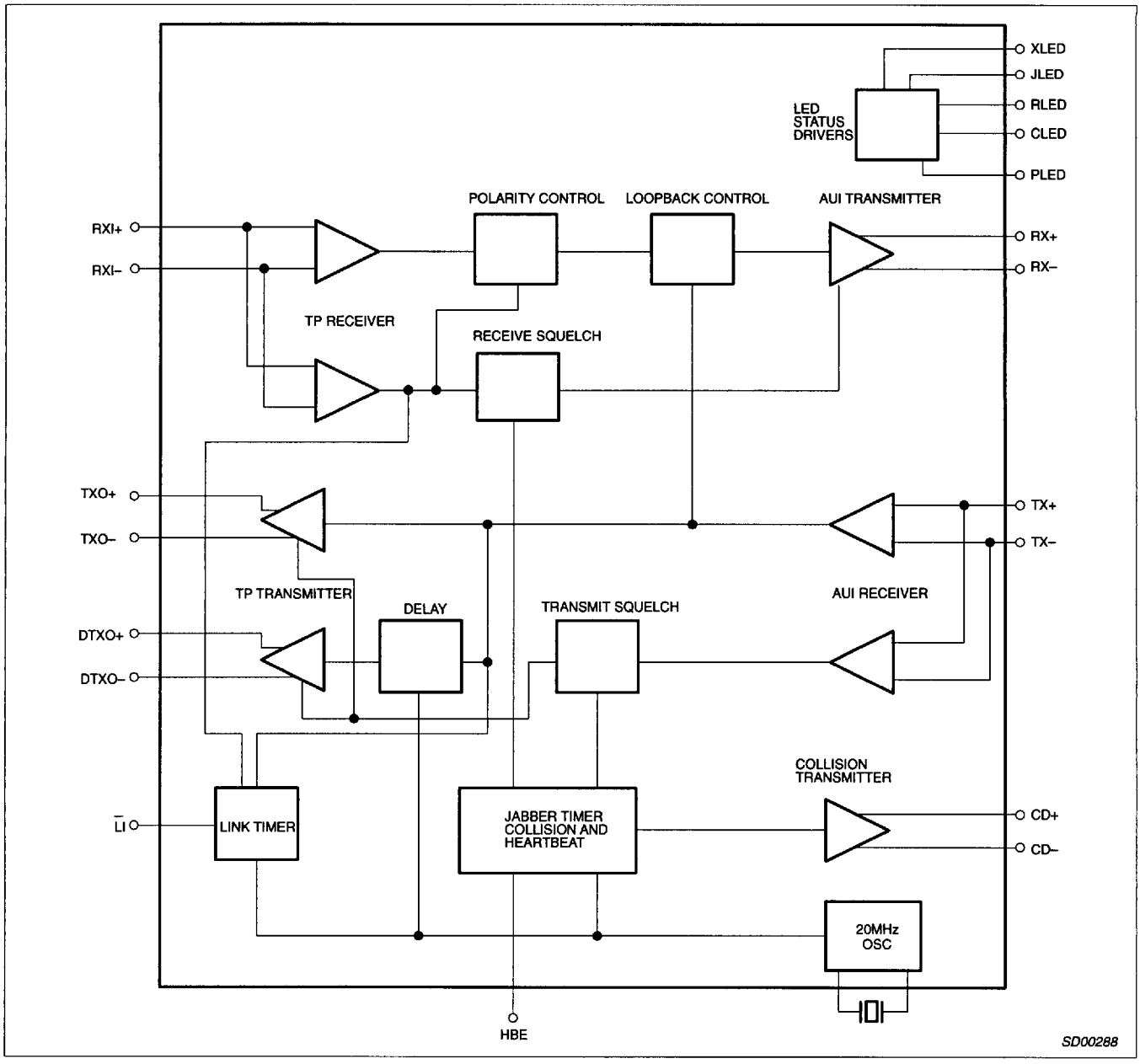
Pin No.	Symbol	Description
1	GND	Ground
2, 3	TX+, TX–	Transmitter inputs. Balanced differential line receiver. Inputs which accept the transmission signal from the Manchester encoder/decoder and apply it to the Twisted-Pair cable at TXO+, DTXO+, TXO– and DTXO-.
4	HBE	Heartbeat Enable. The heartbeat function is disabled when this pin is connected to GND and enabled when connected to V_{DD} or left floating.
5	$\overline{LI}$	Link Integrity. The link integrity function is disabled when this pin is connected to V_{DD} or left floating and enabled when connected to GND.
6, 7	RX+, RX-	Receive Outputs. Balanced differential line driver outputs which send the received signal to the Manchester encoder/decoder.
8, 9	CD+, CD-	Collision Outputs. Balanced differential line driver outputs which send a 10MHz oscillation signal to the Manchester encoder/decoder in the event of a collision, jabber interrupt or heart beat test.
10	V_{DD}	Positive power supply
11	GND	Ground.
12	JLED	Jabber Indicator. Indicates that the jabber timer has timed out and the twisted-pair drivers are disabled.
13	XTAL1	Crystal pin. One terminal of 20MHz crystal; or 20MHz external clock input.
14	XTAL2	Crystal Pin. One terminal of 20MHz crystal.
15	CLED	Collision Indicator. Indicates that a collision has been detected.
16	RLED	Receive Indicator. Indicates a packet is being received from the twisted-pair cable.
17	XLED	Transmit Indicator. Indicates a packet is being transmitted onto the twisted-pair cable.
18	V_{DD}	Positive power supply
19 20 21 22	TXO+, DTXO+, DTXO-, TXO-	Twisted-Pair drivers. These four outputs provide twisted-pair drive with pre-distortion. TXO+ and TXO- are balanced differential outputs that follow the signal at the TX+ and TX- inputs. DTXO+ and DTXO- are delayed and inverted with respect to TXO– and TXO+. Combining these outputs through an external resistor network provides the necessary pre-distortion to overcome the twisted-pair cable attenuation characteristics.
23	GND	Ground.
24	PLED	Polarity reversal indicator. Indicates polarity reversal of the twisted-pair receiver wires. A no-connect at this pin enables auto-correction although there is no LED indication. Connecting to GND disables auto-correction.
25	TEST	Test. No Connection, or connect to ground.
26, 27	RXI-, RXI+	Receiver inputs. These inputs receive the data from the twisted-pair cable and pass it on to RX+ and RX-.
28	V_{DD}	Positive power supply.

NOTE: The IEEE 802.3 designation for CD is CI, for RX is DI, for TX is DO, for RXI is RD and for TXO and DTXO combined is TD.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{DD}	Supply voltage with respect to GND	-0.5 to +6.5	V
V_{IN}	Voltage at any input to GND	-0.5 to V_{DD} +0.5	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec)	+300	°C
T_J	Recommended max junction temperature	+125	°C
θ_{JA}	Thermal impedance N package D package	55 70	°C/W °C/W

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

V_{DD} = +5V ±10%, T_A = 0°C to 70°C; unless otherwise stated. Typical values measured at V_{DD} = +5V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Power supply threshold and currents						
V_{DDEN}	Enable V_{DD} threshold			3.4		V
V_{DDDIS}	Disable V_{DD} threshold			1.2		V
I_{DDI}	Supply current (no traffic)			20		mA
I_{DDT}	Supply current transmitting	TXO± RXI± active, 90% duty cycle		65	100	mA
Digital input voltage (HBE, $\overline{LI}$)						
V_{IL}	Input LOW voltage		GND - 0.3		0.8	V
V_{IH}	Input HIGH voltage		2.0		V_{DD} + 0.3	V
Digital input current (HBE, $\overline{LI}$, PLED)						
I_{IN}	Input current	GND - 0.3 < V_{IN} < V_{DD} + 0.3	-500		0	µA
LED driver output voltage						
V_{OL}	Output LOW voltage	I_{OUT} = 10mA			0.4	V
LED driver leakage current						
I_{OL}	Output leakage current, output inactive	GND < V_{OUT} < V_{DD} + 0.3			30	µA
I_{OLPLED}	PLED output leakage current, inactive	GND < V_{OUT} < V_{DD} + 0.3			500	µA
Transmitter, receiver and collision indicator						
V_{OC}	TX±, RXI± open circuit input voltage		1.5		3.5	V
I_{ITR}	TX+, TX-, RXI+, RXI- input current	GND - 0.3 < V_{IN} < V_{DD} + 0.3	-500		+500	µA
R_{TX}	TX± differential input resistance		16			kΩ
V_{TS}	Transmitter squelch threshold		-150	-200	-300	mV
V_{OH}	Output HIGH voltage TXO±, DTXO±	Load = 500Ω to GND	V_{DD} – 0.1			V
V_{OL}	Output LOW voltage TXO±, DTXO±	Load = 500Ω to V_{DD}			0.1	V
R_{RXI}	RXI± differential input resistance		20			kΩ
V_{RS}	Receive squelch threshold		±300	±400	±585	mV
V_{OD}	Differential output voltage non-idle at RX±, CD±	R_L = 78Ω	±600	±825	±1200	mV
V_{OB}	Differential output voltage imbalance at RX±, CD±, idle and non-idle	R_L = 78Ω	-40		+40	mV
V_{TPOD}	Peak differential output voltage	R_L = 100, R_1 = 48, R_2 = 464		2.8		V
V_{TOB}	Differential output voltage imbalance at TXO±, DTXO± idle and non-idle		-40		+40	mV
R_{TS}	TXO±, DTXO± output resistance	I = 25mA		7	10	Ω

TIMING CHARACTERISTICS

V_{DD} = +5V ±10%, T_A = 0°C to 70°C; unless otherwise stated. Typical values measured at V_{DD} = +5V, T_A = 25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Receiver and collision signal						
t_{RST}	Receive start-up delay	$V_{RXI\pm}$ = 1V peak		250	500	ns
t_{RBL}	Bits lost at receiver start-up	$V_{RXI\pm}$ = 1V peak		2	4	bits
	First validly timed bit on RX±				t_{RBL} + 2	bits
t_{RD}	Receiver propagation delay RXI± to RX±	Include receive filter		40	100	ns
t_{ROFF}	Receiver turn-off pulse width		150		230	ns
t_{RHI}	Receiver high-to-idle time	Measured to ±210mV	200		400	ns
t_{CHI}	Collision high-to-idle time	Measured to ±210mV	400		500	ns
t_{RR}	Differential output rise time on RX±, CD±				5	ns
t_{RF}	Differential output fall time on RX±, CD±				5	ns
t_{RM}	Rise and fall time matching on RX±, CD±	t_{RF} - t_{RR}	-2		2	ns
t_{RJ}	Receiver added jitter RXI± to RX±	$V_{RXI\pm}$ = 1V peak	-1.5		+1.5	ns
t_{CMJ}	Receiver added common-mode jitter RXI± to RX±	$V_{RXI\pm}$ = 2.5V at receive filter input	-2.5		+2.5	ns
Transmitter						
t_{TST}	Transmit start-up delay	$V_{TX\pm}$ = 1V peak		280	400	ns
t_{TBL}	Bits lost at transmitter start-up	$V_{TX\pm}$ = 1V peak			2	bits
	First validly timed bit				t_{TBL+2}	bits
t_{TD}	Transmit propagation delay	$V_{TX\pm}$ = 1V peak (include transmitter filter)		50	100	ns
t_{TS}	Transmitter added jitter	Load = 100Ω and cable model	-3.5		+3.5	ns
t_{TOFF}	Transmitter turn off pulse width	$V_{TX\pm}$ = 1V	150		200	ns
t_{THI}	Transmitter high to idle time		250		450	ns
t_{PDPW}	Pre-distortion pulse width		45		55	ns
Link integrity						
t_{LTSD}	Transmit silence duration		8	16	24	ms
t_{LTPW}	Link test pulse width	With 100Ω load/measure at 585mV amplitude point	80		120	ns
t_{ICLTP}	Time period for ignored consecutive link pulses	$V_{RXI\pm}$ = 1V peak	2	5	7	ms
t_{CCLTP}	Time period for counted consecutive link pulses	$V_{RXI\pm}$ = 1V peak	25	48	150	ms
t_{LLD}	Link loss detect time		50	110	150	ms
Collision and jabber						
f_{CD}	Collision frequency		8.5	10.0	11.5	MHz
t_{CP}	Collision signal pulse width		40	50	60	ns
t_{CON}	Collision turn-on delay				9	bits
t_{COFF}	Collision turn-off delay				9	bits
t_{HON}	Heartbeat turn-on delay		0.6	1.1	1.6	µs
t_{HW}	Heartbeat test duration		0.5	1.0	1.5	µs
t_{JA}	Jabber activation delay		20	50	150	ms
t_{JR}	Jabber reset delay		250	450	750	ms

TIMING CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Loopback						
t_{LBON}	Loopback start-up delay				9	bits
t_{LBE}	Loopback enable time RXI± to RX±				9	bits
t_{LBD}	Loopback disable time RXI± to RX±				9	bits
t_{LBPD}	Loopback propagation delay TXI± to RX±				200	ns
LEDs						
t_{LED}	Turn-on or turn-off delay of LEDs				10	µs
$t_{XLEDOFF}$	XLED maximum off time		95		135	ms
t_{XLEDON}	XLED minimum on time		5		10	ms
$t_{RLEDOFF}$	RLED maximum off time	$\overline{CT}$ = high (V_{DD})	95		135	ms
t_{RLEDON}	RLED minimum on time		5		10	ms
t_{RLEDLL}	RLED turn-off time for link loss[1]			t_{LL}		ms
t_{RLEDLE}	RLED on time after link re-established	$\overline{CT}$ = low (GND)	0.5		1.5	sec
t_{CLEDON}	CLED minimum on time		10	11.5	14	ms
t_{JLEDON}	JLED on time[2]	ON while jabber is active		t_{JON}		ms
$t_{JLEDOFF}$	JLED off time[3]	OFF while jabber is inactive		t_{JOFF}		ms

NOTES:
1. t_{LL} = duration of link loss
2. t_{JON} = jabber active time.
3. t_{JOFF} = jabber inactive time

FUNCTIONAL DESCRIPTION

The NE86C92 contains eight main functional blocks (see Block Diagram). These are:

1. The receiver which takes data from the twisted-pair cable and sends it to the Manchester encoder/decoder.
2. The receive polarity detector and correction control which detects the polarity of the received signal and internally corrects the polarity of a reversed polarity connection.
3. The transmitter which receives data from the Manchester encoder/decoder and sends it onto the twisted-pair cable.
4. The collision detection and heartbeat generation circuitry which indicates to the Manchester encoder/decoder any collision resulting from a coincident transmit and receive activity and tests for collision circuitry functionality at the end of every transmission.
5. The jabber timer which disables the transmitter in the event of a longer than legal length data packet.
6. The link integrity monitor which periodically tests the integrity of the twisted-pair link and indicates if a link failure occurs.
7. A crystal controlled oscillator which provides all on-chip timing functions for control, pre-distortion and the 10MHz collision signal.
8. LED control circuitry and drivers for indicating the transmit, receive and link integrity, collision, jabber and Twisted-Pair polarity status of the NE86C92.

Receiver Functions

The receiver section consists of a differential twisted-pair receiver, a squelch circuit and a differential line driver for the AUI cable.

The twisted-pair receiver is connected to the output of a bandpass filter whose input is transformer coupled to the twisted- pair cable. The receiver has a high differential input impedance to allow accurate external resistors to be used for matching to the bandpass filter. The common mode voltage of the input buffer is set internally on the chip.

The receiver squelch circuit prevents noise on the twisted-pair cable from falsely triggering the receiver in the absence of true data. The twisted-pair receiver will be activated if the differential signal at the RXI pins exceeds typically ±400mV and has a low-high-low sequence with both the positive and negative pulse widths exceeding 50ns. Once activated the squelch threshold reduces to ±200mV to ensure reception. The fifth bit of the Manchester code is always received. The receiver is de-activated by a continuous high of between 150ns and 230ns. The receiver is then inhibited for a further 500ns at the end of a packet in order to reject dribble bits or the twisted-pair cable.

The data packet passed on to the Manchester encoder/decoder will typically have a high-to-idle time of 300ns.

The differential line driver provides typically ±825mV signals into a 78Ω transmission line connecting the transceiver to the Manchester encoder/decoder with rise and fall times less than 5ns. When in the idle state (no received or transmitted signal) both outputs are pulled to GND and provide < 40mV differential voltage offset to minimize DC standing current in the transformer.

Polarity Control Functions

The polarity control circuitry consists of a polarity detector and a polarity correction circuit. The polarity detector is activated following

a link failure or power-on reset. It then waits for the detection of four consecutive link test pulses of the same polarity, or the reception of a data frame to determine the correct polarity. Having determined the correct polarity, the correction circuit provides the correct data polarity to the receiver and the link integrity pulse detector.

The PLED pin provides a buffered output indication of the status of the polarity correction circuit. This output may be used to drive an LED directly (through an external current limiting resistor to V_{DD}) for visual indication of polarity.

The polarity detection and correction circuit may be externally DISABLED by connecting PLED (Pin 24) to ground.

Transmitter Functions

The transmitter consists of a differential receiver, a squelch circuit and a differential twisted-pair cable driver with pre-distortion. When data is being transmitted, and there is no collision or link integrity failure, the transmitted data is looped back to the receiver output ports RX+ and RX-.

The common mode voltage of the differential input buffer is set internally with a differential input resistance of typically 40 kΩ.

The transmitter squelch circuit prevents false triggering of the transmitter from noise on the AUI cable. The transmitter will be activated if the differential signal at the TX± pins exceeds typically ±200mV and has a high-low sequence with both the positive and negative pulse widths exceeding 50ns. The third bit of the Manchester data is always transmitted. The transmitter is de-activated by a continuous high of between 150ns and 200ns.

Pre-distortion of the transmitted waveform is included to reduce the bit dependent jitter at the end of a twisted-pair cable caused by it's inherent low pass characteristics. The pre-distortion is achieved by using two pairs of differential twisted-pair drivers. One pair of drivers produces a signal delayed by 50ns compared to the other. By combining the four driver outputs through an external resistor network, the signal on the twisted-pair is pre-emphasized for the first 50ns following a voltage transition. The pre-emphasis can be changed by selection of different external resistance values.

Collision Functions

The collision circuitry consists of logic for detecting simultaneous transmission and reception, a heartbeat generator, a 10MHz signal source and a differential line driver.

The collision detection scheme implemented in the NE86C92 is transmit mode detection which detects a collision if both the transmitter and receiver are active at the same time. A collision condition is indicated to the Manchester encoder/decoder by a 10MHz signal at the CD outputs of the differential line driver and occurs within 900ns of the onset of a collision. The collision signal begins with a negative going pulse and ends with a continuous high-to-idle state of typically 450ns.

When a collision occurs the internal loopback is disabled and the signal received at the RXI inputs is passed to the RX outputs. At the end of a collision the loopback is enabled again.

At the end of every transmission the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is properly functioning. The pseudo collision consists of a 1µs burst of 10MHz signal at the CD outputs approximately 1us after the end of the transmission. The heartbeat function can be disabled externally by connecting the HBE (heartbeat enable) to GND. This allows the NE86C92 to be used in hub or repeater applications.

As with the receiver outputs the collision outputs CD+ and CD- are pulled low in the idle state and maintain < 40mV offset to minimize DC standing current in the transformer.

Jabber Functions

The jabber timer monitors the transmitter and inhibits transmission if it is active for longer than typically 50ms. The jabber circuit then enables the collision outputs for the remainder of the data frame and for typically 450ms (unjab time) after it has ended. At this point the transmitter becomes uninhibited.

Link Integrity Functions

This circuit monitors the integrity of the twisted-pair cable connected to the RXI inputs. In the event of a fault, the transmit, loopback and receive functions of the NE86C92 are disabled and the fail status is indicated by turning off the LED connected to RLED.

The twisted-pair cable integrity is monitored by detecting periodic link-integrity pulses at the RXI inputs. These pulses are 100ns in duration, with pre-distortion, followed by a return to idle. The receiver does not recognize these as data and is not enabled by them.

When no data frames are being received the NE86C92 provides a link-integrity reception window during which a link pulse is expected to arrive. The window opens nominally 5ms after receipt of the previous link pulse or the end of a data frame and remains open for 110ms. If a link pulse is received before the window opens then it is ignored. If a link pulse arrives while it is open then the internal window timers are reset. If no link pulse is received after 110ms, then the transmit, receive and loopback functions are disabled and a link failure is indicated by turning OFF the LED connected to RLED.

The NE86C92 can only re-enable the transmit, loopback and receive functions if it receives four consecutive link pulses within the link pulse window, or if a data frame is received. In either case the NE86C92 waits until both the transmit and receive paths are idle before re-enabling the transmit, loopback and receive paths.

When the link integrity circuit is enabled ($\overline{LI}$ connected to GND) a link integrity pulse is transmitted onto the twisted-pair cable typically once every 16ms irrespective of whether the transmitter is jabbed or there is a link integrity failure.

If the link integrity circuit is disabled ($\overline{LI}$ connected to V_{DD}) no link pulses are transmitted, the received link pulses are ignored and the RLED indicator remains ON in the absence of receive traffic.

Crystal Controlled Oscillator

Clock signals for the 50ns pre-distortion delay for transmitted data, the 10MHz collision signal and all on-chip timing functions are produced by a 20MHz crystal controlled oscillator.

An external MOS-level or TTL clock can also be applied directly to the XTAL1 input. In the case XTAL2 provides a buffered output of the signal applied to XTAL1; and may be left disconnected, used to drive other devices, or connected ground.

Any commercially available parallel resonant crystal may be used, but it is recommended that the total capacitance on each of the XTAL pins should be kept below 20pF.

LED Status Functions

The NE86C92 provides output drivers for five LED status indicators.

The LED connected to XLED indicates transmit status; (see Figure 8)

- The LED is ON when no transmission is in progress.
- The LED turns OFF when a data frame is transmitted and remains OFF for typically 115ms.
- The LED then turns back ON for a minimum of typically 6.4ms until turned OFF by the next transmission.

The LED connected to RLED indicates receive status and behaves differently depending on whether the link integrity circuit is disabled or enabled.

When the link integrity circuit is disabled; (see Figure 10)

- The LED is ON when no reception is in progress.
- The LED turns OFF when a data frame is received and remains OFF for typically 115ms.
- The LED then turns back ON for a minimum of typically 6.4ms until turned OFF by the next reception.

When the link integrity circuit is enabled the LED behavior is the same as above except that; (see Figure 2)

- The LED is ON when both no reception is in progress and link integrity pulses are being successfully received.
- The LED turns OFF in the event of a link failure
- The LED turns back ON for nominally 1sec when the the link is re-established.

The LED connected to CLED indicates collision status; (see Figure 9)

- The LED is OFF for no collision.
- The LED turns ON for nominally 12ms in the event of a collision.
- The LED remains ON if a further collisions occur during this time and remains ON for the nominal on-time following the last transition.
- There is no minimum OFF time. The LED will turn ON immediately another collision is detected.

The LED connected to JLED indicates jabber status; (see Figure 7)

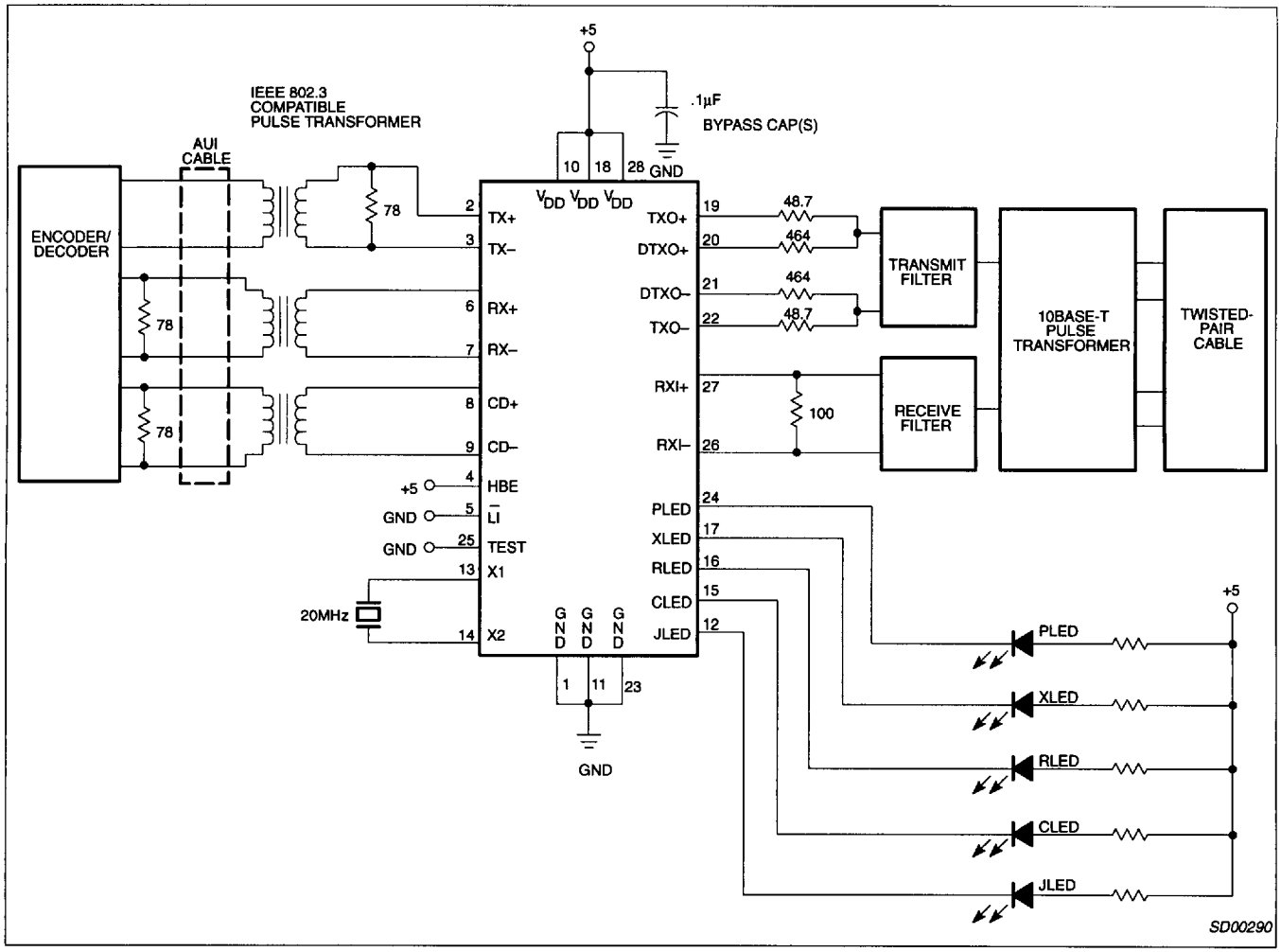
- The LED is OFF for a no-jab condition.
- The LED turns ON when the twisted-pair drivers are jabbed.
- The LED turns back OFF when the twisted-pair drivers are unjabbed.

The LED connected to PLED (when used) indicates polarity reversal status;

- The LED is ON when there is no polarity reversal of the twisted-pair receive wires.
- The LED is OFF when the polarity is reversed.
- The LED flashes during link-fail before polarity has been determined.

The LED drivers require an external resistor in series with the LED (see connection diagram) to limit the LED current.

TYPICAL APPLICATION DIAGRAM



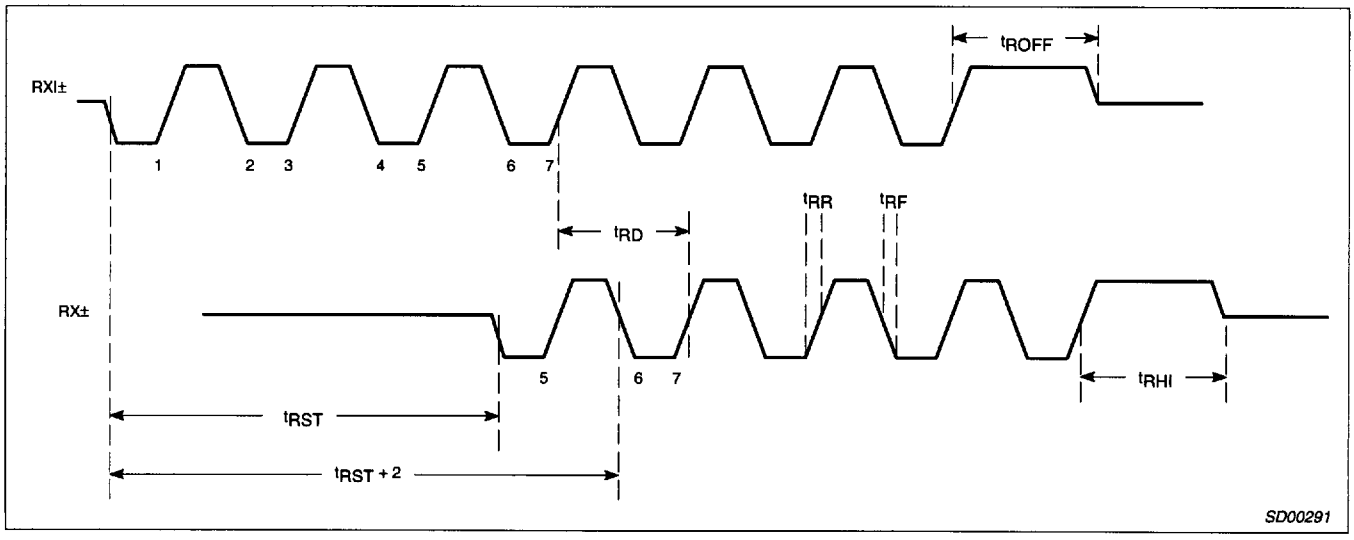


Figure 1. Receiver Timing

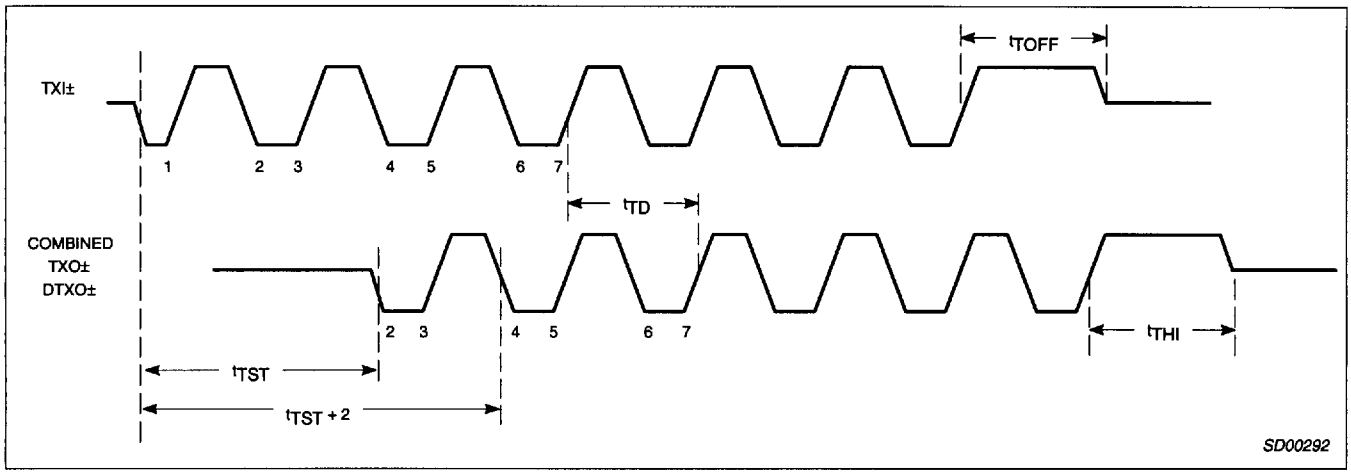


Figure 2. Transmitter Timing

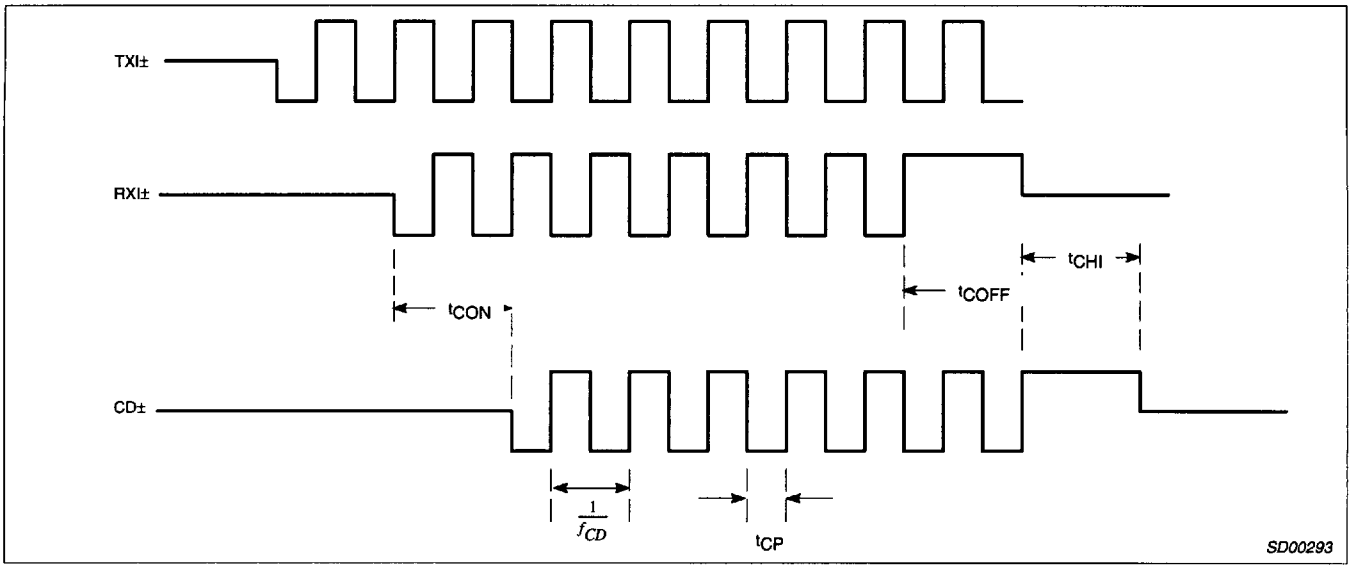


Figure 3. Collision Timing

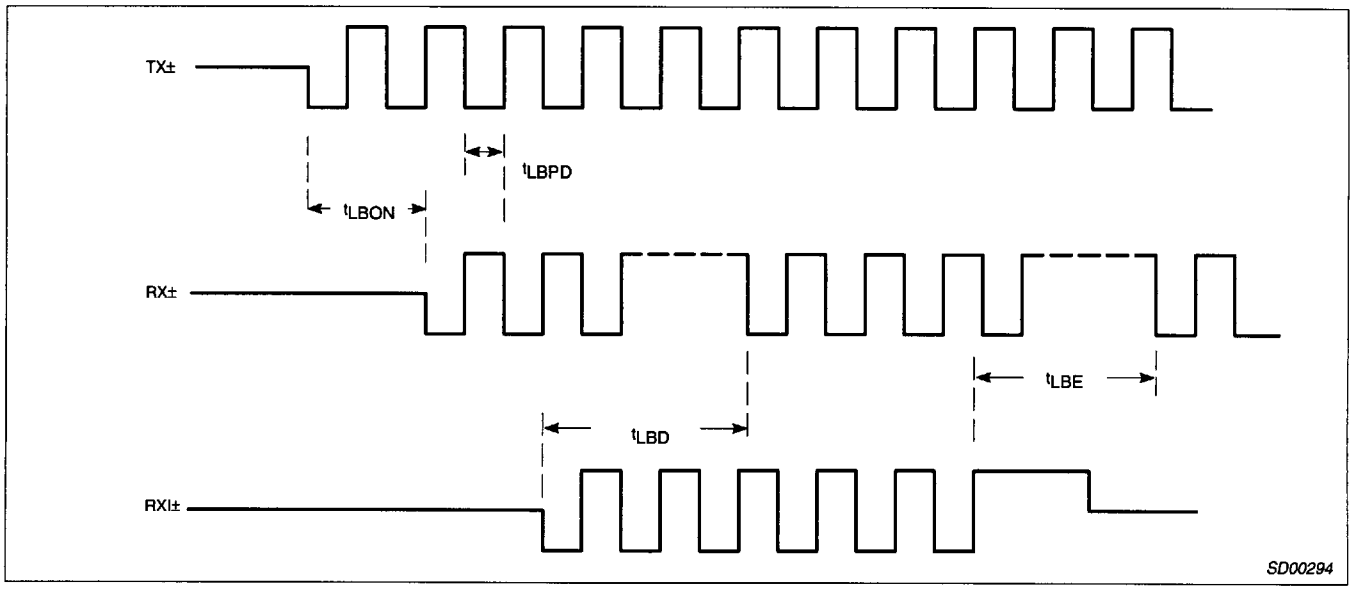


Figure 4. Loopback Timing

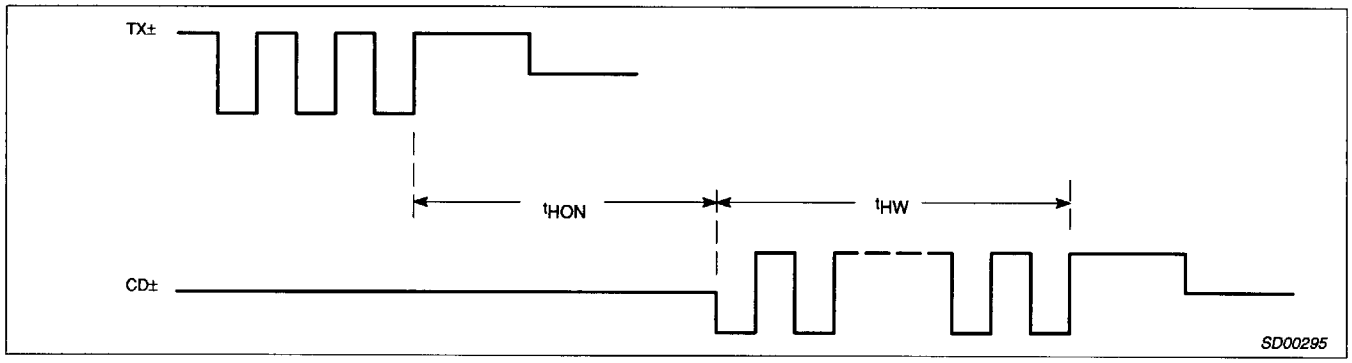


Figure 5. Heartbeat Timing

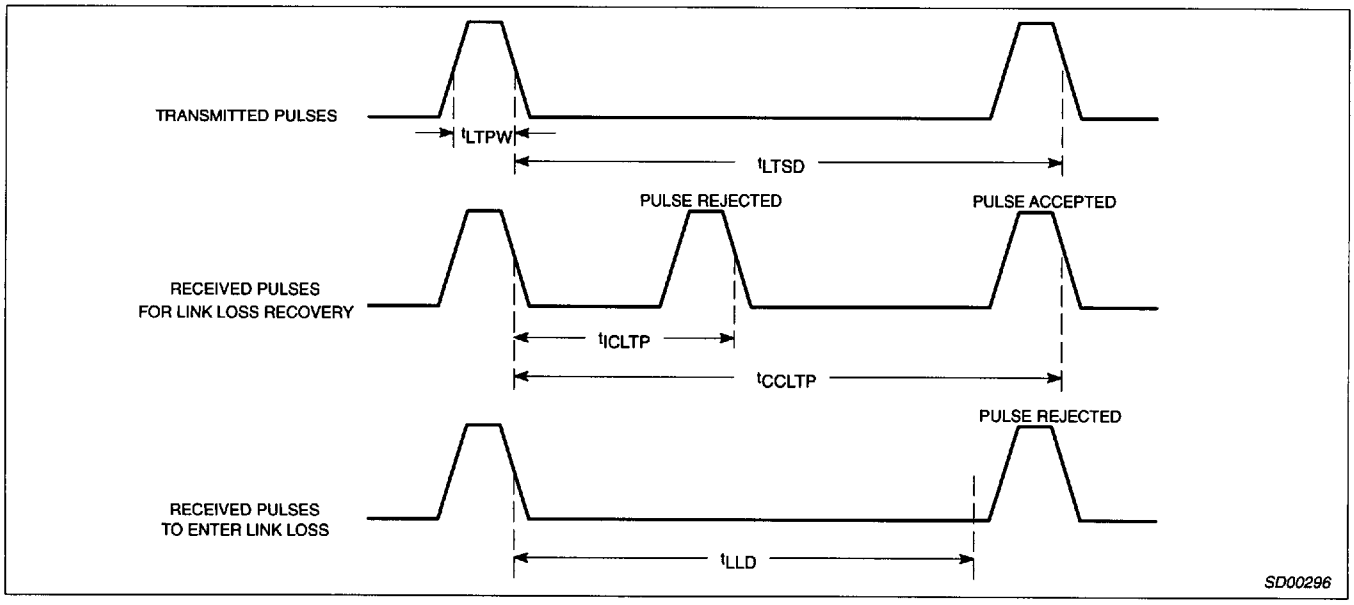


Figure 6. Link Test Timing

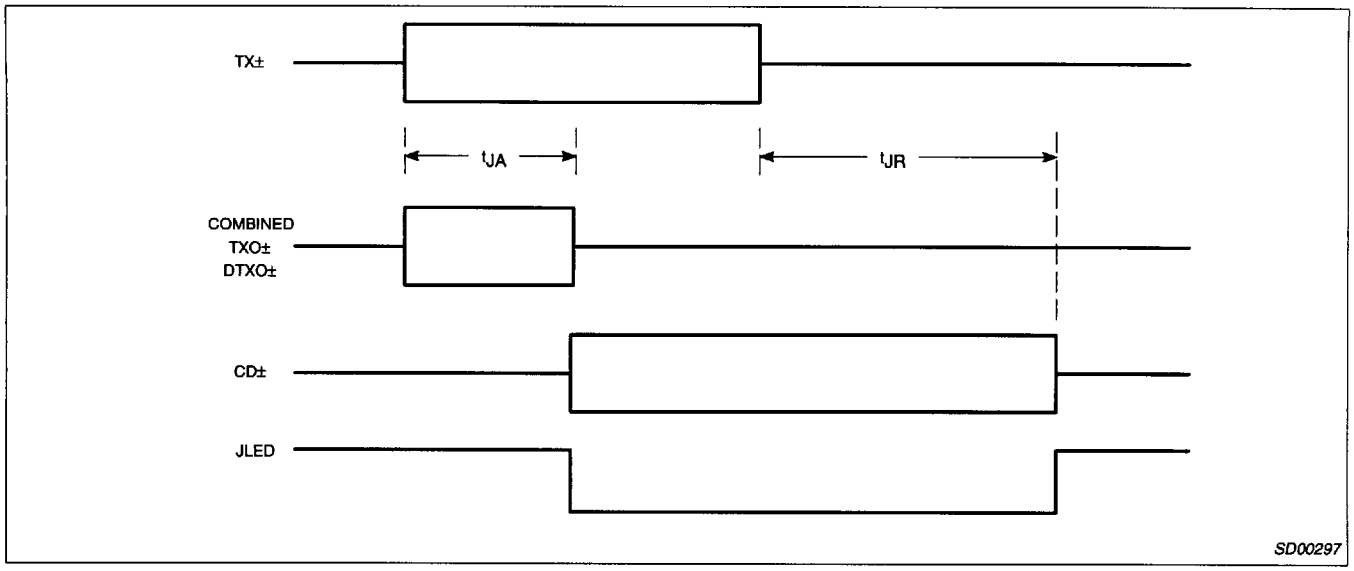


Figure 7. Jabber Timing

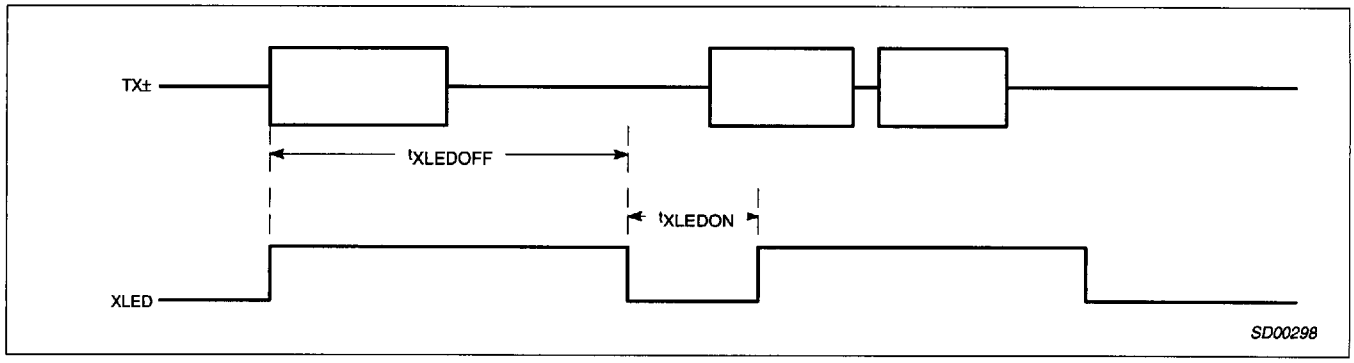


Figure 8. XLED Timing

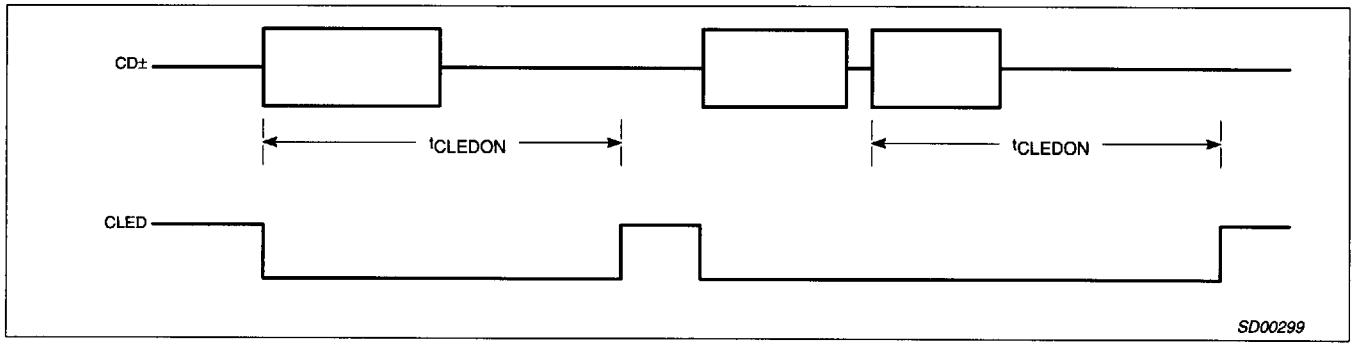


Figure 9. CLED Timing

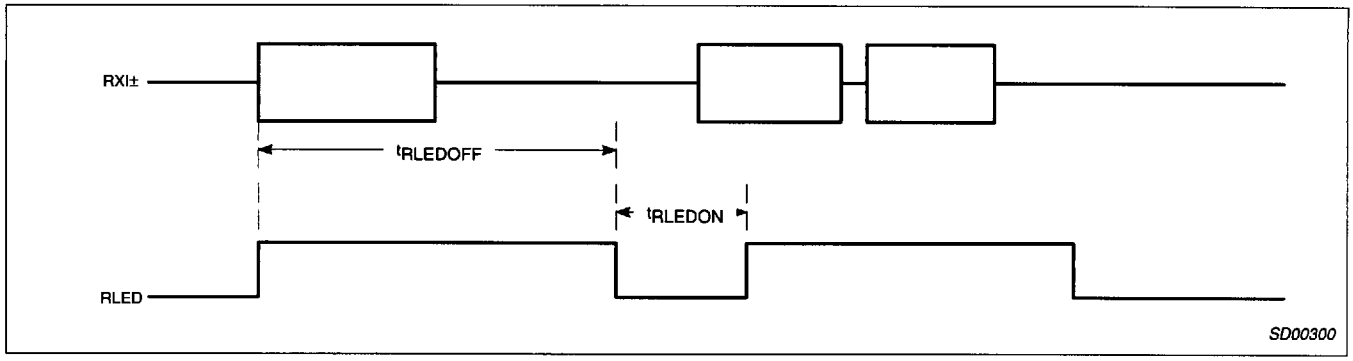


Figure 10. RLED Timing (LI Disabled)

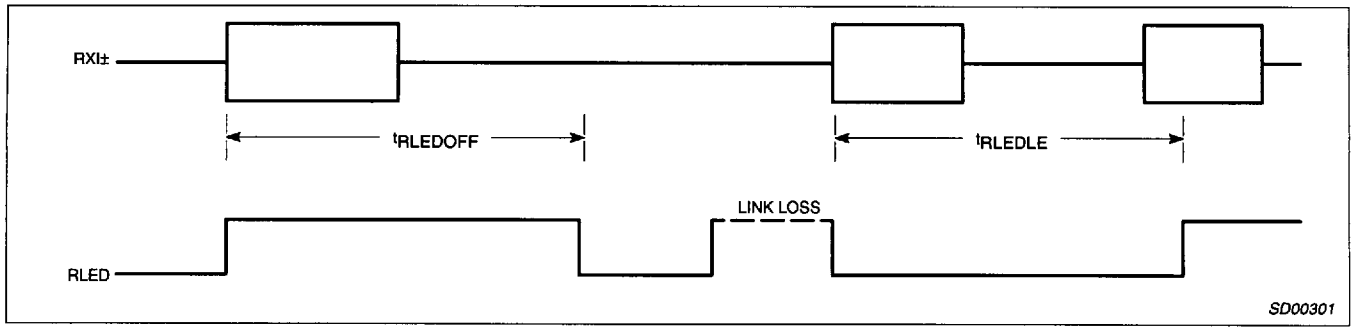
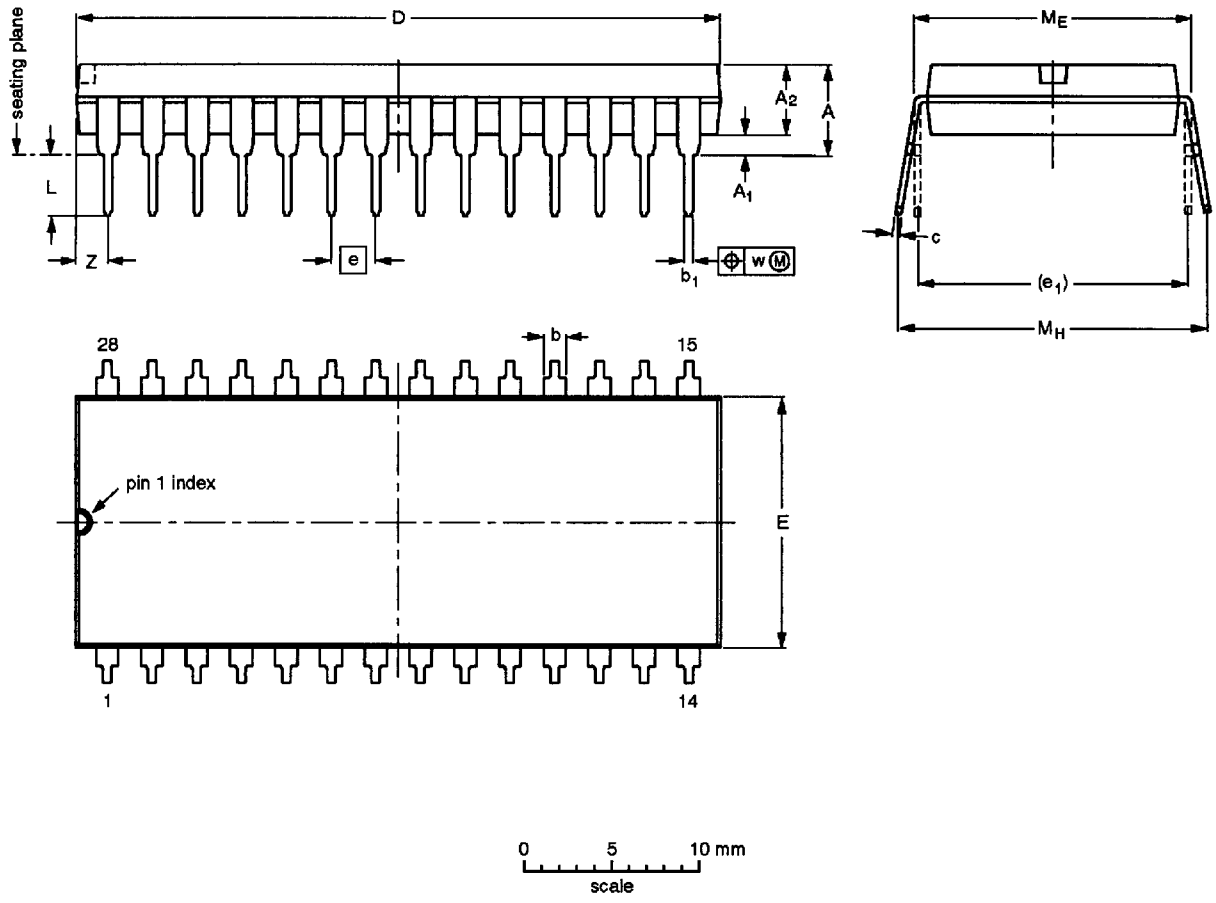


Figure 11. RLED Timing (LI Enabled)

DIP28: plastic dual in-line package; 28 leads (600 mil); long body SOT117-2



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

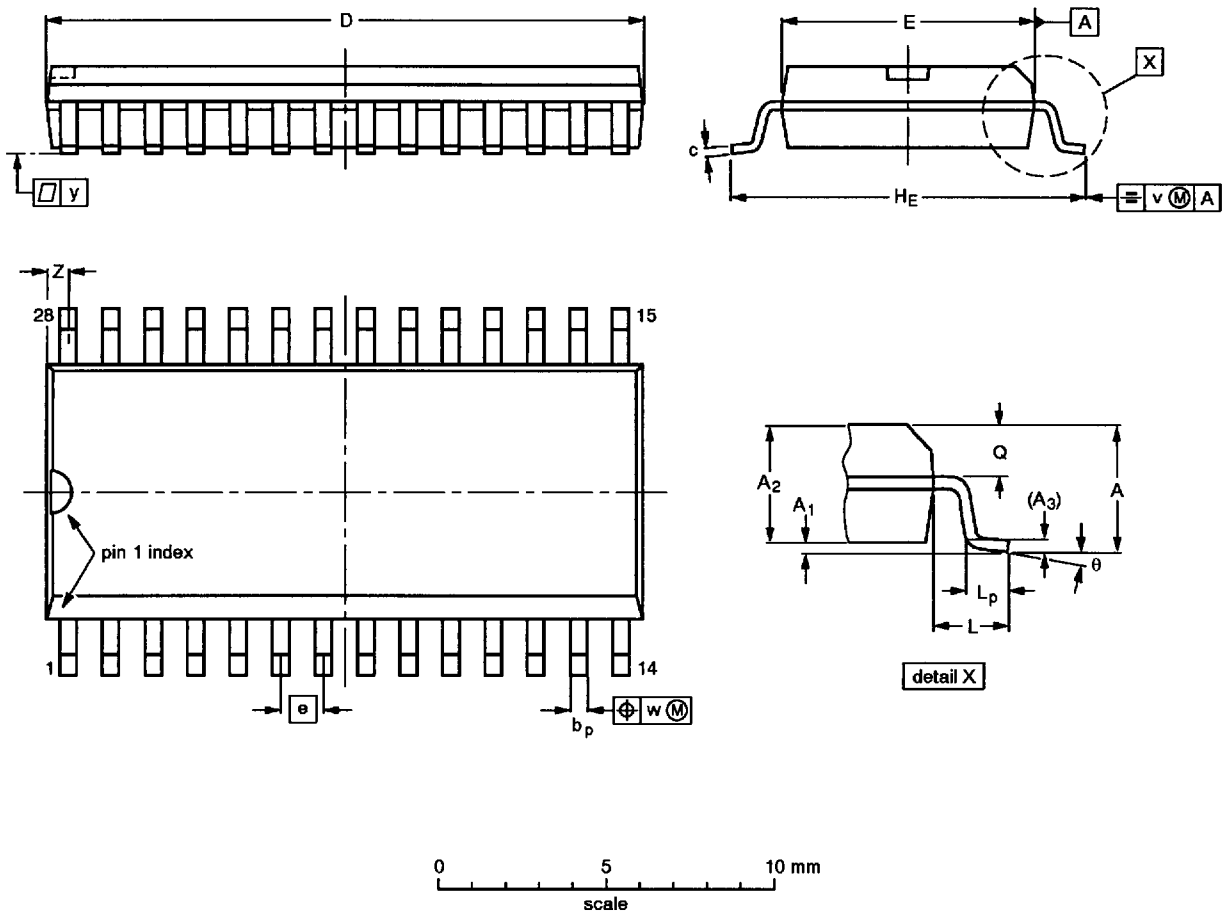
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	5.08	0.51	3.94	1.63 1.14	0.56 0.43	0.38 0.25	37.08 35.94	14.22 13.84	2.54	15.24	3.51 3.05	15.75 15.24	17.65 15.24	0.25	2.10
inches	0.200	0.020	0.155	0.064 0.045	0.022 0.017	0.015 0.010	1.460 1.415	0.560 0.545	0.100	0.600	0.138 0.120	0.62 0.60	0.695 0.600	0.01	0.083

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-2		MS-011AB				95-03-11

SO28: plastic small outline package; 28 leads; body width 7.5mm SOT136-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24