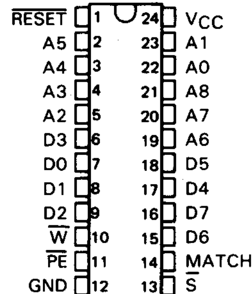
D2993, JANUARY 1987—REVISED SEPTEMBER 1987

- **Address to MATCH Valid Time**
  TACT2150-20 . . . 20 ns max
  TACT2150-30 . . . 30 ns max
- **300-Mil 24-Pin Ceramic Side-Brazed or Plastic Dual-In-Line or Small Outline Packages**
- **53 mA Typical Supply Current**
- **On-Chip Parity Generation and Checking**
- **Parity Error Output/Force Parity Error Input**
- **On-Chip Address/Data Comparator**
- **Asynchronous, Single-Cycle Reset**
- **Easily Expandable**
- **Fully Static**
- **Reliable Advanced CMOS Technology**
- **Fully TTL Compatible**

DW, JD, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit-slice cache address comparator consists of a high-speed 512 × 9 static RAM array, parity generator, parity checker, and 9-bit high-speed comparator. It is fabricated using Advanced CMOS technology for high-speed, low-power interface with bipolar TTL circuits. The cache address comparator is easily cascadable for wider tag addresses or deeper tag memories. Significant reductions in cache memory component count, board area, and power dissipation can be achieved with this device.

When $\overline{S}$ is low and $\overline{W}$ is high, the cache address comparator compares the contents of the memory location addressed by A0-A8 with the data on D0-D7 plus generated parity. An equality is indicated by the high level on the MATCH output. A low-level output from $\overline{PE}$ signifies a parity error in the internal RAM data. $\overline{PE}$ is an N-channel open-drain output for easy OR-tying. During a write cycle ($\overline{S}$ and $\overline{W}$ low), data on D0-D7 plus generated even parity are written in the 9-bit memory location addressed by A0-A8. Also during write, a parity error may be forced by holding $\overline{PE}$ low.

A reset input is provided for initialization. When $\overline{RESET}$ is taken low, all 512 × 9 RAM locations are cleared to zero (with valid parity) and the MATCH output is forced high. If an input data word of zero is compared to any memory location that has not been written into since reset, MATCH will be high indicating that input data, plus generated parity, is equal to the reset memory location. $\overline{PE}$ will be high for every addressed memory location after reset indicating no parity error in the RAM data. By tying a single data input pin high, this bit will function as a valid bit and a match will not occur unless data has been written into the addressed memory location. When cascading in the width direction, only one bit needs to be tied high regardless of the address width.

The TACT2150 operates from a single 5 V supply and is offered in a 24-pin 300-mil ceramic side-brazed or plastic dual-in-line packages and plastic "Small Outline" packages. The device is fully TTL compatible and is characterized for operation from 0°C to 70°C.

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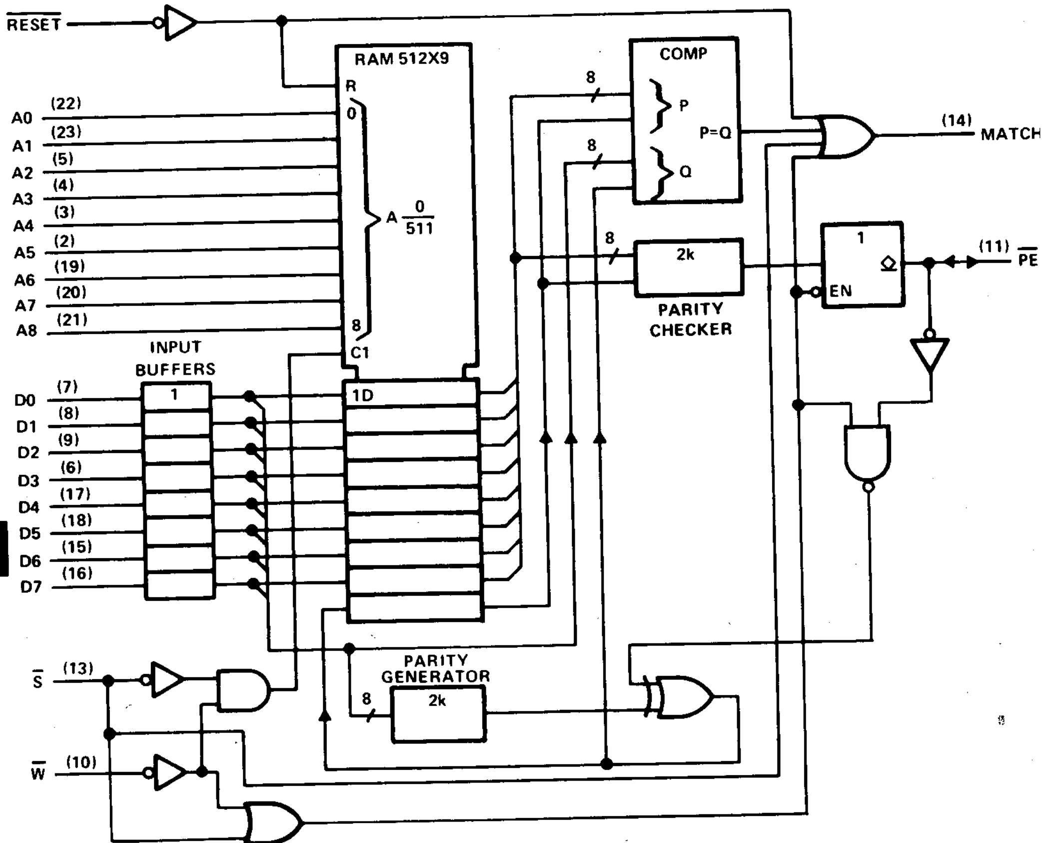
functional block diagram (positive logic)



MATCH OUTPUT DESCRIPTION

MATCH = V_{OH} if: [A0-A8] = D0-D7 + parity,
or: $\overline{\text{RESET}}$ = V_{IL},
or: $\overline{\text{S}}$ = V_{IH},
or: $\overline{\text{W}}$ = V_{IL}

MATCH = V_{OL} if: [A0-A8] ≠ D0-D7 + parity,
with $\overline{\text{RESET}}$ = V_{IH},
$\overline{\text{S}}$ = V_{IL}, and $\overline{\text{W}}$ = V_{IH}

FUNCTION TABLE

OUTPUT		FUNCTION DESCRIPTION
MATCH	$\overline{\text{PE}}$	
L	L	Parity Error
L	H	Not Equal
H	L	Undefined Error
H	H	Equal

Where $\overline{\text{S}}$ = V_{IL}, $\overline{\text{W}}$ = V_{IH}, $\overline{\text{RESET}}$ = V_{IH}

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PIN FUNCTIONAL DESCRIPTION

PIN NAME	PIN NO.	DESCRIPTION
A0	22	Address inputs. Address 1 of 512-by-9-bit random-access memory locations. Must be stable for the duration of the write cycle.
A1	23	
A2	5	
A3	4	
A4	3	
A5	2	
A6	19	
A7	20	
A8	21	
D0	7	Data inputs. Compared with memory location addressed by A0-A8 when $\overline{W}$ is at V_{IH} and $\overline{S}$ is at V_{IL}. Provide input data to RAM when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}.
D1	8	
D2	9	
D3	6	
D4	17	
D5	18	
D6	15	
D7	16	
GND	12	Ground
MATCH	14	When MATCH output is at V_{OH} during a compare cycle, D0 through D7 plus parity equal the contents of the 9-bit memory location addressed by A0 through A8.
$\overline{PE}$	11	Parity error input/output. During write cycles, $\overline{PE}$ can force a parity error into the 9-bit location specified by A0 through A8 when $\overline{PE}$ is at V_{IL}. For compare cycles, $\overline{PE}$ at V_{OL} indicates a parity error in the stored data. $\overline{PE}$ is an open-drain output so an external pull-up resistor is required.
$\overline{RESET}$	1	$\overline{RESET}$ input. Asynchronously clears entire RAM array and forces MATCH high when $\overline{RESET}$ is at V_{IL} and $\overline{W}$ is at V_{IH}.
$\overline{S}$	13	Chip select input. Enables device when $\overline{S}$ is at V_{IL}. Deselects device and forces MATCH high when $\overline{S}$ is at V_{IH}.
V_{CC}	24	5-V supply voltage
$\overline{W}$	10	Write control input. Writes D0 through D7 and generated parity into RAM and forces MATCH high when $\overline{W}$ is at V_{IL} and $\overline{S}$ is at V_{IL}. Places selected device in compare mode if $\overline{W}$ is at V_{IH}.

application

Due to the high-performance switching characteristics of the TACT2150, it is necessary that the address inputs not be allowed to float. Proper termination techniques should be employed. It is recommended that the RC time constant associated with the address inputs (63.2% of rise time on A0-A8) not exceed 60 ns.

absolute maximum ratings over operating free-air temperature range (unless otherwise specified)

Supply voltage range, V_{CC} (see Note 1) .... −1.5 to 7 V
Input voltage range, any input .... −1.5 to 7 V
Continuous power dissipation .... 1 W
Operating free-air temperature range .... 0°C to 70°C
Storage temperature range .... −65°C to 150°C

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		V_{CC}+0.5	V
V_{IL}	Low-level input voltage (See Note 2)		−0.5		0.8	V
V_{OH}	High-level output voltage	$\overline{PE}$			5.5	V
I_{OH}	High-level output current	MATCH			−8	mA
I_{OL}	Low-level output current	MATCH			8	mA
		$\overline{PE}$			16	
T_A	Operating free-air temperature		0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TACT2150-20			TACT2150-30			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{OH(M)}$	MATCH high-level output voltage	I_{OH} = −8 mA, V_{CC} = 4.5 V	2.4			2.4			V
		I_{OH} = −20 μA, V_{CC} = 4.5 V	3.5			3.5			
$V_{OL(M)}$	MATCH low-level output voltage	I_{OL} = 8 mA, V_{CC} = 4.5 V			0.4			0.4	V
$V_{OL(PE)}$	$\overline{PE}$ low-level output voltage	I_{OL} = 16 mA, V_{CC} = 4.5 V,			0.4			0.4	V
I_I	Input current	V_I = 0 V to 5.5 V			10			10	μA
I_{OS}	Short-circuit MATCH output current	V_O = GND, V_{CC} = 5.5 V			−150			−150	mA
I_{CC1}	Supply current (operative)	$\overline{RESET}$ = V_{IH}		53	95		53	95	mA
I_{CC2}	Supply current (reset)	$\overline{RESET}$ = V_L		2.75	6		2.75	6	mA
C_i	Input capacitance	f = 1 MHz			5			5	pF
C_o	Output capacitance	f = 1 MHz			6			6	pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TACT2150-20		TACT2150-30		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A-M)}$	Access time from address to MATCH		20		30	ns
$t_{a(A-PL)}$	Access time from address to $\overline{PE}$ low		22		30	ns
$t_{a(A-PH)}$	Access time from address to $\overline{PE}$ high		30		35	ns
$t_{a(S-M)}$	Access time from $\overline{S}$ to MATCH		10		15	ns
$t_{p(D)}$	Propagation time, data inputs to MATCH		15		20	ns
$t_{p(R-MH)}$	Propagation time, $\overline{RESET}$ low to MATCH high		10		15	ns
$t_{p(S-MH)}$	Propagation time, $\overline{S}$ high to MATCH high		10		12	ns
$t_{p(W-MH)}$	Propagation time, $\overline{W}$ low to MATCH high		10		12	ns
$t_{p(W-PH)}$	Propagation time, $\overline{W}$ low to $\overline{PE}$ high		15		20	ns
$t_{v(A-M)}$	MATCH valid time after change of address	3		3		ns
$t_{v(A-P)}$	$\overline{PE}$ valid time after change of address	5		5		ns

timing requirements over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TACT2150-20		TACT2150-30		UNIT
		MIN	MAX	MIN	MAX	
$t_{w(RL)}$	Pulse duration, $\overline{RESET}$ low	35		40		ns
$t_{w(WL)}$	Pulse duration, $\overline{W}$ low, without writing $\overline{PE}$	20		25		ns
$t_{wPE(WL)}$	Pulse duration, $\overline{W}$ low, writing $\overline{PE}$ (see Note 3)	20		25		ns
$t_{su(A)}$	Address setup time before $\overline{W}$ low	0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ high	20		25		ns
$t_{su(P)}$	$\overline{PE}$ setup time before $\overline{W}$ high (see Note 3)	20		25		ns
$t_{su(S)}$	Chip select setup time before $\overline{W}$ high	20		25		ns
$t_{su(RH)}$	$\overline{RESET}$ inactive setup time before first tag cycle	0		0		ns
$t_{h(A)}$	Address hold time after $\overline{W}$ high	0		0		ns
$t_{h(D)}$	Data hold time after $\overline{W}$ high	0		0		ns
$t_{h(P)}$	$\overline{PE}$ hold time after $\overline{W}$ high	0		0		ns
$t_{h(S)}$	Chip select hold time after $\overline{W}$ high	0		0		ns
t_{AVWH}	Address valid to write enable high	20		25		ns

NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

PARAMETER MEASUREMENT INFORMATION

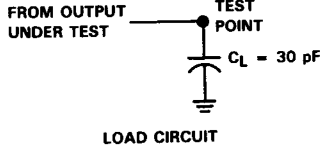


FIGURE 1. TOTEM-POLE OUTPUTS

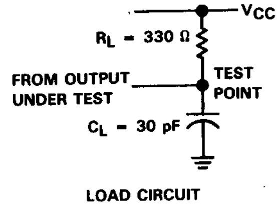
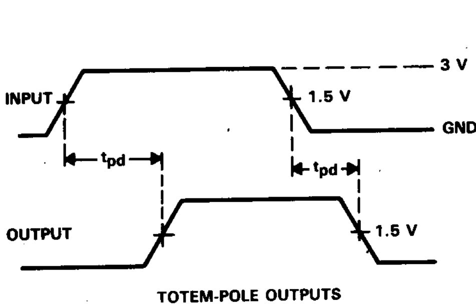


FIGURE 2. OPEN-DRAIN OUTPUTS



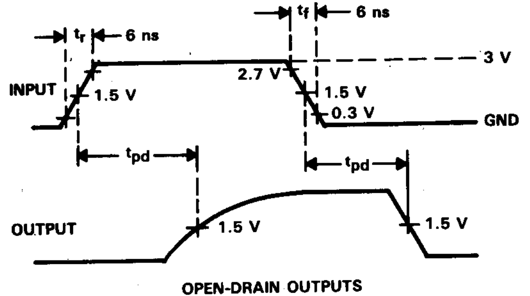


FIGURE 3. TIMING REFERENCE LEVELS

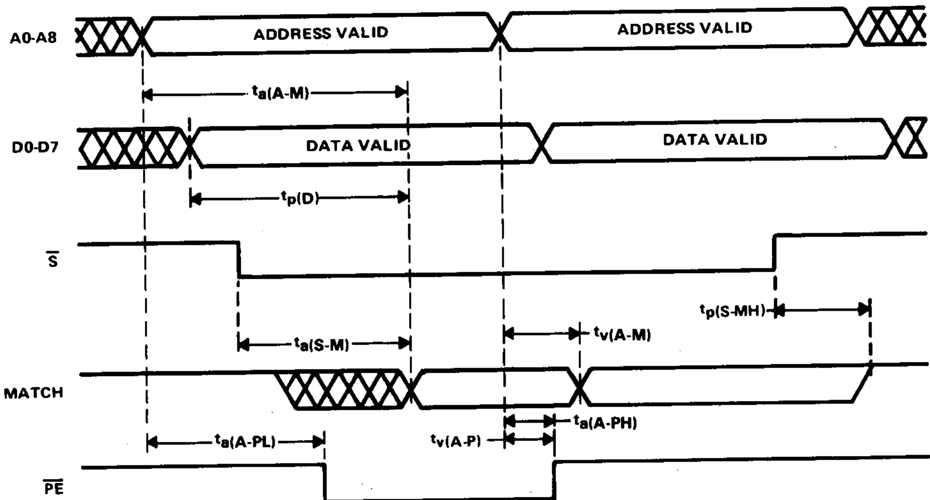


FIGURE 4. COMPARE CYCLE TIMING

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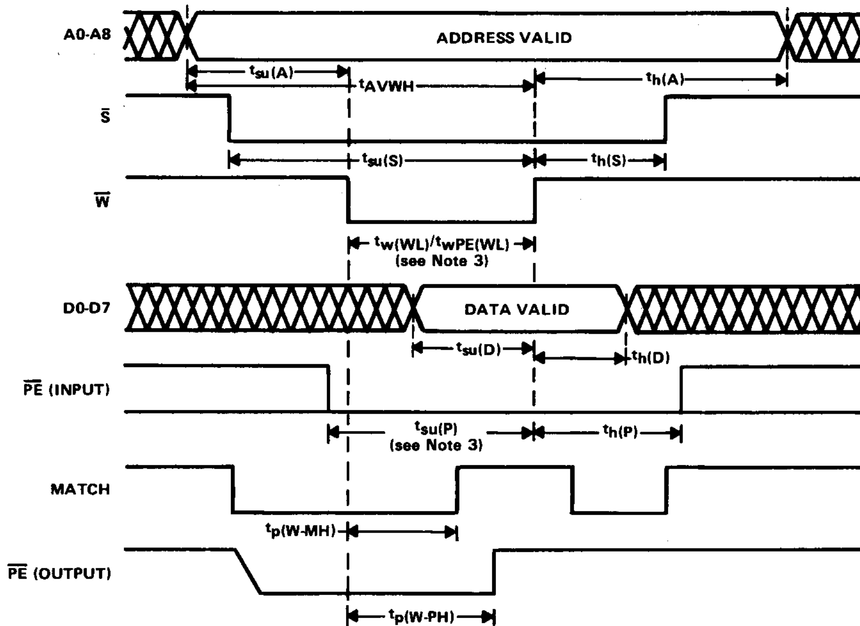
PARAMETER MEASUREMENT INFORMATION



NOTE 3: Parameters $t_{wPE(WL)}$ and $t_{su(P)}$ apply only during the write cycle time when writing a parity error, $t_{cPE(W)}$.

FIGURE 5. WRITE CYCLE TIMING

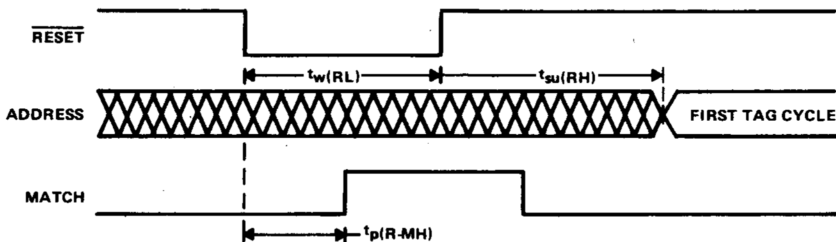


FIGURE 6. RESET CYCLE TIMING

Designing and Manufacturing Surface Mount Assemblies

T-90-20

Elizabeth Gunther, Charles Hutchins, and Paul Peterson

The competitive nature of the semiconductor industry has driven vendors to minimize the size of electronic components, so that more functions can be achieved in a given volume. In addition, improved electrical performance, decreased mass, and the potential for lower system cost are all by-products of compacted packaging and circuitry which hold interest to component manufacturers and users alike.

Surface Mount Technology (SMT) offers an excellent method of reducing component size. A typical memory array can be reduced to 50 percent of its original PWB size with single-sided mounting, and 25 to 30 percent with double-sided mounting. Logic designs cannot achieve the same dramatic reduction, but decreases up to 40 to 60 percent can be achieved for single-sided and double-sided assemblies respectively.

The key design and manufacturing process issues must be understood in order to fully reap the benefits of Surface Mount Technology. This article gives a general overview of the key aspects of design, process, and manufacturing of surface mounted assemblies, and offers surface mount as an opportunity to lower a system's cost without sacrificing reliability.

Components

Most surface mount components are at least one-third the size of the comparable through-hole mounted device (Figure 1). The 68-pin chip carrier is approximately one square inch, while the 64-pin DIP is approximately three square inches. The 20-pin chip carrier is slightly larger than 0.1 square inch, while the 20-pin DIP is 0.3 square inch. Similarly, other IC packages are reduced to approximately one-third the size of comparable lead count packages. The passive components occupy approximately one-tenth the board area, and this is why they have been used in most small consumer products built in the last couple of years.

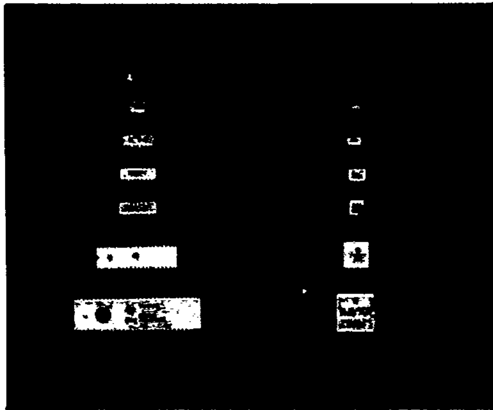


Figure 1. Component Site Reduction

There were many references in the recent past to problems with component availability, cost, and standardization. This area of SMT has probably received more attention than any other. Several recent magazine articles now state that significantly more components (particularly actives) are now available and that cost parity has been achieved on most of them. The effort by various industry committees on standardization has also been effective.

Thus, although more needs to be accomplished in these areas, a designer can begin a project with confidence that there will be no insurmountable barriers in this area. There are several consultants and subcontract assembly companies to assist in this effort. It is strongly recommended that all new designs utilize some form of SMT, particularly when space is an important consideration.

Process

The process to manufacture a surface mount assembly (SMA) is very simple. It consists of four basic steps, as shown in Figure 2. First, the solder paste is screened on the PWB. Then the component is placed on the board, with due care to get it positioned correctly. Typical geometries require placement accuracy of less than plus/minus 4 mils. Next the solder is reflowed with either a vapor phase or infrared system. Finally, the assembly is cleaned and is now ready for test. This process, although simple in concept, relies on board and component planarity and solderability. These are easily achievable with the chip carriers and memory modules we will discuss later.

Texas Instruments has installed a Surface Mount Technology Center at its plant in Houston, Texas. At this center, we have a complete and flexible engineering line to assist our customers in converting to Surface Mount Technology.

The engineering line is equipped with a screen printer, pick and place system, vapor phase reflow, and clean-up station that will easily handle PWBs up to 9″ × 10″. Larger boards up to 14″ × 16″ can be processed with some additional care. TI uses this engineering line to produce its prototype and demo boards. It is also available to any of TI's customers, free of charge, for use in building test or prototype boards.

The effectiveness of the assembly process can be characterized by the number of unacceptable solder joints formed during the process. Unacceptable joints are defined by their electrical and mechanical (strength and reliability) characteristics. The major problem is open solder joints, followed by bridging and misregistration.

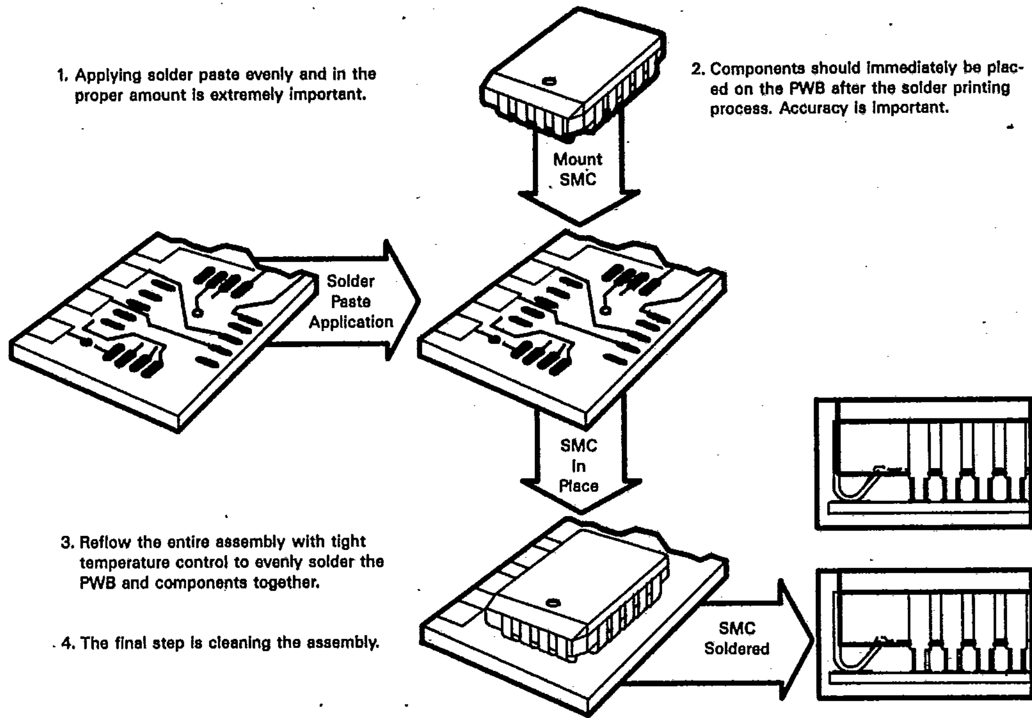


Figure 2. Basic Process Steps

Open circuits are detected at electrical test and are the first defects detected after soldering. At Texas Instruments, 10 PPM or less is the desirable defect level. Several factors that contribute to open solder joints were identified during production start-up. Lead tip planarity of the J-leaded plastic chip carriers is the most important factor in obtaining acceptable process yields. Lead position, lead finish, solder paste composition, and PWB solderability affect process yield as well.

Experiments in which lead tip planarity was confined to specific limits between 1 to 7 mils indicate that a 2 mil planarity requirement produces acceptable results with the process currently in use. Little gain in yield was noted at a 1 mil planarity requirement.

Another interesting result showed that silver in the process, either as a lead finish or in the solder paste, improves yields significantly. One explanation may have to do with the dynamics of the solder during the reflow process as they are affected by the different surface forces acting in the silver and non-silver process.

Design

The design of the PWB, in addition to providing the component interconnections, will provide the proper amount and correct placement of solder paste for a strong fillet formation. The wave soldering process, by comparison, provides a semi-infinite amount of solder, whereas the SMT process will provide only a predetermined amount. Thus, the component connection pad must be correctly placed and be of the proper size.

Further, consideration must be given for inspection, testing, and rework. The density achievable can lead to severe problems at these points if understanding and due care are not exercised in the design. The project team should include members from manufacturing, testing, QA, and purchasing, in addition to the design engineers, from the start. The design and processing of test boards is strongly recommended to provide experience and direction for the major project.

A very practical set of design guidelines is given in Figure 3. These have been used on a number of SMT designs and have given good results. With proper manufacturing techniques as described later, a high yield can be achieved. Component spacings should be approximately equal to the height of the tallest component. This allows an angle of 45 degrees for visual inspection of test probes.

Figure 4 shows the standard footprint for all Small Outline (SO) packages. The larger and more important fillet of an SO package is on the inside of the gull-wing lead. The solder pad, or land, should therefore be designed to extend slightly under the body of the package in order to optimize this fillet. From Table 1 we can see all packages have 50 mil centers with 25 mil spacings between lands. This allows the designer enough space to put traces between pads, and also reduces the occurrence of solder bridging of adjacent lands. Table 1 also summarizes the suggested land lengths and placement, depending on the terminal count of the SO. While not an absolute solution, these land sizes offer a conservative design solution that will meet most vendors' specifications and provide a mechanically and electrically sound solder joint.

- **Geometries**
  - **Trace Width/Space** — **8/8 MIL Min., 10/10 MIL Typ.**
  - **IC Lead Solder Pad Size** — **25 ± 5 MIL × 70 ± 10 MIL**
  - **Via Hole Size** — **20 MIL DIA**
  - **Via Pad Size** — **40 MIL DIA**
  - **Cap/Resistor Pad Size** — **W = MAX Dimensions of Component**; **L = 20 MIL Beyond Metallization, 10 MIL Inside Metallization**
- **Solder Mask** — **5 MIL Larger than IC/Component Pad**

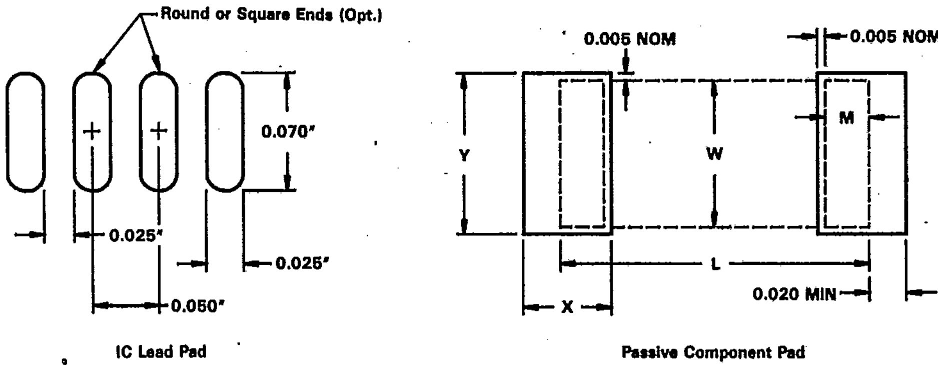


Figure 3. PWB Design Guidelines

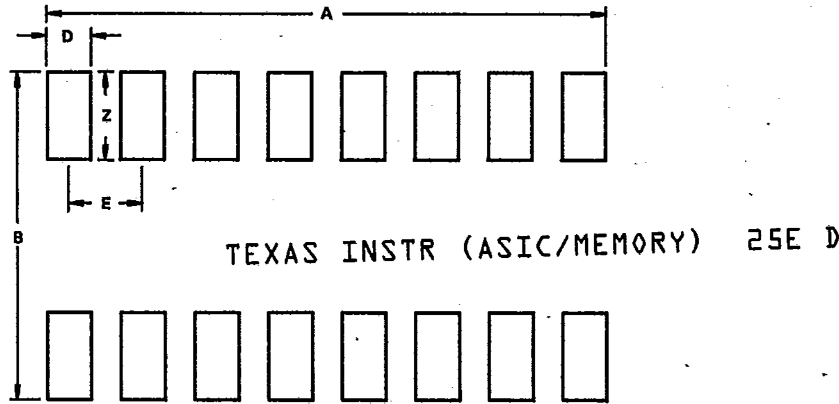


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Figure 4. Standard SOIC Footprint

Table 1. SOIC Footprint Dimensions

No. of Terminals	A	B	Z	D	E
8	.175	.250	.050	.025	.050
14	.325	.250	.050	.025	.050
16	.375	.250	.050	.025	.050
20	.475	.430	.070	.025	.050
24	.575	.430	.070	.025	.050

Test	4164A PLCC	4164 DIP	Units
Life Test, 125°C	42	64	Fits*—60% UCL
85°C/85% RH	0.17	0.37	%/1000 Hours
Autoclave	0.17	0.96	%/240 Hours
T/C−65/150	0.52	1.44	%/1000 Cycles
T/C 0/125	0.0	0.0	%/2000 Cycles

*Derated to 55°C Assuming 0.5EV Activation Energy

Figure 5. Failure Rate Comparison
4164A PLCC VS DIP

Manufacturing

The SMT manufacturing area must have the following basic equipment:

- Solder Paste Printer
- Component Pick and Place Machine
- Solder Paste Reflow Machine
- Clean-up System
- Inspection/Process Control Aids
- Electrical Test

The criteria for choosing the above is determined mainly by the size(s) and quantity of PWBs per month, the gross number of components per PWB, and the number of different components per PWB.

The size of the largest PWB is an important criterion in the choice of all of the major items. The printer, pick and place, reflow, and clean-up must all be able to handle it with no difficulty or process nonuniformity. The number and size of the various PWBs that may be produced will secondarily be considered for ease of set up and changeover in the printer and pick and place. The pick and place machine(s) will probably be the most expensive item in the list above and therefore, should get the most attention.

The gross number of components and PWBs will provide data for choosing the pick and place. Component per hour placement speed should be checked in actual operation, as the interrelationship may affect ultimate speed. The number of different components per board will determine how many feeders and what types of feeders will be required. This is a very key issue, as well as the accuracy of placement.

Reflow

The solder reflow is easily achieved with any of the commercially available equipment. Subtle differences between vapor phase, either batch or in-line, and infrared are overshadowed by the choice of solder paste and the solderability/planarity issue. A batch vapor phase is extremely flexible for different sizes of boards with different component counts. The in-line vapor phase is a good choice for a more automated processing line with standard or similar sized boards. The infrared has the advantage of being less expensive to operate, but requires more alteration to set up the time-temperature profile for a different size PWB. This would be a minimal problem on a manufacturing line building high volumes of the same board.

Clean-up

The most popular flux for SMT is the mildly activated rosin flux (RMA). This was developed in the days of vacuum tube assembly when clean-up was next to impossible. It is noncorrosive but provides sufficient fluxing action for good quality components and PWBs. Thus it is the preferred choice for SMAs with small spacings under most passives and SOICs, where complete cleaning is difficult. A mild solvent, such as Freon TMS, is generally sufficient to achieve a good visual cleanup, and there are several systems available that provide hot vapor, spray, or ultrasonic de-fluxing.

Reliability

With the smaller surface mount packages, there is some concern about component reliability. Texas Instruments addressed the overall DRAM reliability issue several years ago. Through an extensive task force effort, the major problems of the life test, humidity performance, and temperature cycle were identified. The best solutions to these problems required several changes in the design and process of the silicon chip. In doing so, the reliability of the DRAM chip became independent of the package used. Thus, the 64K DRAM in the plastic chip carrier package performs equivalently to the same chip in a DIP as shown in Figure 5. Similar data is available on most semiconductor ICs.

An additional reliability concern originates in the surface mount solder reflow process, which submits components to higher reflow temperatures more suddenly than the wave-soldering methods of DIP components, with oftentimes repeated reflow cycles for rework and repair.

The best method for resolving this issue involves comparing the temperature-time differential of the vapor phase or infrared solder reflow process to the standard temperature

cycling reliability tests to which surface mount components are routinely submitted. Figures 6 and 7 show temperature profiles of the vapor phase and infrared solder reflow processes. In the vapor phase process, the maximum temperature change with time is:

$$\frac{215°C - 25°C}{45 \text{ sec}} = \frac{190°C}{45 \text{ sec}}$$

equaling approximately 4°C/sec. The infrared solder reflow method submits the ICs to a similar, yet less severe temperature over time change of 3°C/second. Comparing these temperature profile ramp-ups to that which a surface mount component undergoes in a temperature cycling reliability test proves that there should be no concern over damage to the component during reflow. In the temp cycling test, the surface mount components were submitted to 1000 cycles of sudden cycling from 150°C to −65°C within three seconds. This represents a temperature-time differential of:

$$\frac{150°C-(-65°C)}{3} = \frac{215°C}{3 \text{ sec}} = \frac{70°C}{\text{sec}}$$

with less than 0.5 percent failures.

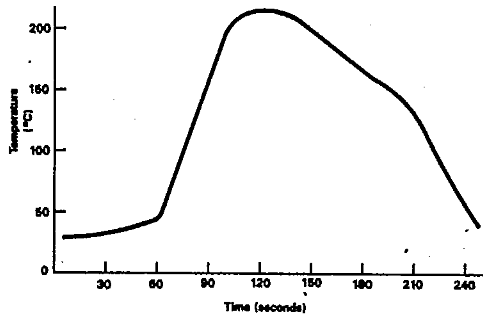

Figure 6. Typical Temperature Profile for In-Line Vapor Phase Reflow

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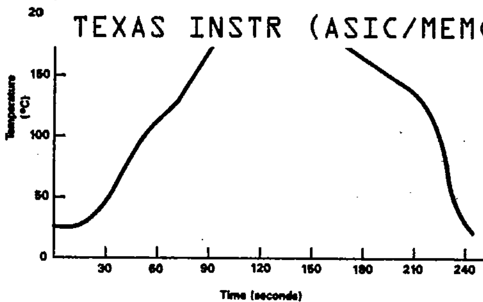

Figure 7. Typical IR Reflow System Profile

Since the surface mounted components were able to withstand a 70°C/second temperature change of 1000 cycles, they should be able to withstand the less severe conditions of a 4°C/second damage during reflow without reliability degradation.

Another concern in the solder reflow processing of surface mount components is the dwell time in reflow temperatures of 215°C or above. The dwell time for a small PWB populated with surface mount devices is about 20 seconds. For a larger board of about 10"×12" up to 50 seconds is needed for reflow. A generalized component degradation curve, relating accumulated time and temperature, can be assumed to exist. The shape of the curve for this discussion is assumed to be a decaying parabolic for simplicity and conservatism. There are two generally known points of this curve. The flame retardant mold compound (FRMC) of a plastic package starts to break down at 300°C in two to three seconds. Also, the molding and curing of a surface mount device is performed over several hours at 175°C. These two points are shown on the generalized curve shown in Figure 8, with the "safe" region being the area under the curve. Two points that fall within this region are the industry standard practice of solder dipping leads of several types of ICs, and of the soldering plastic devices on the bottom with Type III surface mount assembly, each submerges the component for three to four seconds in a solder wave.

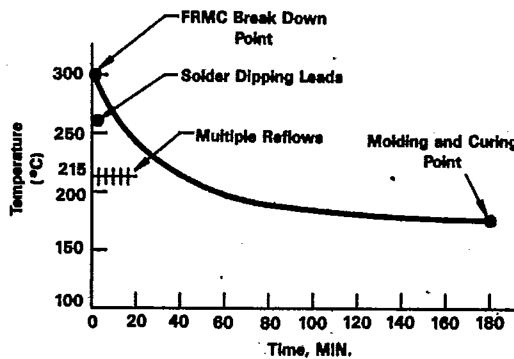

Figure 8. General Plastic Degradation Curve

Summary

Surface mount assembly techniques provide a significant advantage in cost, volume, and reliability over the current "thru-hole" technology. These are well documented, and the manufacturing equipment and related products are becoming readily available to support new production lines. Also, as experience grows, improved products and ideas are developed from the cooperative efforts of vendors and users in standardization organizations and in problem-solving sessions. The broad selection of package types and product technologies available now are sufficient to begin conversion of existing electronic system products for size reduction or feature enhancement. Definitely, new products should be designed with surface mount technology.