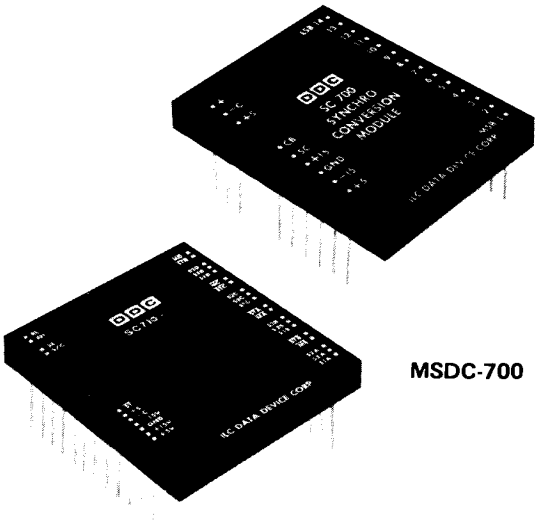
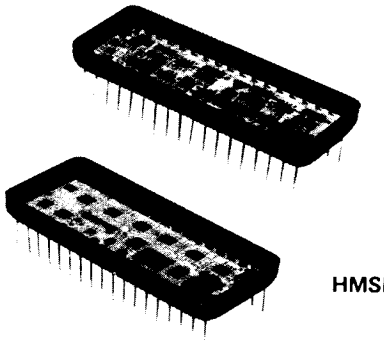
# MSDC-700/HMSDC-8700

## MULTIPLEXED 14 BIT S/D AND R/D CONVERTERS
## New Design Requires Fewer Modules




MSDC-700



HMSDC-8700

E

### DESCRIPTION

These two new series of multiplexed S/D and R/D converters are cost effective because they require fewer components and interconnections. Since each input module contains four signal channels, and the central converter is complete in one module, a 4 channel system can be made with only two modules. All common synchro and resolver line-to-line voltages and frequencies are available, and signal and reference input channels can be interconnected in any combination.

Discrete and hybrid modules can be used together because they are electrically interchangeable. Modules in the discrete MSDC-700 series are low profile (0.43 inch high) and low cost. They feature internal isolation transformers at both 60 Hz and 400 Hz. Modules in the hybrid HMSDC-8700 series have the small size, low weight, and high reliability of thick-film hybrids. They feature differential solid-state signal and reference inputs with substantial common mode rejection so that transformer isolation is not usually required.

### APPLICATIONS

Multiplexed S/D and R/D converters can be used when multiple synchro or resolver inputs are sampled for digital computation or display, and real time tracking is not required. Multiplexing is found in data logging systems, process monitors, ordnance aiming controls, navigation systems, numerical control, and range instrumentation. The synchro and resolver inputs often represent variables which are analyzed by a computer for monitoring or control.

*FEATURES*

- *SIMULTANEOUS SAMPLING AND RANDOM ACCESS*
- *SUPERIOR ALGORITHM GIVES INHERENTLY HIGH ACCURACY*
- *ONLY TWO TYPES OF MODULES 4 channel input module and central converter*
- *MODULES AVAILABLE IN DISCRETE OR HYBRID FORM*

## SPECIFICATIONS

**Apply over reference frequency, reference amplitude, temperature and power supply ranges; 10% signal amplitude variation; and up to 10% harmonic distortion in the reference.**

| PARAMETER | VALUE |
|---|---|
| **RESOLUTION** | 14 bits |
| **ACCURACY** | ±4.6 minutes ± 1/2 LSB |
| **DYNAMIC CHARACTERISTICS** | |
| Signal Sample Rate at Each Signal Input Channel | Once per cycle of the reference processor controlling that input channel. |
| Conversion Time, Per Channel | 120-150 μsec |
| Number of Conversions per Carrier Cycle | |
| At 400 Hz | 15 max |
| At 60 Hz | 100 max |
| Channel Access | Random, one address per line per channel |

**ANALOG INPUT CHARACTERISTICS FOR DISCRETE UNITS, MSDC-700**

| | | | |
|---|---|---|---|
| Input Type | Transformer isolation, both reference and signal inputs. Input impedance is maintained with power off. | | |
| Breakdown Voltage | 500V min to ground | | |
| Reference and Signal Characteristics | Min $Z_{IN}$ L-L (Balanced, Resistive) | Ref Input Voltage (±20%) | Min Ref $Z_{IN}$ (Resistive) |
| Synchro Input | | | |
| 11.8V L-L, 360–440 Hz (SC-710) | 19 KΩ | 26V rms | 40 KΩ |
| 90V L-L, 360–440 Hz (SC-711) | 148 KΩ | 115V rms | 160 KΩ |
| 90V L-L 47-440 Hz (SC-715) Reference 47-66 Hz | 148 KΩ | 115V rms | 160 KΩ |
| Resolver Input | | | |
| 11.8V L-L, 360-440 Hz (SC-712) | 26 KΩ | 26V rms | 40 KΩ |
| 26V L-L, 360-440 Hz (SC-713) | 57 KΩ | 26V rms | 40 KΩ |
| 90V L-L, 360-440 Hz (SC-714) | 198 KΩ | 115V rms | 160 KΩ |

**ANALOG INPUT CHARACTERISTICS FOR HYBRID UNITS, HMSDC-8700**

| | | | |
|---|---|---|---|
| Input Type | Differential solid state. Input impedance is maintained with power off. | | |
| Frequency Range* | 47–440 Hz | | |
| Reference Voltage Range | 10–150V RMS | | |
| Reference Input Impedance | Single ended: 1.5 MΩ min<br>Differential: 3 MΩ min. | | |
| Reference Common Mode Range | DC common mode plus recurrent AC peak: 210V max | | |
| Signal Input Minimum Impedance (Balanced, Resistive) | | | |
| Synchro* | $Z_{in}$ Line-to-Line | $Z_{in}$ Each Line to GND | |
| 11.8V L-L (SC-8710) | 17.5 KΩ | 11.5 KΩ | |
| 90V L-L (SC-8711) | 130 KΩ | 85 KΩ | |
| Resolver* | $Z_{in}$ Single Ended | $Z_{in}$ Differential | $Z_{in}$ Each Line to GND |
| 11.8V L-L (SC-8712) | 23 KΩ | 46 KΩ | 23 KΩ |
| 26V L-L (SC-8713) | 50 KΩ | 100 KΩ | 50 KΩ |
| 90V L-L (SC-8714) | 175 KΩ | 350 KΩ | 175 KΩ |
| Signal Common Mode Ranges | | | |
| For 90V L-L Input | 150V max } DC common mode plus recurrent AC peak | | |
| For 26V L-L Input | 50V max } | | |
| For 11.8V L-L Input | 25V max } | | |

*Other voltages and frequencies available — consult factory.

| PARAMETER | VALUE | | | |
|---|---|---|---|---|
| **DIGITAL INPUTS** | Input Type | Internal Pullup to +5V (min) | Std TTL Load (Includes Pullup) | Description |
| System Inputs | | | | |
| Start Convert (SC) | | | | 1–4μsec positive pulse; leading edge initiates conversion |
| Discrete (SC 700) | LS TTL | – | 0.2 | |
| Hybrid (SC 8700) | LS TTL | 27 KΩ | 0.4 | |
| Mux Select ($\overline{MA}$, $\overline{MB}$, $\overline{MC}$, $\overline{MD}$) | CMOS | 40 KΩ | 0.08 | Logic 0 selects channel; must start within 1 μsec of SC and remain until conversion is complete (CB=0) |
| Sample Enable (SE) | CMOS | 40 KΩ | 0.08 | Logic 0 inhibits sample time pulse (ST) from ref channel; ST resumes when SE returns to logic 1. |
| Sin/Cos Select (S/C) | CMOS | 40 KΩ | 0.08 | Switches cos output line on input module between cos output (logic 1) and sin output (logic 0); for interfaces not using central converter. |
| Interconnection Inputs | | | | |
| Sample Time Input ($\overline{STA}$, $\overline{STB}$, $\overline{STC}$, $\overline{STD}$) | CMOS | 40 KΩ | 0.08 | Gate control for sample/hold; connected by user to ST output from any ref channel. |
| + Input | LS TTL | 27 KΩ | 0.3 | Normally tied to +5V |

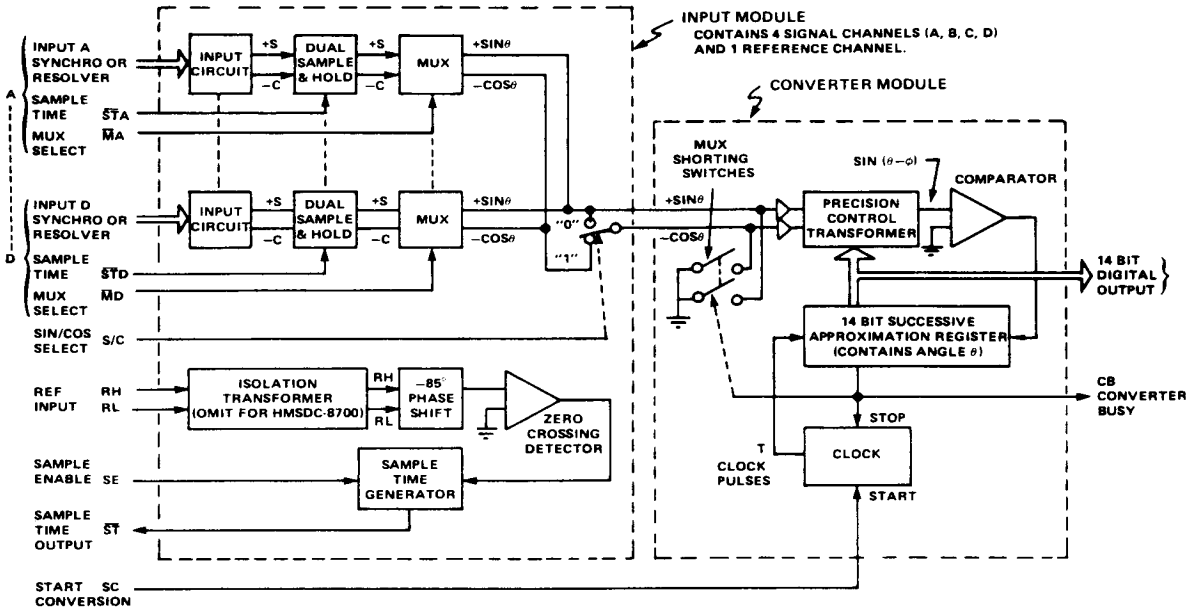
| DIGITAL OUTPUT | Output Type | Drive capab. STD TTL Loads | Description |
|---|---|---|---|
| System Outputs | | | |
| 14 Parallel Data Bits | LP TTL | 2 | Natural binary angle; positive logic |
| Converter Busy (CB) | CMOS | 2 | 150 μsec max; logic 1 during conversion |
| Interconnection Outputs | | | |
| Sample Time Output ($\overline{ST}$) | CMOS | 0.2 | Drives up to 8 sample/hold gates; connnected by user to ST inputs in any signal channel. Negative pulse, 50 μsec nominal, 40 μsec min, 70 μsec max. $\overline{ST}$ pulse is automatically initiated close to the positive peak in each ref cycle. |

| TEMPERATURE RANGES | |
|---|---|
| Operating | |
| –1 Option | –55°C to +105°C |
| –3 Option | 0°C to +70°C |
| Storage | |
| Discrete (MSDC-700) | –55°C to +125°C |
| Hybrid (HMSDC-8700) | –55°C to +135°C |

| POWER SUPPLIES | | | |
|---|---|---|---|
| Nominal Voltage (±5%) | +5 VDC | +15 VDC | –15 VDC |
| Max Voltage Without Damage | +7 VDC | +18 VDC | –18 VDC |
| Current in mA | | | |
| Central Converter | 58 nom | 9 nom | 8 nom |
| (SC700, SC8700) | 83 max | 15 max | 14 max |
| Input Modules | 3 nom | 15 nom | 14 nom |
| (SC710-715, SC8710-8714) | 5 max | 24 max | 23 max |

| PHYSICAL CHARACTERISTICS | |
|---|---|
| Discrete Units | |
| Type | Encapsulated module; each contains either a central converter or 1 ref plus 4 signal input channels. |
| Size, Each Module | 3.125 x 2.625 x 0.43 inch (7.94 x 6.67 x 1.09 cm) |
| Weight, Each Module | 4 oz. (114 g) |
| Hybrid Units | |
| Type | 36 pin double DIP; each module contains either a central converter or 1 ref plus 4 signal input channels. |
| Size, Each Module | 1.9 x 0.78 x 0.21 inch (4.83 x 1.98 x 0.53 cm) |
| Weight, Each Module | 1 oz. max (28 g) |

E




**BLOCK DIAGRAM**
**MSDC-700 AND HMSDC-8700**

## TECHNICAL INFORMATION

### INTRODUCTION AND BLOCK DIAGRAM

Each multiplexed system consists of one converter module and one or more signal input modules. The block diagram shows one input module connected to one converter module. The input module contains four signal input channels A, B, C, D and one reference input channel.

Each synchro or resolver is connected to a separate input channel, and each reference to a reference channel. In the discrete MSDC-700 series the input circuit is either a resolver isolation transformer or a Scott-T transformer. In the hybrid HMSDC-8700 series the input circuit is either a solid state buffer or a solid state Scott-T.

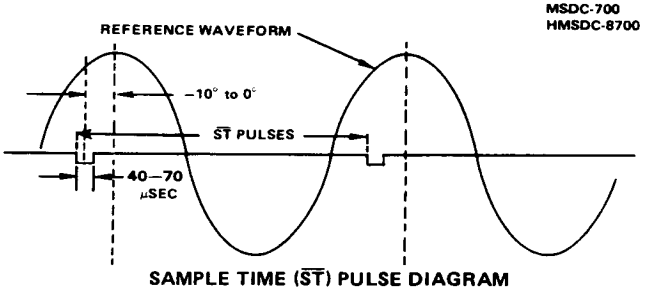
If several synchro or resolvers share a reference, they will also share a reference input channel. The purpose of the reference input channel is to produce the sample time pulse $\overline{ST}$. The $\overline{ST}$ output from each reference channel can be connected to the sample time inputs $\overline{STA}$. . . $\overline{STD}$ in up to 8 input channels. Each $\overline{ST}$ pulse causes the dual sample/holds to which it is connected to sample the synchro or resolver input in that channel.

The sample enable, SE, inhibits the sample time generator. If the SE is at logic 1, the sample time generator automatically produces an $\overline{ST}$ pulse near each positive peak of the reference waveform, as shown in the sample time pulse diagram. The synchro and resolver inputs connected to each reference are therefore sampled simultaneously once during each cycle, unless an SE pulse is applied. The $\overline{ST}$ pulse is inhibited only if the SE is at logic 0 at the moment the $\overline{ST}$ is initiated; once the $\overline{ST}$ begins, a subsequent SE drop to logic 0 will not affect the $\overline{ST}$ pulse completion.

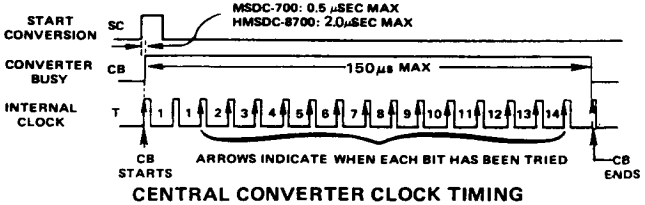
The outputs from each signal input circuit are nominally +4.1 sin $\theta$ sin $\omega t$ and −4.1 cos $\theta$ sin $\omega t$. These signals are sampled by the dual sample/hold at a time close to the positive peaks of the reference waveform. The dual sample/hold outputs are nominally +4.1 sin$\theta$ and −4.1 cos$\theta$. These outputs are muxed together to the central converter input. The MUX select lines $\overline{MA}$, $\overline{MB}$,...determine which of these outputs will be processed. The MUX shorting switches are operated automatically by the converter busy pulse to discharge the central converter muxed input lines between conversions.

The sin/cos select S/C was designed for situations in which the output from a signal module is processed not by a converter module, but by some other means such as a computer. By operating the S/C control, the sin$\theta$ and cos$\theta$ information can be muxed into one output line.

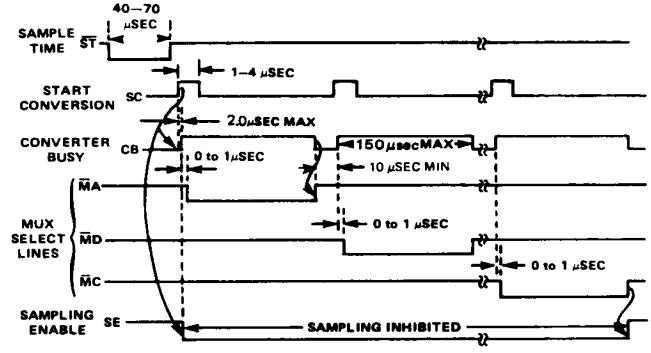
The −85° nominal phase shifter and the zero crossing detector in the reference channel detect the peak of the reference waveform. The 5° shift away from 90° compensates for a lead of approximately this amount which normally occurs between the signal output and reference input of a synchro or resolver.



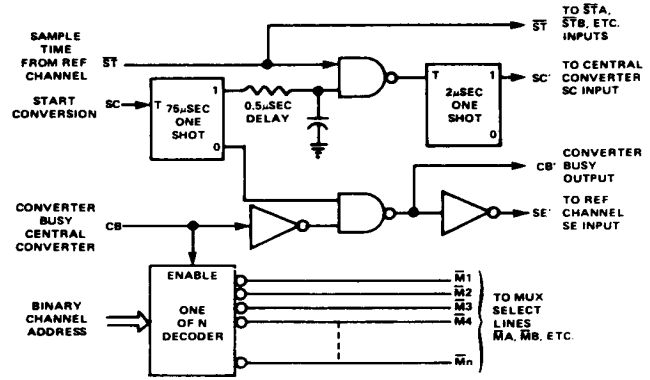

SAMPLE TIME ($\overline{ST}$) PULSE DIAGRAM




CENTRAL CONVERTER CLOCK TIMING




TIMING DIAGRAM




TIMING INTERLOCK CIRCUIT

## SYSTEM TIMING

Timing and control for the MSDC-700 and the HMSDC-8700 are depicted in the timing diagram. An SC pulse for converting data from any channel can be initiated at any time. The basic timing sequence is as follows:

1. Start conversion with an SC pulse. The leading edge of the SC pulse will cause a converter busy (CB) pulse to be generated, and the MUX shorting switches will open automatically during the CB pulse interval. 10 μsec min must elapse between trailing edge of CB and the leading edge of channel select.
2. Select the channel to be converted by driving any of the MUX select lines $\overline{MA}$, $\overline{MB}$,... to logic 0 within 1 μsec of the CB leading edge.
3. Drive the MUX select line back to logic 1 after the CB returns to logic 0.

This sequence is repeated for each conversion, with a minimum time interval of 10 μsec between the end of one CB and the start of the next SC.

Errors of a few LSBs can occur if a signal input is sampled while it is being converted. The following methods can be used to prevent simultaneous sampling and conversion:

1. Conversions can be timed to occur only between $\overline{ST}$ pulses. This is accomplished by interlocking the SC and the $\overline{ST}$ pulse with logic circuitry.
2. New $\overline{ST}$ pulses can be inhibited during conversions by keeping the SE at logic 0 until all conversions have been completed, as shown in the timing diagram. However, it is still necessary to avoid starting a conversion while sampling is in progress.

The timing interlock circuit shown will prevent simultaneous sampling and conversion. An SC input pulse first produces an SE to inhibit $\overline{ST}$ pulses. Then after a 0.5 μsec delay the SC input produces a start conversion pulse SC' only if there is no $\overline{ST}$ in progress. The SE pulse will remain low during the conversion process because of the interlock with the central converter CB. The one-of-N decoder is used to gate the MUX channel addresses with the CB. An SE input may be combined with the SE' to inhibit sampling between conversions.

The maximum number of conversions per carrier cycle may be calculated as follows:

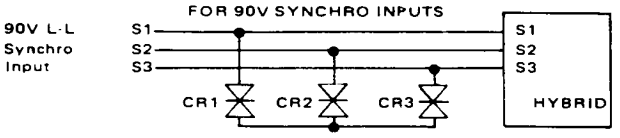
$$\text{Max no. of conversions/cycle} = \frac{\text{minimum period} - \text{max } \overline{ST} \text{ pulse time}}{\text{max CB pulse time} + 10\ \mu\text{sec}}$$

## SOLID STATE BUFFER INPUT PROTECTION (HMSDC-8700 ONLY)

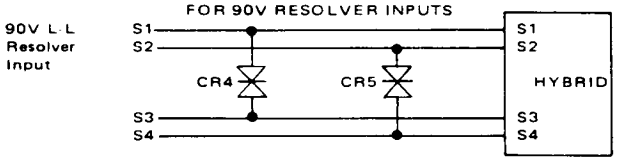
The solid state signal and reference inputs in the HMSDC-8700 input modules are true differential inputs with high AC and DC common mode rejection. Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage range should not exceed the following values:

| INPUT | COMMON MODE MAXIMUM | MAX TRANSIENT PEAK VOLTAGE |
|---|---|---|
| 11.8V L-L | 25V Peak | 150V |
| 26V L-L | 50V Peak | 150V |
| 90V L-L | 150V Peak | 350V |
| Reference | 210V Peak | 1000V |

90V line-to-line systems generally have voltage transients which exceed the 350V specification listed above. These transients can destroy the thin film input resistor network in the hybrid. Therefore, 90V L-L solid state input modules should always be protected by installing voltage suppressors as shown. Voltage transients are likely to occur whenever synchro or resolver voltages are switched on or off.




CR1, CR2 and CR3 are SA85C, 100V bi-polarity transient voltage suppressors or equivalent.

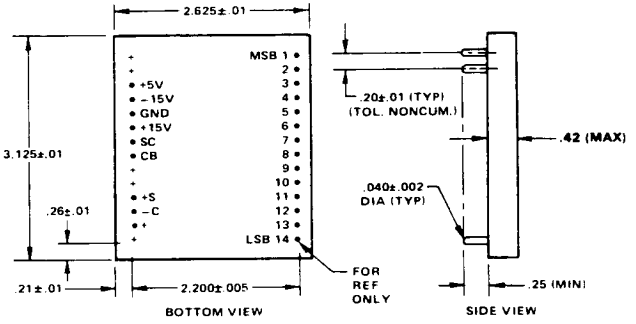



CR 4 and CR5 are 1N6137, 200V bi-polarity transient voltage suppressors or equivalent.

**CONNECTIONS FOR VOLTAGE TRANSIENT SUPPRESSORS**

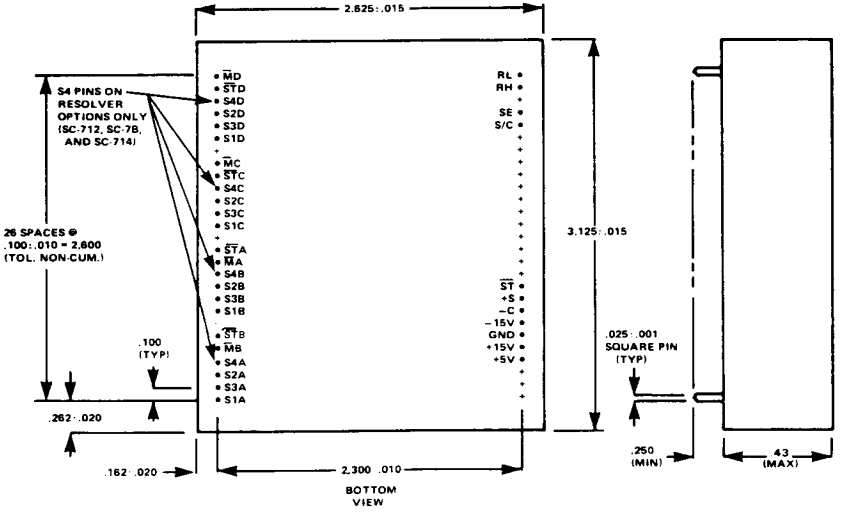
## MECHANICAL OUTLINES FOR DISCRETE MODULES

### 1. CENTRAL CONVERTER: SC-700




Notes:
1. Pin material is electrosoldered brass per MIL-F-14072, M222.
2. Case material is glass filled Diallyl Phthalate per MIL-M-14.

### 2. SIGNAL INPUT MODULES: SC-710 TO SC-715




Notes:
1. Case in glass filled Diallyl Phthalate per MIL-M-14
2. Pin material is 3/4 hard phosphor bronze per ASTM Type 1 B159-606
3. Pin plating is .00015 min acid tin per MIL-T-10727A

## RELIABILITY

The use of MSI and thin film resistor networks, as well as careful thermal design, results in very high MTBF values. Summaries of MTBF calculations are available on request.

## PIN CONNECTION TABLES FOR HYBRID MODULES

### 1. PIN CONNECTION TABLE FOR CENTRAL CONVERTER: SC-8700

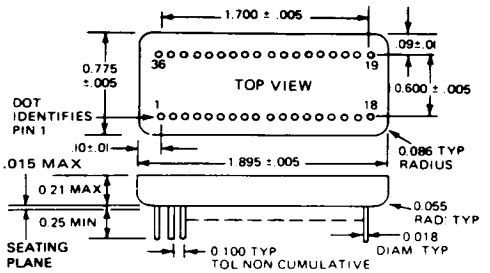
| Pin | Name | Description | Pin | Name | Description |
|---|---|---|---|---|---|
| 1 | B1 | 14 Bit Outputs | 20 | -C | -COS input. Connect to -C outputs on all input modules. |
| 2 | B2 | | | | |
| 3 | B3 | | | | |
| 4 | B4 | | 21 | +S | +SIN input. Connect to +S outputs on all input modules. |
| 5 | B5 | | | | |
| 6 | B6 | | | | |
| 7 | B7 | | 22 | CB | Converter busy output |
| 8 | B8 | | 23 | SC | Start conversion input |
| 9 | B9 | | 24 | TP4 | (+5.6) Factory test point |
| 10 | B10 | | 25 | TP6 | (e) Factory test point |
| 11 | B11 | | 26 | NC | No connection |
| 12 | B12 | | 27 | + | No connection if unused |
| 13 | B13 | | 28 | NC | No connection |
| 14 | B14 | | 29 | TP8 | Factory test point |
| 15 | NC | No connection | 30 | TP9 | (T) Factory test point |
| 16 | TP1 | (+BC) Factory test points | 31 | +5V | Power supply connections |
| 17 | TP3 | (-BS) Factory test points | 32 | -15V | Power supply connections |
| 18 | TP2 | (-BC) Factory test points | 33 | TP7 | (E) Factory test point |
| 19 | AG | Analog GND (Must be connected to pin 34) | 34 | GND | Power supply and logic GND |
| | | | 35 | TP5 | Factory test point |
| | | | 36 | +15V | Power supply connection |

### 2. PIN CONNECTION TABLE FOR INPUT MODULES: SC-8710 TO SC-8714

| Pin | Name | Description | Pin | Name | Description |
|---|---|---|---|---|---|
| 1 | S1A | Synchro or resolver input A. S4 for resolver only. | 21 | NC | No connection |
| 2 | S3A | | 22 | +5V | Power supply connections |
| 3 | S4A | | 23 | -15V | |
| 4 | S2A | | 24 | GND | |
| 5 | S1B | Synchro or resolver input B. S4 for resolver only. | 25 | +15V | |
| 6 | S3B | | 26 | $\overline{STD}$ | Sample time inputs and MUX select lines for inputs A, B, C, and D. Connect sample time inputs to any appropriate ST output. |
| 7 | S4B | | 27 | $\overline{MD}$ | |
| 8 | S2B | | 28 | $\overline{STC}$ | |
| 9 | S1C | Synchro or resolver input C. S4 for resolver only. | 29 | $\overline{MC}$ | |
| 10 | S3C | | 30 | $\overline{MB}$ | |
| 11 | S4C | | 31 | $\overline{STB}$ | |
| 12 | S2C | | 32 | $\overline{STA}$ | |
| 13 | S1D | Synchro or resolver input D. S4 for resolver only. | 33 | $\overline{MA}$ | |
| 14 | S3D | | 34 | +S | +SIN output. Connect to +S input on central converter module. |
| 15 | S4D | | | | |
| 16 | S2D | | | | |
| 17 | RH | Ref input high | 35 | -C | -COS output. Connect to -C input on central converter module. |
| 18 | RL | Ref input low | | | |
| 19 | SE | Sample enable input. No connection if unused. | 36 | S/C | SIN/COS select input. No connection if unused. |
| 20 | $\overline{ST}$ | Sample time output. Connect to sample time inputs on any module. | | | |

D

## MECHANICAL DIAGRAM FOR ALL HYBRID MODULES (SC 8700, SC 8710 – SC 8714)




PACKAGE IS KOVAR WITH ELECTROLESS NICKEL PLATING
PINS ARE KOVAR WITH GOLD PLATING (50 μINCH MIN)
CASE IS ELECTRICALLY FLOATING

## ORDERING INFORMATION

Each module required is specified separately. Modules are called out with temperature range as follows:

SC 8710 – 1 – 883B

- Reliability Grade: (Applies to hybrid modules only.)
  - 883B = Fully compliant with MIL-STD-883.
  - B = Screened to MIL- STD-883 but without QCI testing.
  - Blank = Standard DDC procedures.
- Temperature Range (Operating):
  - 1 = −55°C to +105°C
  - 3 = 0°C to +70°C
- Module Number:
  - 700 Series = Discrete encapsulated modules
  - 8700 Series = Hybrid modules

Each system requires the following:

1. Central Converter. Order one of the following:
   - Discrete: SC 700.
   - Hybrid: SC-8700
2. Signal Input Module. Order one or more of the following:

| Input Type | L-L Voltage | Discrete Module No. | Discrete Frequency | Hybrid Module No. | Hybrid Frequency |
|---|---|---|---|---|---|
| Synchro | 11.8V | SC 710 | 360-440 Hz | SC 8710 | 47-440 Hz |
| Synchro | 90V | SC 711 | 360-440 Hz | SC 8711 | 47-440 Hz |
| Synchro | 90V | SC-715* | 47-440 Hz | – | – |
| Resolver | 11.8V | SC 712 | 360-440 Hz | SC 8712 | 47-440 Hz |
| Resolver | 26V | SC 713 | 360-440 Hz | SC 8713 | 47-440 Hz |
| Resolver | 90V | SC 714 | 360-440 Hz | SC 8714 | 47-440 Hz |

*The SC-715 module may be used at 400 Hz by interconnecting the SC-711 sample time outputs ($\overline{ST}$) to the desired SC-715 sample time inputs ($\overline{STA}$, $\overline{STB}$, $\overline{STC}$ and $\overline{STD}$).