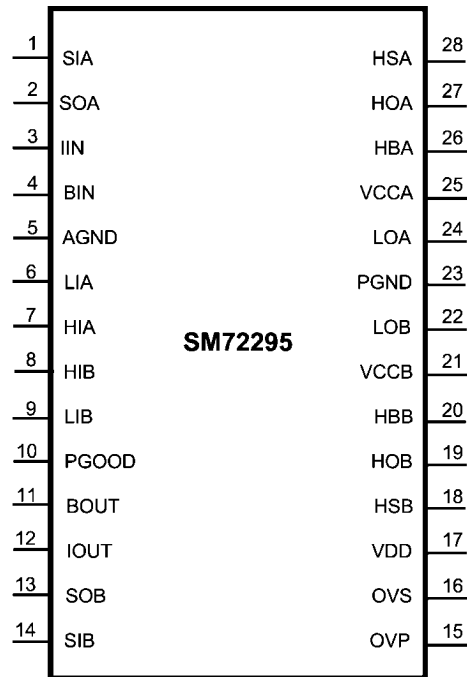


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Connection Diagram



30134116

Top View
SOIC-28

Ordering Information

Order Number	Description	NSC Package Drawing	Supplied As	Package Top Mark
SM72295MAX	28L SOIC WIDE	M28B	1000 Units in Tape and Reel	S72295
SM72295MAE	28L SOIC WIDE	M28B	250 Units in Tape and Reel	S72295
SM72295MA	28L SOIC WIDE	M28B	26 Units in Rail	S72295

Pin Descriptions

Pin	Name	Description	Application Information
1	SIA	Sense high input for input current sense transconductance amplifier	Tie to positive side of the current sense resistor through an external gain programming resistor (RI). Amplifier transconductance is 1/RI.
2	S0A	Sense low input for input current sense transconductance amplifier	Tie to negative side of the current sense resistor through an external gain programming resistor. Amplifier transconductance is 1/RI.
3	IIN	Output for current sense transconductance amplifier	Output of the input current sense amplifier. Requires an external resistor to ground (RL). Gain is RL/RI, where RI is the external resistor in series with the SIA pin.
4	BIN	Buffered IIN	Buffered IIN.
5	AGND	Analog ground	Ground return for the analog circuitry. Tie to the ground plane under the IC
6, 9	LIA, LIB	Low side driver control input	The inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
7, 8	HIA, HIB	High side driver control input	The inputs have TTL type thresholds. Unused inputs should be tied to ground and not left open.
10	PGOOD	Power good indicator output	Open drain output with an internal pull-up resistor to VDD indicating VCC is in regulation. PGOOD low implies VCC is out of regulation.
11	BOUT	Buffered IOOUT	Buffered IOOUT.
12	IOOUT	Output for current sense comparator.	Output of the output current sense amplifier. Requires an external resistor to ground (RL). Gain is RL/RI, where RI is the external resistor in series with the SIB pin.
13	S0B	Sense low input for output current sense amplifier	Tie to negative side of the current sense resistor through an external gain programming resistor. Amplifier transconductance is 1/RI.
14	SIB	Sense high input for output current sense amplifier	Tie to positive side of the current sense resistor through an external gain programming resistor (RI). Amplifier transconductance is 1/RI.
15	OVP	Over voltage indicator output	Open drain output with an internal pull-up resistor to VDD indicating OVS >VDD. OVP is low when OVS >VDD.
16	OVS	Sense input for over voltage	Requires an external resistor divider. VDD is the reference voltage.
17	VDD	3.3V or 5V regulator output	Bypass with 0.1uF. Reference for over voltage shutdown and IOOUT/IIN clamp
18, 28	HSA, HSB	High side MOSFET source connection	Connect to bootstrap capacitor negative terminal and the source of the high side MOSFET.
19, 27	HOA, HOB	High side gate driver output	Connect to gate of high side MOSFET with a short low inductance path.
20, 26	HBA, HBB	High side gate driver bootstrap rail.	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal to HS. The bootstrap capacitor should be placed as close to IC as possible.
21, 25	VCCA, VCCB	Positive gate drive supply	Locally decouple to PGND using low ESR/ESL capacitor located as close to IC as possible.
22, 24	LOA, LOB	Low side gate driver output	Connect to the gate of the low side MOSFET with a short low inductance path.
23	PGND	Power ground return	Ground return for the LO drivers. Tie to the ground plane under the IC

Absolute Maximum Ratings *(Note 1)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VCCA, VCCB	-0.3 to 14V
VDD	-0.3 to 7V
HBA to HSA, HBB to HSB	-0.3 to 15V
LIA, LIB, HIA, HIB, OVS	-0.3 to 7V
LOA, LOB	-0.3 to VCC+ 0.3V
HOA, HOB	HS-0.3 to HB + 0.3V
SIA, SOA, SIB, SOB	-0.3 to 100V
SIA to SOA, SIB to SOB	-0.8 to 0.8V
HSA, HSB (note 5)	-5 to 100V
HBA, HBB	115V
PGOOD, OVP	-0.3 to VDD
IIN, IOUT	-0.3 to VDD

BIN, BOUT	-0.3 to VDD
Junction Temperature	150°C
Storage Temperature Range	-55°C to +150°C
ESD Rating	
Human Body Model	2 kV

Recommended Operating Conditions

VCCA, VCCB	+8V to +14V
VDD	+3V to 7V
SI, SO common mode	VDD+1V to 100V
HS (Note 5)	-1V to 100V
HBA, HBB	HS+7V to HS+14V
HS Slew Rate	<50V/ns
Junction Temperature	-40°C to +125°C

Electrical Characteristics Specifications in standard typeface are for $T_j = 25^\circ\text{C}$, and those in boldface type apply over the full operating junction temperature range. No load on LO & HO, VCC = 10V, VDD = 5V, HB-HS = 10V, OVS = 0V unless otherwise indicated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SUPPLY CURRENTS						
I_{DD}	VDD Quiescent Current	SIA = SOB, SIB = SOB.		25	40	μA
I_{CC}	VCC Quiescent Current (ICCA+ICCB)	All outputs off		500	800	μA
I_{CCO}	VCC Operating Current (ICCA+ICCB)	LOA & LOB switching at 200kHz		2.2	3	mA
I_{HB}	HBA, HBB Quiescent Current	All outputs off		55	200	μA
I_{HBO}	HBA, HBB Operating Current	HOA & HOB switching at 200kHz		700	1000	μA
I_{HBS}	HBA & HBB to V_{SS} Current, Quiescent	HS = 100V, HB = 110V		0.1	10	μA
I_{HBSO}	HBA and HBB to V_{SS} Current, Operating	f = 200kHz		130		μA
PGOOD, OVB OUTPUTS						
V_{OL}	Output Low RDS			25	50	Ω
R_{PU}	VDD pull up resistor			50	90	k Ω
LI, HI INPUT PINS						
V_{IL}	Input Voltage Threshold		1.3	1.8	2.3	V
V_{IHYS}	Input Voltage Hysteresis			50		mV
R_I	LI, HI Pull down Resistance		100	200	400	k Ω
OVER VOLTAGE SHUTDOWN						
V_{OVR}	OVS Rising Threshold		VDD-50mV	VDD	VDD+50mV	V
V_{OVH}	OVS threshold Hysteresis			5%		VDD
I_{OVS}	OVS input bias current	OVS < VDD		1		nA
UNDER VOLTAGE SHUTDOWN						
V_{CCR}	VCC Rising Threshold		6	6.9	7.4	V
V_{CCH}	VCC threshold Hysteresis			0.5		V
V_{HBR}	HB-HS Rising Threshold		5.7	6.6	7.1	V
V_{HBH}	HB-HS Threshold Hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DH}	High-Current Forward Voltage	$I_{VCC-HB} = 100\text{mA}$		0.8	1	V
R_D	Dynamic Resistance	$I_{VCC-HB} = 100\text{mA}$		1	1.65	Ω

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LO & HO GATE DRIVER						
V_{OL}	Low-Level Output Voltage	$I_{LO} = 100\text{mA}$ $V_{OL} = \text{LO-PGND or HO-HS}$		0.16	0.4	V
V_{OH}	High-Level Output Voltage	$I_{LO} = -100\text{mA}$ $V_{OH} = \text{VCC-LO or VCC-HO}$		0.28	0.6	V
I_{OHL}	Peak Pullup Current	HO, LO = 12V		3		A
I_{OLL}	Peak Pulldown Current	HO, LO = 0V		3		A
t_{LPHL}	LO Turn-Off Propagation Delay	LI Falling to LO Falling		22		ns
t_{LPLH}	LO Turn-On Propagation Delay	LI Rising to LO Rising		26		ns
t_{HPHL}	HO Turn-Off Propagation Delay	HI Falling to HO Falling		22		ns
t_{HPLH}	HO Turn-On Propagation Delay	HI Rising to HO Rising		26		ns
t_{MON}	Delay Matching: LO on & HO off			1		ns
t_{MOFF}	Delay Matching: LO off & HO on			1		ns
t_{RC}, t_{FC}	Either Output Rise/Fall Time	$C_L = 1000\text{pF}$		8		ns
t_{PW}	Minimum Input Pulse Width that Changes the Output			50		ns
t_{BS}	Bootstrap Diode Turn-On or Turn-Off Time	$I_F = 100\text{mA} / I_R = 100\text{mA}$		37		ns
CURRENT SENSE AMPLIFIER						
V_{OS}	Offset voltage	$R_{SI} = R_{SO} = 500, 10\text{mV}$ sense resistor voltage	-2		2	mV
Gain 5mV	Gain is programmed with external resistors $I_{OUT}, I_{IN} = (R_L/R_{SI}) * (SI-SO)$	5mV sense resistor voltage $R_{SI} = R_{SO} = 1000, R_L = 75\text{K}$		390		mV
Gain 50mV	Gain is programmed with external resistors $I_{OUT}, I_{IN} = (R_L/R_{SI}) * (SI-SO)$	50mV sense resistor voltage $R_{SI} = R_{SO} = 1000, R_L = 75\text{K}$		3.85		V
Vclamp	Output Clamp	0.1V sense resistor voltage $R_{SI} = R_{SO} = 1000, R_L = 75\text{K}$		VDD		V
CURRENT SENSE BUFFER						
	Offset voltage (BIN-IIN), (BOUT-IOUT)	$I_{IN} = 2.5\text{V}$	-60		60	mV
	Output low voltage BOUT, BIN	$I_{IN}, I_{OUT} = 0$	0		50	mV
	Output high voltage BOUT, BIN	$I_{IN}, I_{OUT} = \text{VDD}$	VDD-100mV	VDD-30mV	VDD	mV
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	SOIC-28 (<i>Note 3</i>)		60		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

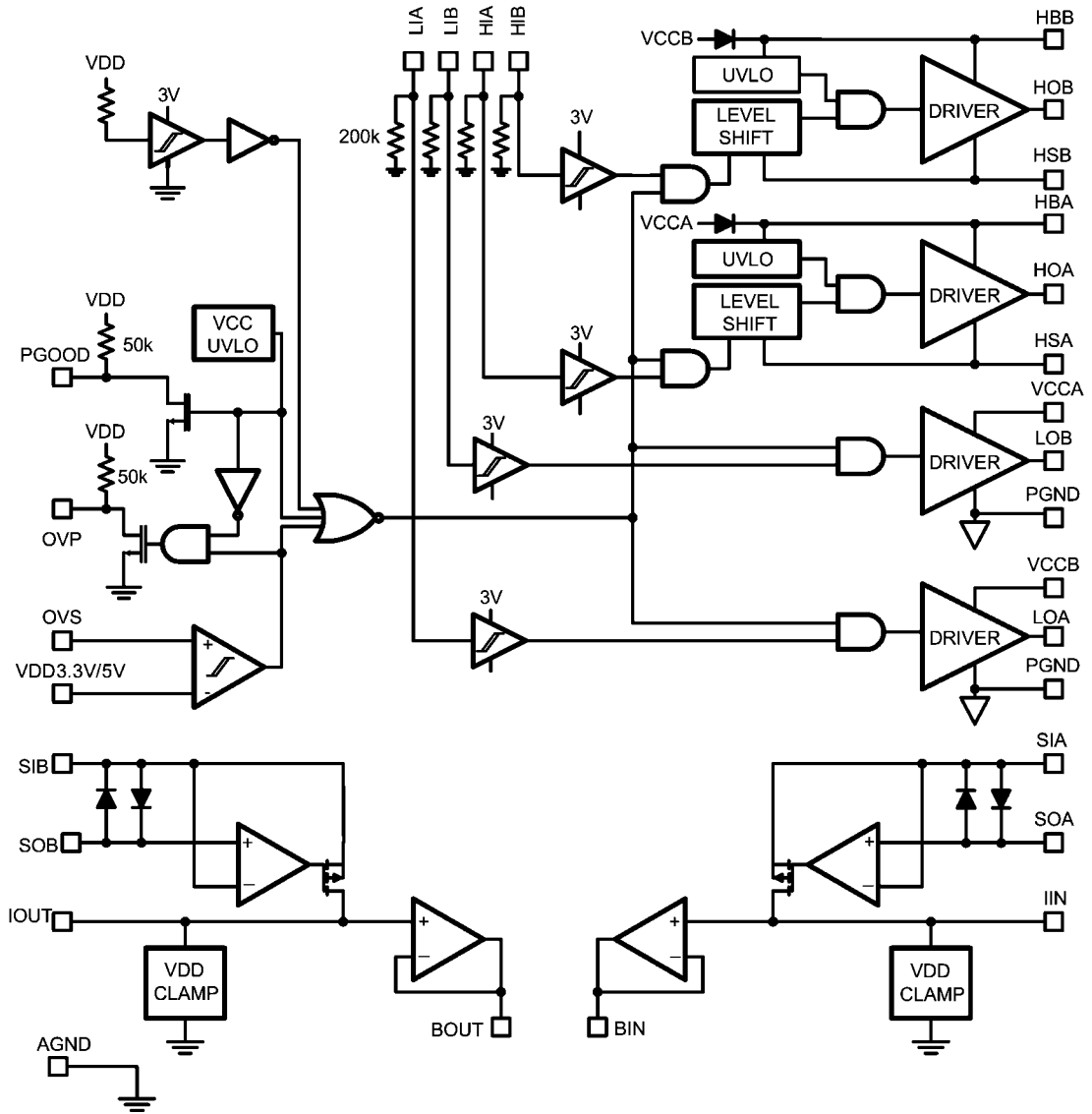
Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. 2 kV for all pins except HB, HO & HS which are rated at 1000V.

Note 3: 2 layer board with 2 oz Cu using JEDEC JESD51 thermal board.

Note 4: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 5: In the application the HS nodes are clamped by the body diode of the external lower N-MOSFET, therefore the HS node will generally not exceed -1V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur, the HS voltage must never be more negative than VCC-15V. For example if VCC = 10V, the negative transients at HS must not exceed -5V.

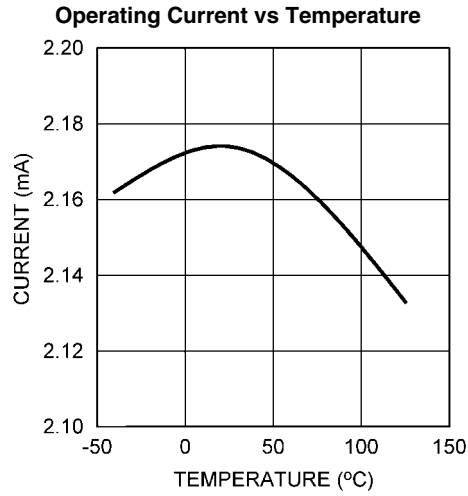
Block Diagram



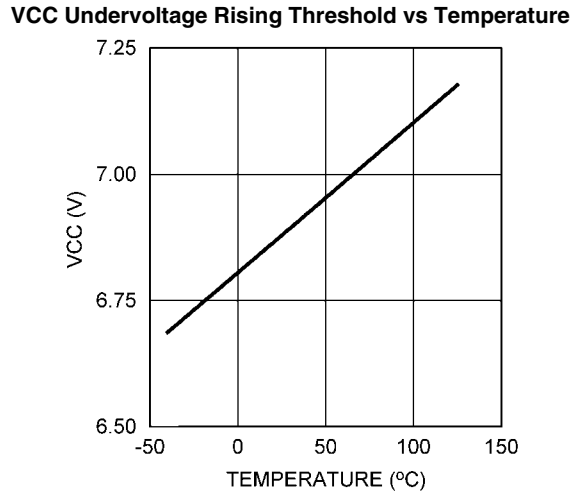
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FIGURE 1. Block Diagram

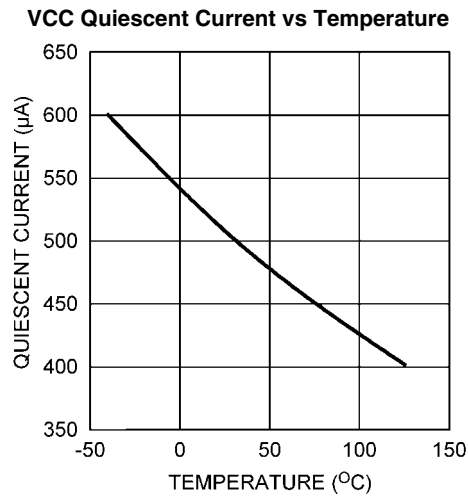
Typical Performance Characteristics



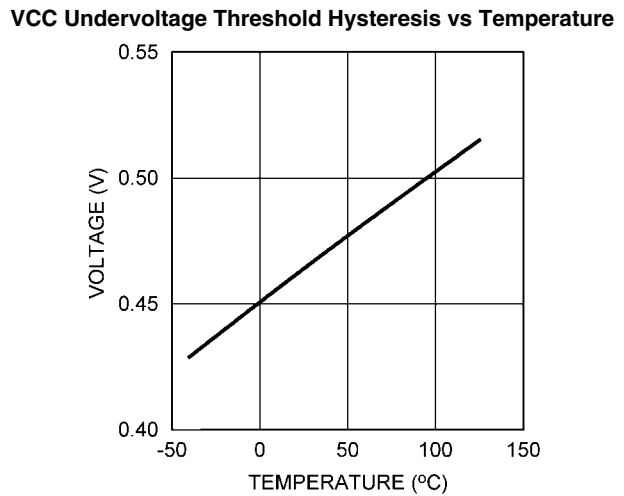
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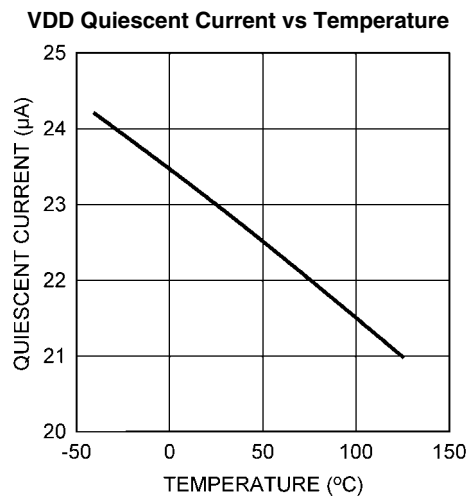
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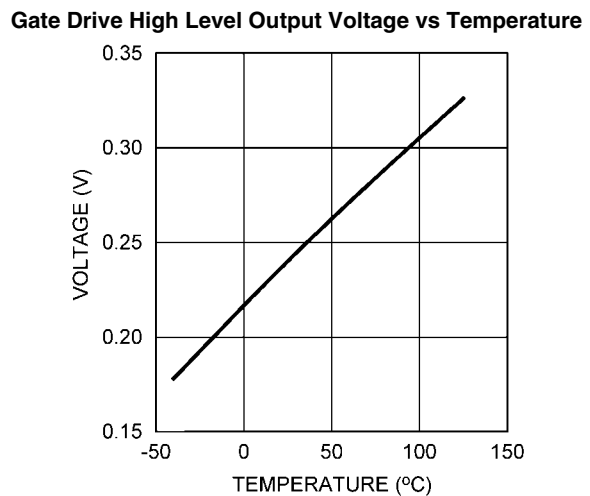
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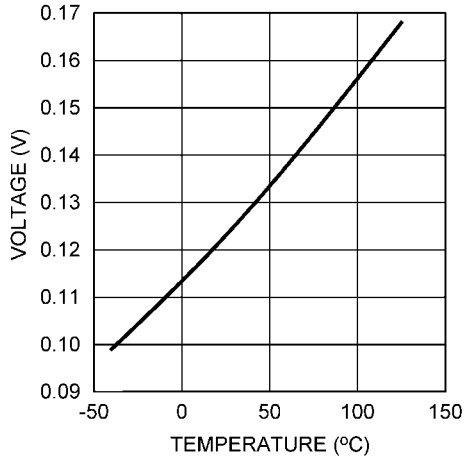


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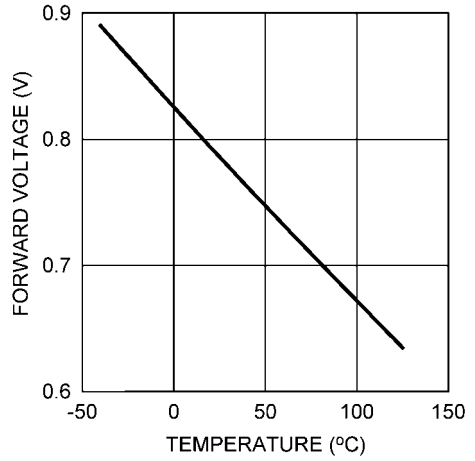
30134109

Gate Drive Low level Output Voltage vs Temperature



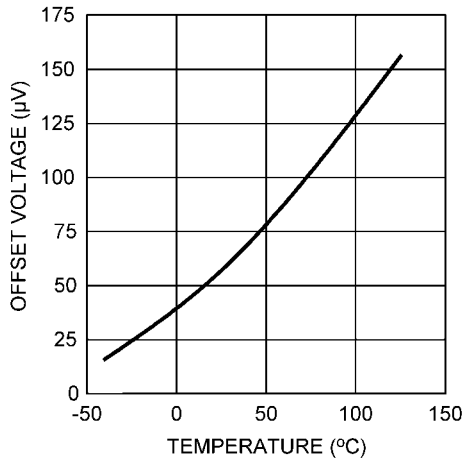
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Bootstrap Diode Forward Voltage vs Temperature



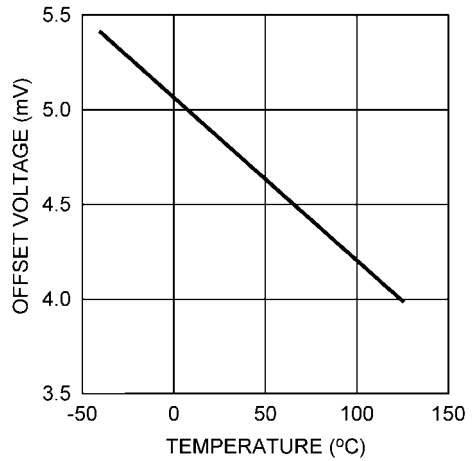
30134106

Current Sense Amplifier Input Offset Voltage vs Temperature



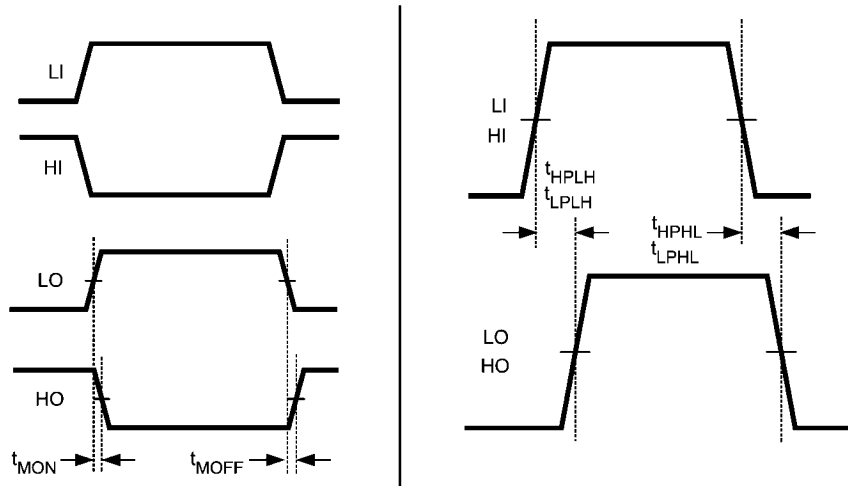
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Current Sense Amplifier Output Buffer Offset Voltage vs Temperature



30134108

Timing Diagram



30134103

FIGURE 2.

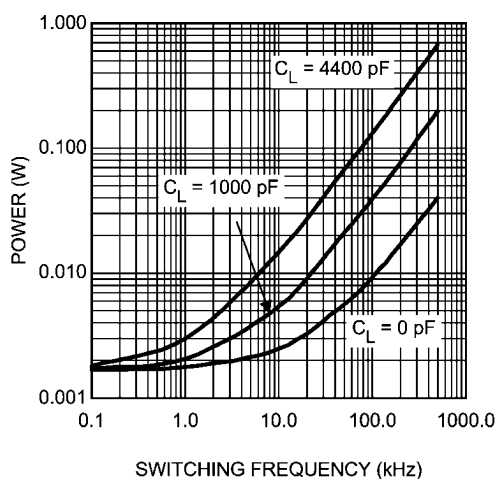
Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated as:

$$P_{DGATES} = 2 \cdot f \cdot C_L \cdot V_{DD}^2$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. The following plot shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the above equation. This plot can be used to approximate the power losses due to the gate drivers.

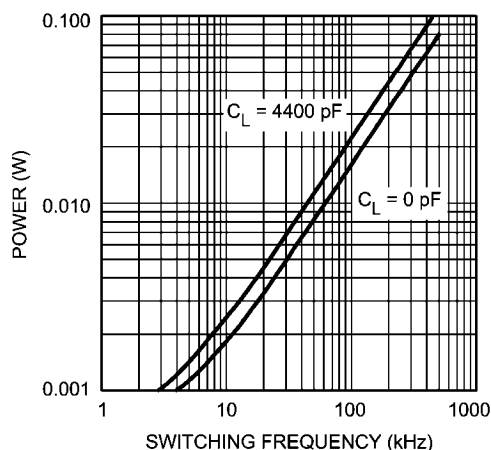
Gate Driver Power Dissipation (LO + HO)
 $V_{CC} = 12V$, Neglecting Diode Losses



30134104

The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to frequency. Larger capacitive loads require more current to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge result in higher reverse recovery losses. The following plot was generated based on calculations and lab measurements of the diode recovery time and current under several operating conditions. This can be useful for approximating the diode power dissipation. The total IC power dissipation can be estimated from the previous plots by summing the gate drive losses with the bootstrap diode losses for the intended application.

Diode Power Dissipation $V_{IN} = 50V$



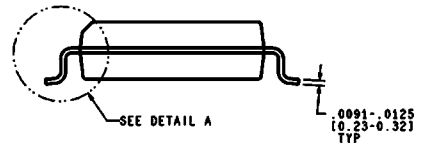
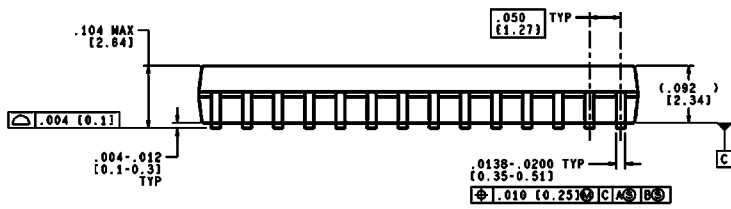
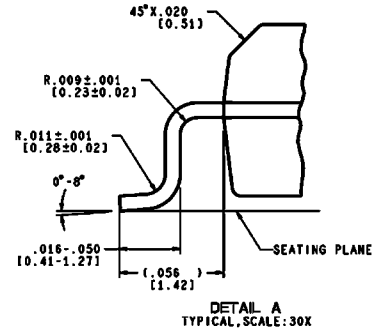
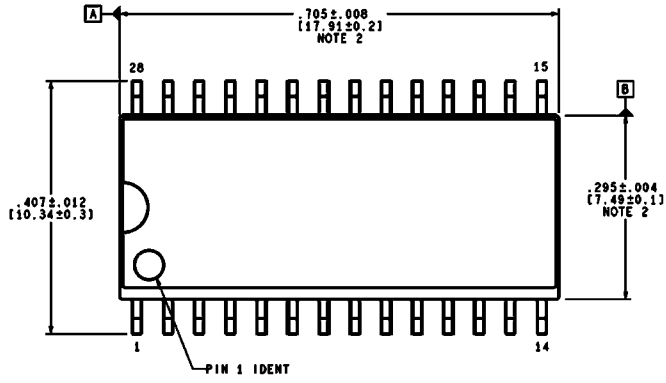
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Layout Considerations

The optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. Low ESR / ESL capacitors must be connected close to the IC, between VDD and VSS pins and between the HB and HS pins to support the high peak currents being drawn from VDD during turn-on of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS pin), the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding Considerations:
 - a. The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs should be placed as close as possible to the gate driver.
 - b. The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

Physical Dimensions



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

NS Package Drawing M28B

30134150

Notes

Notes

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