

Le79485

Subscriber Line Interface Circuit

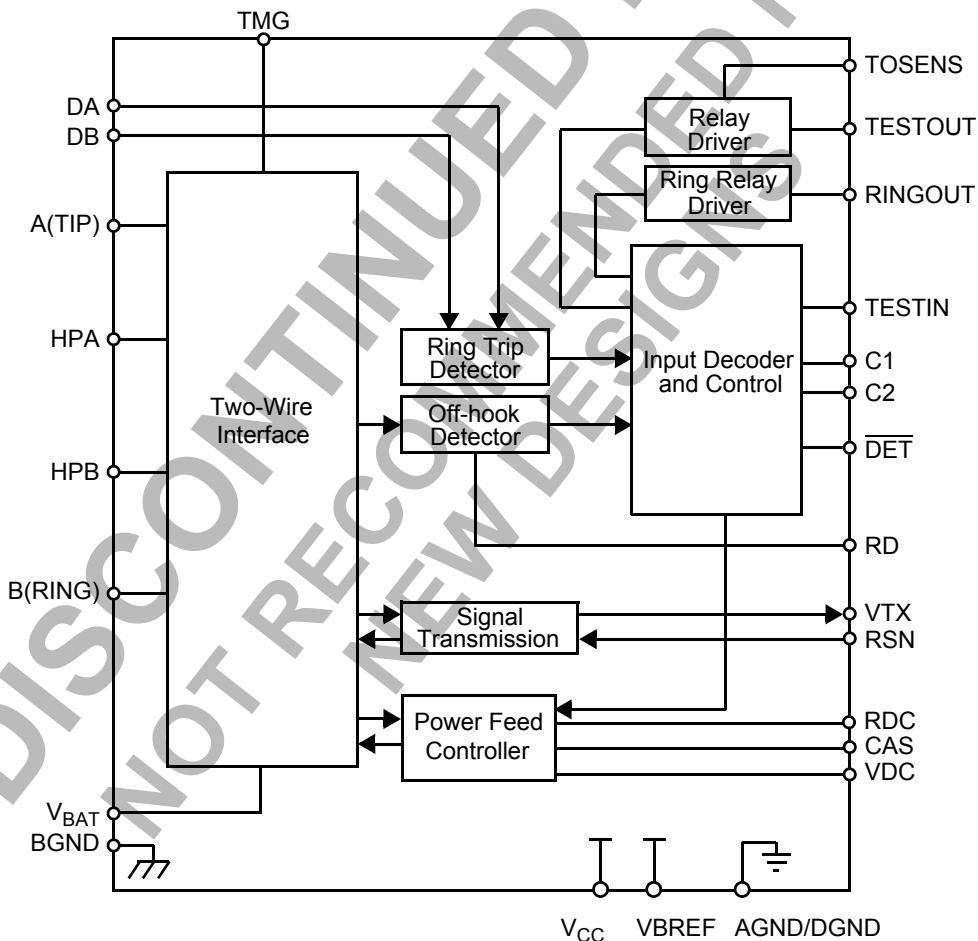


The Le79485 Subscriber Line Interface Circuit implements the basic telephone line interface functions and enables the design of low cost, high performance POTS line interface cards.

DISTINCTIVE CHARACTERISTICS

- Control states: Active, Ringing, Standby and Disconnect
- Low standby power
- -19 V to -58 V battery operation
- On-hook transmission
- Two-wire impedance set by single external impedance
- Programmable constant current feed
- Programmable loop detect threshold
- Programmable ring trip detect threshold
- No -5 V supply required
- Current Gain = 500
- On chip thermal management (TMG)
- Two on chip-relay drivers with relay snubbers

BLOCK DIAGRAM



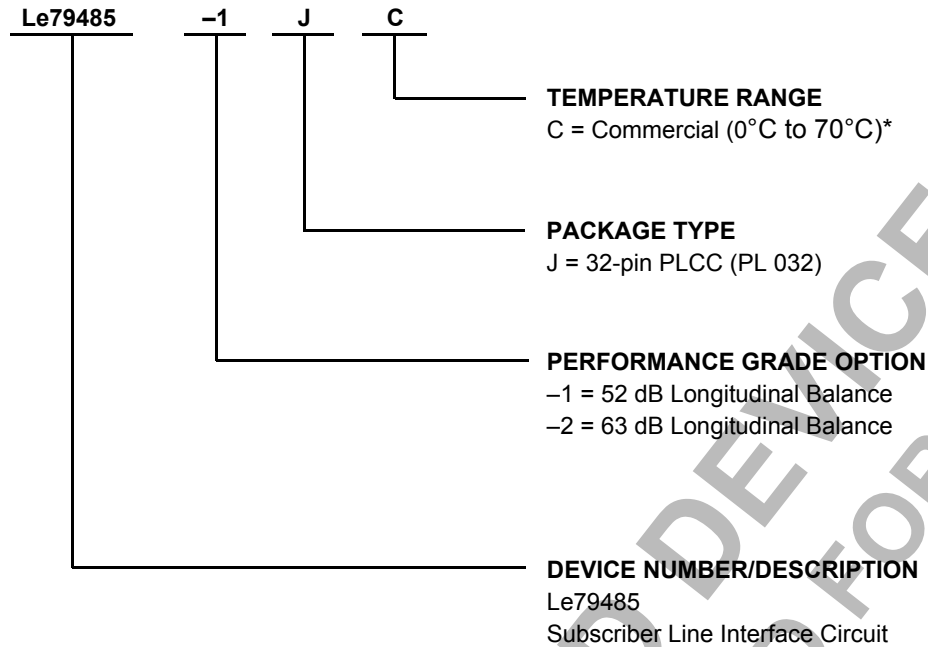
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ORDERING INFORMATION

Standard Products

Legerity standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations		
Le79485	-1	JC
	-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Legerity sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on Legerity's standard military grade products.

Note:

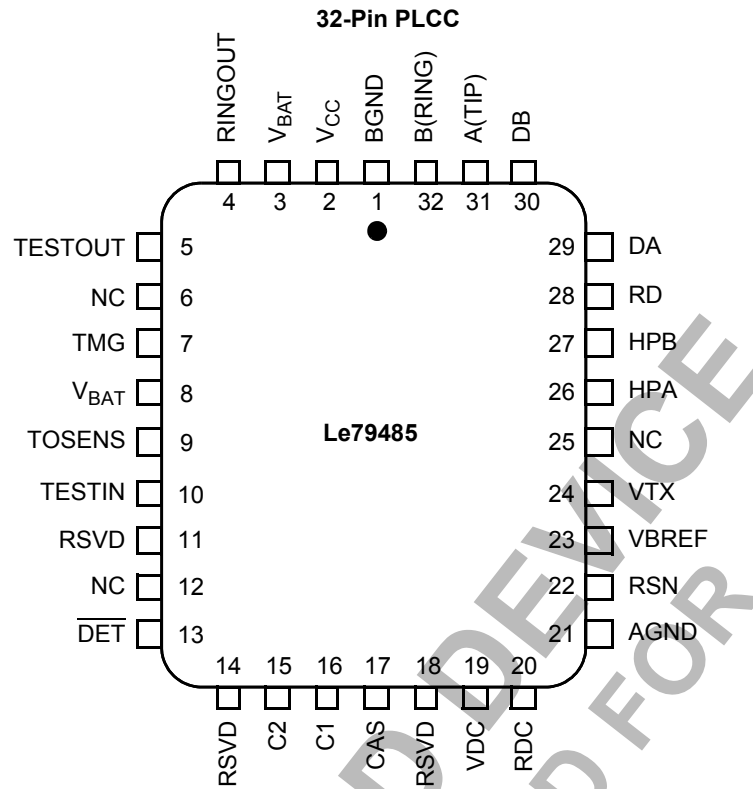
* Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from -25°C to +85°C is guaranteed by characterization and periodic sampling of production units.

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CONNECTION DIAGRAM

Top View



Notes:

1. Pin 1 is marked for orientation.
2. NC = No Connect
3. RSVD = Reserved. Make no connection to these pins.

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PIN DESCRIPTIONS

Pin Names	Type	Description
AGND/DGND	Gnd	Analog and Digital ground.
A(TIP)	Output	Output of A(TIP) power amplifier.
BGND	Gnd	Battery (power) ground.
B(RING)	Output	Output of B(RING) power amplifier.
C1, C2	Input	Decoder. SLIC control pins. C2 is MSB and C1 is LSB. TTL compatible with internal current source pullup.
CAS	Capacitor	Anti-saturation pin for capacitor to filter reference voltage when operating in anti-saturation region.
DA	Input	Ring trip negative. Negative input to ring trip comparator.
DB	Input	Ring trip positive. Positive input to ring trip comparator.
$\overline{\text{DET}}$	Output	Switch Hook Detector. A logic Low indicates that selected condition is detected. The detect condition is selected by the logic inputs (C1 and C2). The output is open-collector with a built-in 15 k Ω pull-up resistor.
HPA	Capacitor	High-Pass Filter Capacitor. A(TIP) side of high-pass filter capacitor.
HPB	Capacitor	High-Pass Filter Capacitor. B(RING) side of high-pass filter capacitor.
NC	—	No connect. Pin not internally connected.
RD	Resistor	Detector resistor. Detector threshold set and filter pin.
RDC	Resistor	DC feed resistor. Connection point for the DC feed current programming network. The other end of the network connects to the receiver summing node (RSN).
RINGOUT	Output	Ring Relay Driver. Open collector driver with emitter internally connected to BGND.
RSN	Input	The metallic current (AC and DC) between A(TIP) and B(RING) is equal to 500 x the current into this pin. The networks that program receive gain, two-wire impedance, and feed current all connect to this node.
RSVD	—	This pin is reserved for Legerity use. Make no connection to this pin.
TESTIN	Input	Relay driver control. A logic low at TESTIN forces TESTOUT low. TTL compatible with internal current source pullups.
TESTOUT	Output	Relay driver. Open collector driver with emitter internally connected to BGND.
TMG	—	Thermal Management. External resistor connects between this pin and VBAT to offload power from SLIC.
TOSENS	Output	TESOUT sense pin. Internally connected to resistive divider from TESTOUT pin.
VBAT	Battery	Battery supply and connection to substrate.
VCC	Power	+5 V power supply.
VBREF	—	This is an Legerity reserved pin and always must be connected to the V _{BAT} pin.
VDC	Output	The voltage output at this pin is proportional to the voltage across pins A and B (V _{AB}).
VTX	Output	Transmit Audio. This output is 0.50 times the A(TIP) and B(RING) metallic voltage. VTX also sources the two-wire input impedance programming network.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−55°C to +150°C
V _{CC} with respect to AGND/DGND	−0.4 V to +7 V
V _{BAT} with respect to AGND/DGND:	
Continuous	+0.4 V to −70 V
10 ms	+0.4 V to −75 V
BGND with respect to AGND/DGND	+3 V to −3 V
A(TIP) or B(RING) to BGND:	
Continuous	V _{BAT} to +1 V
10 ms (F = 0.1 Hz)	−70 V to +5 V
1 μs (F = 0.1 Hz)	−80 V to +8 V
250 ns (F = 0.1 Hz)	−90 V to +12 V
Current from A(TIP) or B(RING)	±150 mA
RINGOUT Current	50 mA
TESTOUT Current	100 mA
RINGOUT/TESTOUT voltage	BGND to +7 V
RINGOUT/TESTOUT transient	BGND to +10 V
DA and DB inputs	
Voltage on ring trip inputs	V _{BAT} to 0 V
Current into ring trip inputs	±10 mA
C1, C2, TESTIN	
Input voltage	−0.4 V to V _{CC} + 0.4 V
Maximum power dissipation, continuous,	
T _A = 70°C, No heat sink (See note):	
In 32-pin PLCC package	1.7 W
Thermal Data:	θ _{JA}
In 32-pin PLCC package	43°C/W typical
ESD immunity/pin (HBM)	1500 V

Note: Thermal limiting circuitry on chip will shut down the circuit at a junction temperature of about 165°C. The device should never see this temperature and operation above 145°C junction temperature may degrade device reliability.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Ambient Temperature	0°C to +70°C*
V _{CC}	4.75 V to 5.25 V
V _{BAT}	−19 V to −58 V
AGND/DGND	0 V
BGND with respect to	
AGND/DGND	−100 mV to +100 mV
Load resistance on VTX to ground	20 kΩ minimum

The operating ranges define those limits between which the functionality of the device is guaranteed.

* Specifications in this data sheet are guaranteed by testing from 0°C to +70°C. Performance from −25°C to +85°C is guaranteed by characterization and periodic sampling of production units.

ELECTRICAL SPECIFICATIONS (See Note 1)

Description	Test Conditions		Min	Typ	Max	Unit	Note
Transmission Performance							
2-wire return loss	200 Hz to 3.4 kHz		18	36		dB	1, 4
Analog output (VTX) impedance				3	20	Ω	4
Analog (VTX) output offset voltage	0°C to +70°C -25°C to +85°C		-40 -50		+40 +50	mV mV	4
Overload level, 2 wire and 4 wire	Active state		2.5			Vpk	2.1
Overload level	On-hook, $R_{LAC} = 900 \Omega$		1.5			Vrms	2.2
THD, Total Harmonic Distortion	0 dBm +7 dBm			-64 -55	-50 -40	dB	5
THD, on-hook	+3 dBm, $R_{LAC} = 900 \Omega$				-36		
Longitudinal Capability (See Test Circuit D)							
Longitudinal to metallic L-T, L-4 balance	<u>200 Hz to 1 kHz</u>		<u>P.G.*</u>				
	-1	0°C to +70°C	-1	53		dB	4
	-2	0°C to +70°C	-2	63			
	-1	-25°C to +85°C	-1	50			
	-2	-25°C to +85°C	-2	58			
	<u>1 kHz to 3.4 kHz</u>						
	-1	0°C to +70°C	-1	53		dB	
	-2	0°C to +70°C	-2	58			
-1	-25°C to +85°C	-1	50				
-2	-25°C to +85°C	-2	53				
Longitudinal current per pin (A or B)	Active state		8.5	27		mArms	7
Longitudinal impedance at A or B	0 to 100 Hz			25	35	Ω /pin	
Idle Channel Noise							
C-message weighted noise	$R_L = 600 \Omega$ $R_L = 600 \Omega$	0°C to +70°C -25°C to +85°C		+7	+11 +13	dBrnC	4
Insertion Loss and Balance Return Signal (See Test Circuits A and B)							
Gain accuracy 4- to 2-wire	0 dBm, 1 kHz	0°C to +70°C -25°C to 85°C	-0.15 -0.20	0 0	+0.15 +0.20	dB	4
Gain accuracy 2- to 4-wire, 4- to 4-wire	0 dBm, 1 kHz	0°C to +70°C -25°C to 85°C	-6.17 -6.22	-6.02 -6.02	-5.87 -5.82		4
Gain accuracy, 4- to 2-wire	On-hook, $R_{LAC} = 900 \Omega$		-0.35		+0.35		4
Gain accuracy, 2- to 4-wire, 4- to 4-wire	On-hook, $R_{LAC} = 900 \Omega$		-6.37	-6.02	-5.67		
Gain accuracy over frequency	300 to 3400 Hz relative to 1 kHz	0°C to +70°C -25°C to +85°C	-0.10 -0.15		+0.10 +0.15		4
Gain tracking	+3 dBm to -55 dBm relative to 0 dBm	0°C to +70°C -25°C to +85°C	-0.10 -0.15		+0.10 +0.15		4

* Performance Grade

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ELECTRICAL SPECIFICATIONS (See Note 1) (continued)

Description	Test Conditions	Min	Typ	Max	Unit	Note
Gain tracking On-hook, $R_{LAC} = 900 \Omega$	0 dBm to -37 dBm	0°C to +70°C	-0.10		+0.10	dB dB dB
		-25°C to +85°C	-0.15		+0.15	
	+3 dBm to 0 dBm		-0.35		+0.35	
Group delay	0 dBm, 1 kHz		4		μ s	4, 7
Line Characteristics						
I_L , short loops, active	$R_{LDC} = 900 \Omega$	20	23	26	mA	
I_L , long loops, active	$R_{LDC} = 1600 \Omega$, $BAT = -42.75 V$, $T_A = 25^\circ C$	18	22			
I_L , accuracy, Standby mode	$I_L = \frac{ BAT - 3 V}{R_L + 400}$ $T_A = 25^\circ C$	$0.7I_L$	I_L	$1.3I_L$		
	Constant current region	18	30			
I_L , loop current, Disconnect mode	$R_L = 0$			100	μ A	
$I_{L LIM}$	Active, A and B to GND		80	120	mA	
VDC accuracy	$R_L = 300 \Omega$	0.300	0.350	0.400	V	
	$R_L = 900 \Omega$	0.920	1.050	1.18		
V_{AB} , open circuit voltage	$V_{BAT} = -52 V$	-42.75	-46			
Power Supply Rejection Ratio (Vripple = 100 mV RMS), Active Normal Mode						
V_{CC}	50 Hz to 3400 Hz	30	50		dB	5
	500 Hz to 3000 Hz	35				
V_{BAT}	50 Hz to 3400 Hz	28	50			
	500 Hz to 3000 Hz	40				
V_{CC} , on-hook	50 Hz to 3400 Hz	30	50			
V_{BAT} , on-hook	50 Hz to 100 Hz	4	8			4
	100 Hz to 200 Hz	9	14			
	200 Hz to 300 Hz	16	24			
	300 Hz to 500 Hz	24	28			
	500 Hz to 1000 Hz	30	34			
	1 kHz to 3400 Hz	34	40			
Control pin feed-through (C1, C2)	50 Hz to 3400 Hz	35	50			
Effective internal resistance	CAS pin to V_{BAT}	85	170	255	k Ω	
Power Dissipation						
On-hook, disconnect			45	70	mW	
On-hook, Standby mode			55	85		
On-hook, Active mode	$R_{TMG} = 2500 \Omega$		150	270		
Off-hook, Standby mode	$R_L = 600 \Omega$		860	1200		
Off-hook, Active mode	$R_L = 300 \Omega$, $R_{TMG} = 2500 \Omega$		700	950		
Supply Currents, Battery = -48 V						
ICC, On-hook V_{CC} supply current	Disconnect mode		3.0	4.0	mA	
	Standby mode		2.8	4.0		
	Active mode		6.3	8.5		
IBAT, On-hook V_{BAT} supply current	Disconnect mode		0.6	1.0		
	Standby mode		0.8	1.5		
	Active mode		2.8	4.8		
RFI Rejection						

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ELECTRICAL SPECIFICATIONS (See Note 1) (continued)

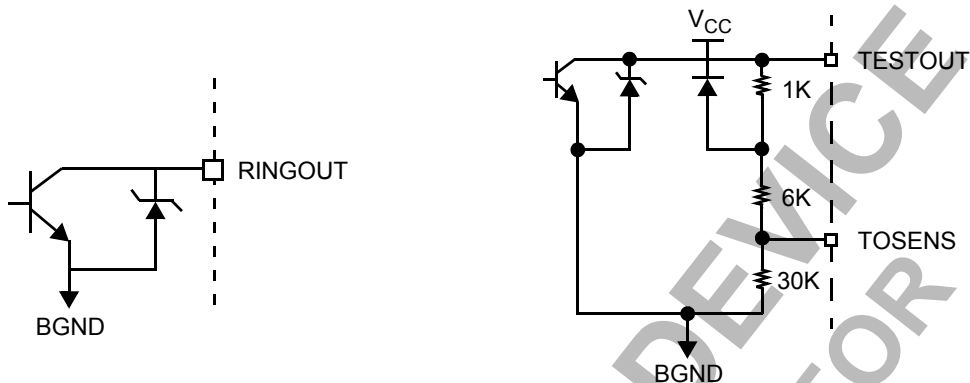
Description	Test Conditions	Min	Typ	Max	Unit	Note
RFI rejection	100 kHz to 30 MHz, (See Figure F)			1.0	mVrms	4
Receive Summing Node (RSN)						
RSN DC voltage	$I_{RSN} = 0$ mA		0		V	4
RSN impedance	200 Hz to 3.4 kHz		10	20	Ω	
Logic Inputs (C1, C2, TESTIN)						
V_{IH} , input High voltage		2.0			V	
V_{IL} , input Low voltage				0.8		
I_{IH} , input High current		-75		40	μ A	
I_{IL} , input Low current		-400		-13		
Logic Output (DET)						
V_{OL} , output Low voltage	$I_{out} = 0.3$ mA, 15 k Ω to V_{CC}			0.40	V	
V_{OH} , output High voltage	$I_{out} = -0.1$ mA, 15 k Ω to V_{CC} $I_{out} = -10$ μ A	2.4 $0.7 \cdot V_{CC}$	$0.97 \cdot V_{CC}$			
Ring Trip Detector Input (DA, DB)						
Bias current		-20	-5		nA	4
Offset voltage	Source resistance = 2 M Ω	-50	0	+50	mV	6
Offset voltage	Source resistance mismatch = 3 M Ω	-50	0	+50		4
Relay Driver Output (RINGOUT, TESTOUT)						
V_{OH} , On voltage, RINGOUT	$I_{OL} = 40$ mA		+0.3	+0.7	V	
V_{OH} , On voltage, TESTOUT	$I_{OL} = 80$ mA		+0.4	+1.0		
I_{OL} , Off leakage, RINGOUT	$V_{OH} = +5$ V		0	100	μ A	
I_{OL} , Off leakage, TESTOUT	$V_{OH} = +5$ V	80	140	200		
Zener break over	$I_Z = 300$ μ A	5.7	7.2		V	
Zener On voltage, RINGOUT	$I_Z = 30$ mA		8			
Zener On voltage, TESTOUT	$I_Z = 80$ mA		8			
TESTOUT Sense Output (TOSENS)						
V_{OL}	I_{OL} TESTOUT = 80 mA		+0.2	+0.6	V	
V_{OH}	$I_{OUT} = 100$ μ A $I_{OUT} = 10$ μ A	2.4 $0.7 \cdot V_{CC}$	3.5 $0.81 \cdot V_{CC}$	5		
V_{OH} , with transient @ TESTOUT	$I_Z = 60$ mA		V_{CC}	$V_{CC} + 0.3$		
Z_{OUT}			5.7		k Ω	
Loop Detector						
R_{LTH} , loop detect threshold resistance	Active state, RD = 35.4 k Ω Standby state, RD = 35.4 k Ω	RD/11.5 RD/15	RD/10.1 RD/12.6	RD/8.8 RD/10	Ω	8

Notes:

- Unless otherwise noted, test conditions are
 $BAT = -52$ V, $V_{CC} = +5$ V, $R_L = 900$ Ω , $R_T = 225$ k Ω , $RRX = 225$ k Ω , $R_{DC1} = R_{DC2} = 27.17$ k Ω , $R_{TMG} = 2500$ Ω , $RD = 35.4$ k Ω ,
no fuse resistors, $CHP = 0.1$ μ F, $C_{DC} = 0.1$ μ F, $C_{CAS} = 0.1$ μ F, $D1 = 1N400x$, $BSWEN =$ logic low (0), (two-wire AC input impedance is a 900 Ω).

- 2.1 Overload level is defined when THD = 1%.
- 2.2 Overload level is defined when THD = 1.5%.
3. Balance return signal is the signal generated at VTX by V_{RX} . This spec assumes that the two-wire AC load impedance matches the programmed impedance.
4. Not tested in production. This parameter is guaranteed by characterization or correlation to other tests.
5. This parameter is tested at 1 kHz in production. Performance at other frequencies is guaranteed by characterization.
6. Tested with $0\ \Omega$ source impedance. $2\ M\Omega$ specified for system design only.
7. Minimum current level guaranteed not to cause a false Loop Detect.
8. \overline{DET} will go high during loss of V_{BAT} supply.

RELAY DRIVER SCHEMATICS



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Table 1. User-Programmable Components

$Z_T = 250(Z_{2WIN} - 2R_F)$	Z_T is connected between the VTX and RSN pins. The fuse resistors are R_F , and Z_{2WIN} is the desired 2-wire AC input impedance. When computing Z_T , the internal current amplifier pole and any external stray capacitance between VTX and RSN must be taken into account.
$Z_{RX} = \frac{Z_L}{G_{42L}} \cdot \frac{500 \cdot Z_T}{Z_T + 250(Z_L + 2R_F)}$	Z_{RX} is connected from V_{RX} to RSN. Z_T is defined above, and G_{42L} is the desired receive gain.
$R_{DC1} + R_{DC2} = \frac{1250}{I_{LOOP}}$ $C_{DC} = 1.5 \text{ ms} \cdot \frac{R_{DC1} + R_{DC2}}{R_{DC1} \cdot R_{DC2}}$	R_{DC1} , R_{DC2} , and C_{DC} form the network connected to the RDC pin. R_{DC1} and R_{DC2} are approximately equal. I_{LOOP} is the desired loop current in the constant current region.
$R_{D_{ACTIVE}} = 10.1 \cdot R_{LTH}$ <p style="text-align: right;">for $V_{BAT} > 40 \text{ V}$</p> $R_{D_{STANDBY}} = 10(R_{LTH} + 400) \cdot \frac{54 \text{ V}}{BAT - 3}$ $R_{D_{ACTIVE}} = \frac{375}{I_{DET}}$ <p style="text-align: right;">for $V_{BAT} < 40 \text{ V}$</p> $R_{D_{STANDBY}} = \frac{375}{I_{DET}}$	R_{LTH} is the desired loop resistance detect threshold. I_{LTH} is the loop current at R_{LTH} for a given battery.
$C_{CAS} = \frac{1}{3.4 \cdot 10^5 \pi F_c}$	C_{CAS} is the regulator filter capacitor and F_c is the desired filter cut-off frequency.
$I_{Standby} = \frac{V_{BAT} - 3 \text{ V}}{400 \Omega + R_L}$	Standby Loop current (resistive region).
$\text{VDC Scale Factor} = \frac{63.4 \cdot R_L}{R_{DC1} + R_{DC2}}$	VDC Scale Factor valid for constant current region.
Thermal Management Equations (Normal Active and Tip Open States)	
$R_{TMG} \geq \frac{ V_{BAT} - 6 \text{ V}}{I_{LOOP}} - 70 \Omega$	R_{TMG} is connected from TMG to V_{BAT} and is used to limit power dissipation within the SLIC in Active and Disconnect modes only.
$P_{RTMG} = \frac{(V_{BAT} - 6 \text{ V} - (I_L \cdot R_L))^2}{(R_{TMG} + 70 \Omega)^2} \cdot R_{TMG}$	Power dissipated in the thermal management resistor, R_{TMG} , during Active and Disconnect states.
$P_{SLIC} = V_{BAT} \cdot I_L - P_{RTMG} - R_L(I_L)^2 + 0.12 \text{ W}$	Power dissipated in the SLIC while in active and disconnect states.

Table 2. SLIC Decoding

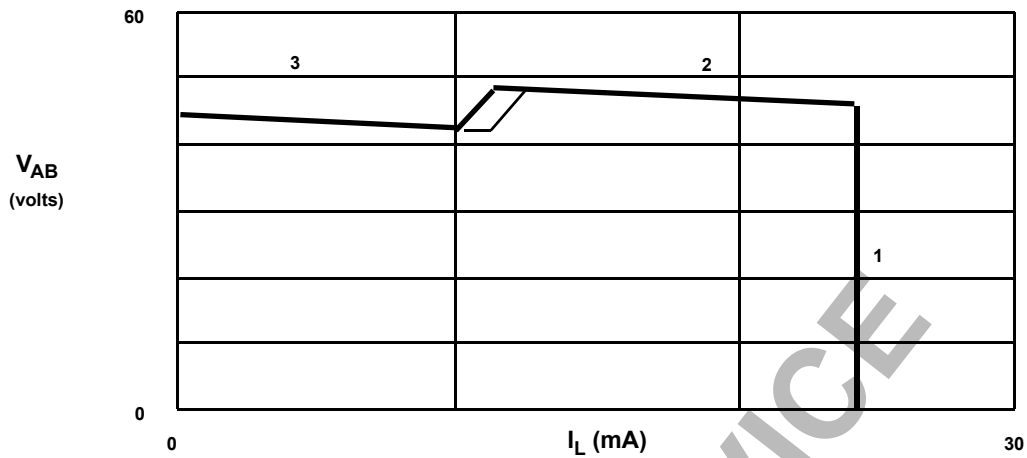
State	C2	C1	2-Wire Status	DET Output
0	0	0	Disconnect	Ring Trip
1	0	1	Ringing	Ring Trip
2	1	0	Active	Loop Det.
3	1	1	Standby	Loop Det.

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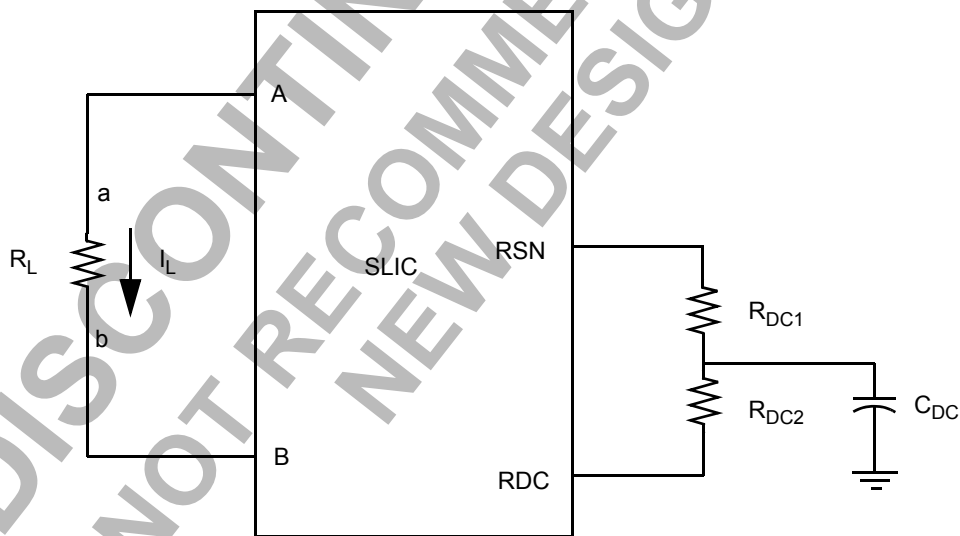
DC Feed Characteristics

$R_{DC} = R_{DC1} + R_{DC2} = 54.34 \text{ k}\Omega$
 $BAT = -48 \text{ V}$



1. $V_{AB} = I_L R_L' = \frac{1250}{R_{DC}} R_L'$, where $R_L' = R_L + 2R_F$
2. $V_{AB} = |V_{BAT}| - 3.3 - I_L \frac{R_{DC}}{300}$
3. $V_{AB} = |V_{BAT}| - 5.5 - I_L \frac{R_{DC}}{300}$

Figure 1. Load Line (typical)



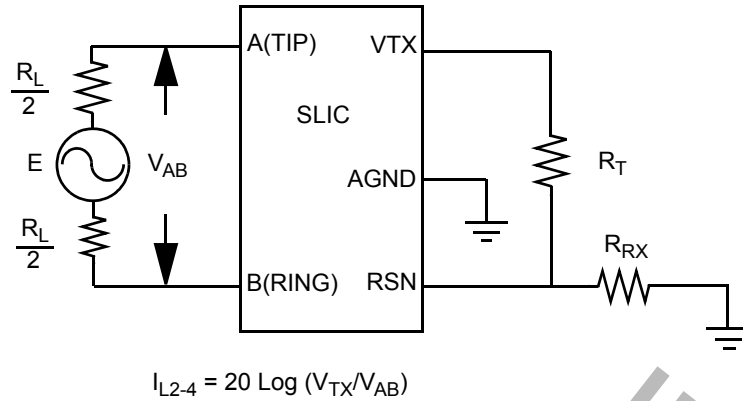
Feed current programmed by R_{DC1} and R_{DC2}

Figure 1. Feed Programming

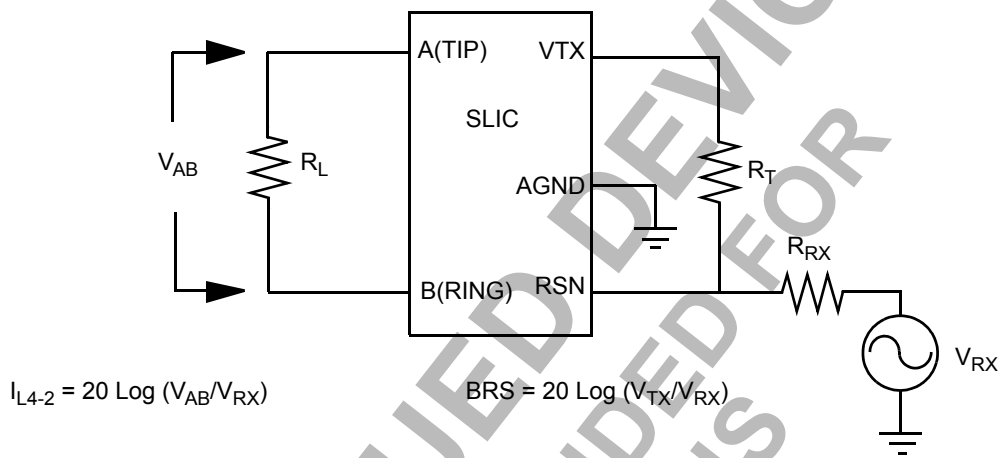
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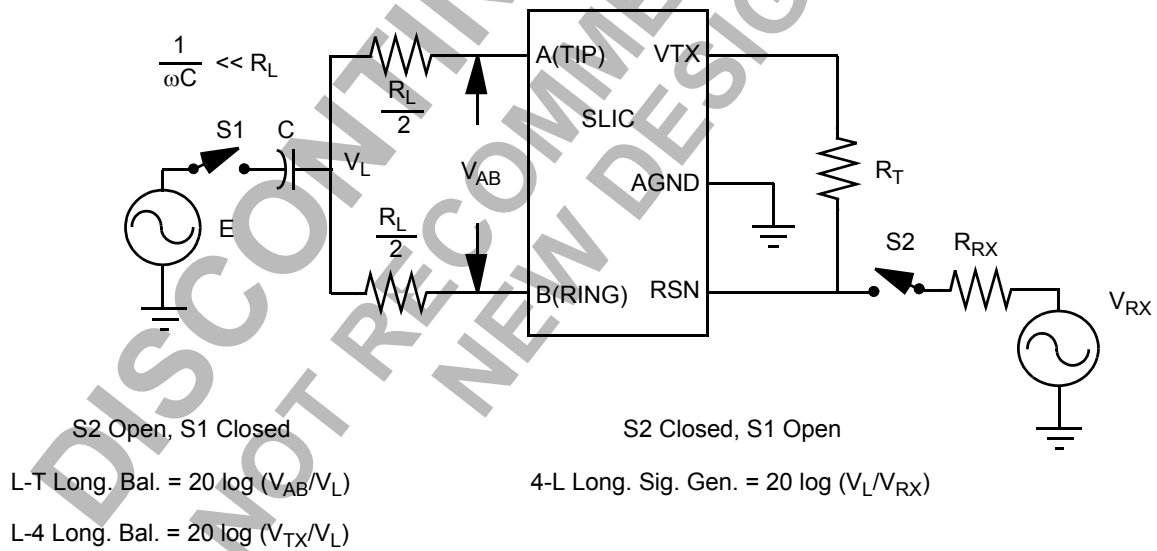
TEST CIRCUITS



A. Two- to Four-Wire Insertion Loss



B. Four- to Two-Wire Insertion Loss and Balance Return Signal

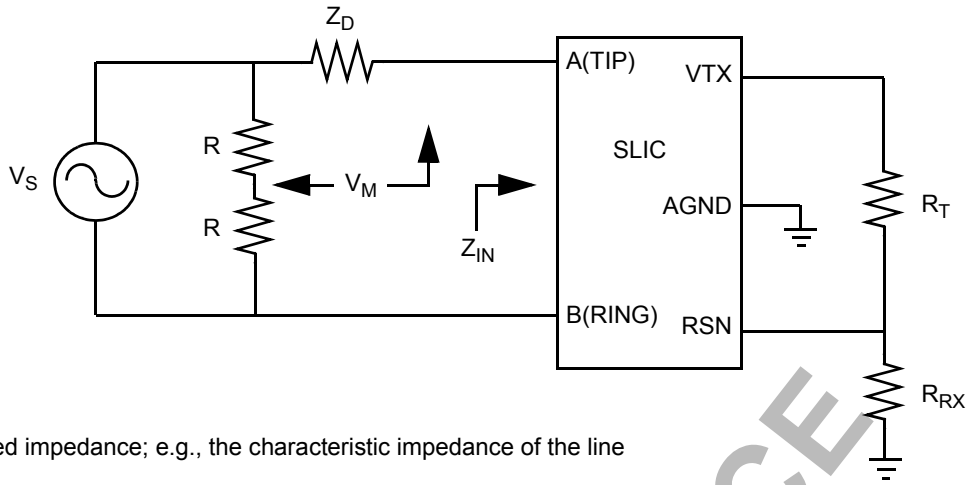


C. Longitudinal Balance

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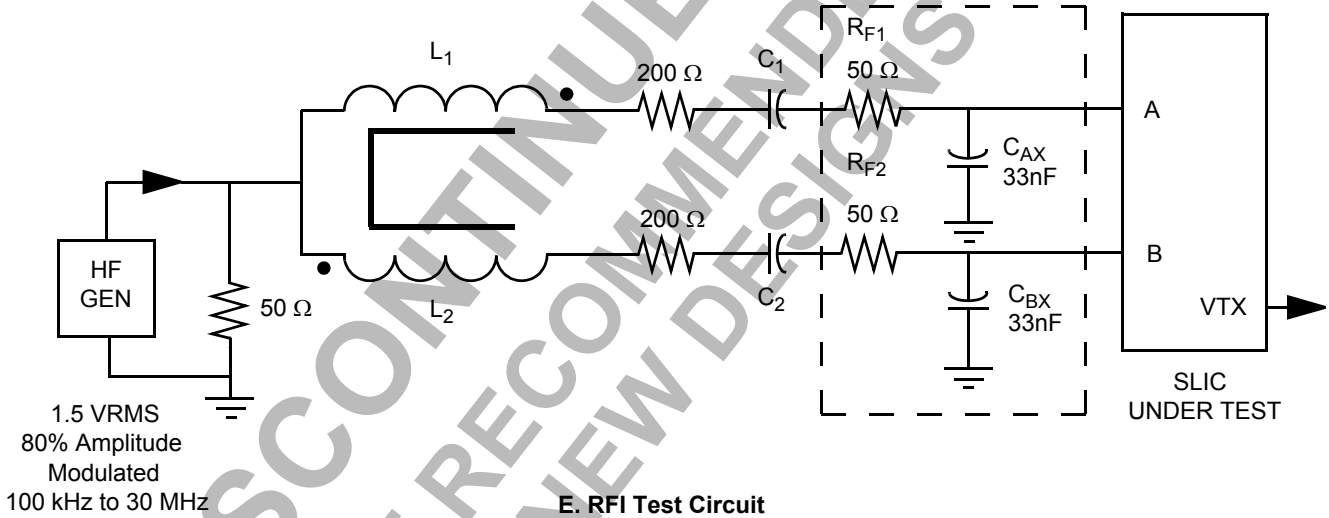
TEST CIRCUITS (continued)



Z_D : The desired impedance; e.g., the characteristic impedance of the line

$$\text{Return loss} = -20 \log(2V_M/V_S)$$

D. Two-Wire Return Loss Test Circuit

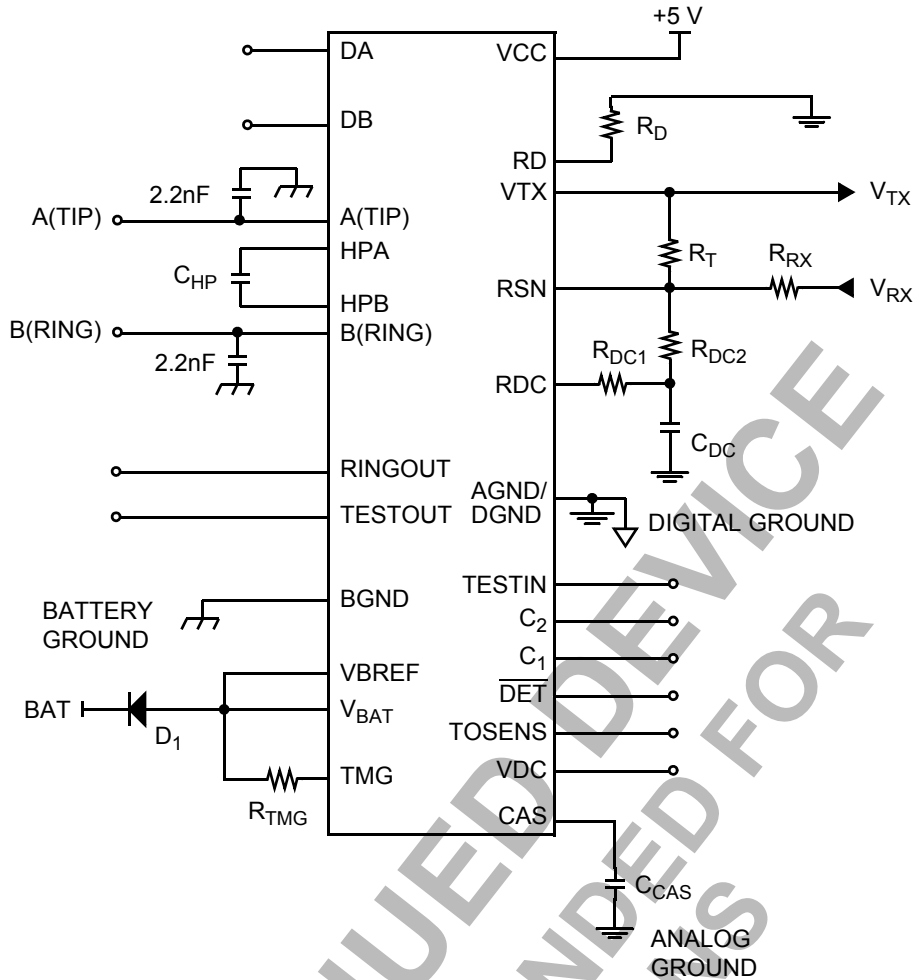


E. RFI Test Circuit

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TEST CIRCUITS (continued)



F. Le79485 Test Circuit

REVISION SUMMARY

Revision 1 to Revision 2

- Absolute Maximum Ratings: Added ESD immunity specification

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