AMCC S3062

SONET/SDH/Gigabit Ethernet

Multi-Rate Performance Monitor

with Forward Error Correction

Revision D

Table of Contents

List of Tables

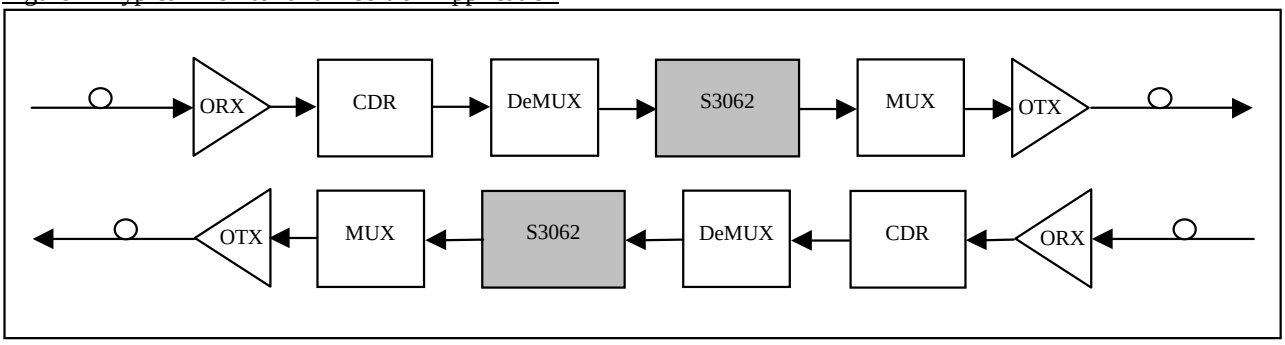
List of Figures

1 GENERAL DESCRIPTION

The S3062 Multi-Rate SONET/SDH STS-3/STM-1, STS-12/STM-4, STS-48/STM-16 & Gigabit Ethernet (GBE) Performance Monitor chip is a fully integrated checking device complying with SONET/SDH transmission standards. The S3062 implements all necessary Performance Monitoring functions on the SONET/SDH section and line overhead bytes at three different rates (STS-3/STM-1, STS-12/STM-4, and STS-48/STM-16). It also has a mode of operation permitting it to monitor a Gigabit Ethernet data stream for loss of synchronization, 8B/10B code violations and disparity errors. Furthermore, any type of data entering and leaving the chip can be optionally decoded and encoded with forward error correction (FEC) information and also differentially encoded and decoded.

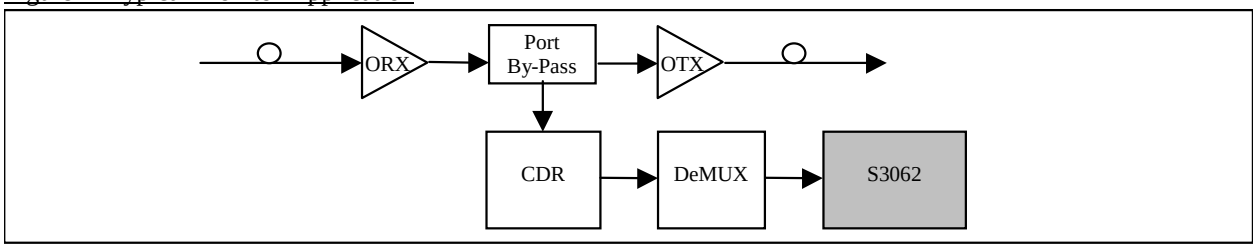
Figure 1 shows a typical network application for the Performance Monitor. Data is received from the fiber and passed through a clock/data recovery device (CDR) and a de-multiplexer device to the S3062. The S3062, optionally, carries out performance monitor error checking, and overhead data extraction, and insertion. Detected errors and accumulated error counts can be accessed by the user either through a processor interface, an FPGA interface, or in a number of cases, from I/O pins. The data stream is then transmitted out onto the fiber via a high-speed multiplexer, and an optics device. All SONET/GBE performance monitor error checking and overhead insertion may be by-passed by selecting the low-power pass-through mode of operation.

Figure 1 Typical Monitor and Insertion Application



In Figure 2 , the S3062 is only used to monitor data without overhead insertion. In this application, the MUX may be removed and a Port By-Pass circuit added for a low power monitoring solution.

Figure 2 Typical Monitor Application



1.1 Applications

- ✓ SONET/SDH-based transmission systems and test equipment
- ✓ Gigabit Ethernet-based transmission systems
- ✓ Add Drop Multiplexers (ADM)
- ✓ Fiber optic terminators, repeaters and test equipment
- ✓ FEC augmented applications for reliable data transmission over impaired channels

1.2 Features

- ✓ Single 3.3V supply
- ✓ 352-pin SBGA (Super Ball Grid Array) package
- ✓ Bellcore, ITU-T and IEEE compliant*
- ✓ Functions with AMCC MUX/DeMUX chipsets
- ✓ Provides a 16 bit input and a 16 bit output single-ended PECL data path
- ✓ Optionally differentially decodes and encodes incoming and outgoing data
- ✓ Provides optional Reed Solomon encoding of data for Forward Error Correction (FEC)
- ✓ Provides optional Reed Solomon decoding of data for Forward Error Correction (FEC)
- ✓ Provides on-chip clock dividers to simplify external clock generation for Forward Error Correction (FEC)
- ✓ Optionally provides a data link in the FEC framing bytes for transmission of messages, error information, orderwire, etc.
- ✓ Provides selectable error correcting rates
- ✓ Monitors FEC data for total corrected bit errors, corrected ones, corrected zeros, corrected bytes, and uncorrectable blocks
- ✓ Extracts and optionally inserts SONET/SDH overhead bytes via an MPC860 microprocessor port
- ✓ Extracts and optionally inserts SONET/SDH overhead bytes via a 21 bit FPGA port
- ✓ Extracts and optionally inserts orderwire bytes (E1 and E2) via serial I/O
- ✓ Extracts and optionally inserts the data communication channels (D1-3 and D4-12) via serial I/O
- ✓ Performs frame and byte alignment and outputs frame pulses
- ✓ Performs optional frame-synchronous scrambling and descrambling
- ✓ Monitors for Loss of Signal and outputs alarm (LOS)
- ✓ Monitors for Out of Frame and outputs alarm (OOF)
- ✓ Monitors for Loss of Frame and outputs alarm (LOF)
- ✓ Monitors J0 byte for section trace messages
- ✓ Monitors B1 byte for Bit Interleave parity errors and outputs error indications (B1ERR)
- ✓ Monitors B2 byte for Bit interleave parity errors, Signal Degrade (SD) and Signal Fail (SF)
- ✓ Monitors K1, K2 bytes for Automatic Protection Switching (APS) changes, line AIS and line RDI
- ✓ Monitors the S1 byte for mismatches and inconsistent values
- ✓ Monitors the M1 byte for Remote Error Indications (REI)
- ✓ Monitors for Gigabit Ethernet Loss of Synchronization (LOS), 8B/10B code violations and disparity errors
- ✓ Optionally calculates and inserts section bit interleaved parity (B1)
- ✓ Optionally calculates and inserts line bit interleaved parity (B2)
- ✓ Optionally turns OFF (sets low) all transmitted data
- ✓ Optionally inserts AIS, either automatically depending on line conditions or under user control
- ✓ Optionally inserts valid SONET/SDH section and line overhead on any data format with a CLKINP/N and TXCLKP/N input
- ✓ Generates valid SONET/SDH section (regenerator) overhead with line AIS data with only a TXCLKP/N input
- ✓ Optionally permits transparent pass through of all data regardless of format
- ✓ Optionally injects bit errors in any data type

* The OOF/LOF State Machine has changed with respect to the different revisions of silicon. Please consult Errata 7.2 OOF/LOF in the back of the data sheet for details.

1.3 Specification References

Bell Communications Research

- GR-253-CORE Issue 2, Revision 1 "SONET Transport Systems: Common Generic Criteria", December 1997.
- GR-253-ILR, Issue 2B, "SONET Transport Systems: Common Generic Criteria", December 1997.

International Telecommunications Union

- ITU-T G.783, “General Aspects of Digital Transmission Systems, Terminal Equipments”, Revised 1994.
- ITU-T G.707, “Network Node Interfaces for the Synchronous Digital Hierarchy”, March 1996.
- ITU-T G.975, “Forward Error Correction for Submarine Systems”, November 1996.

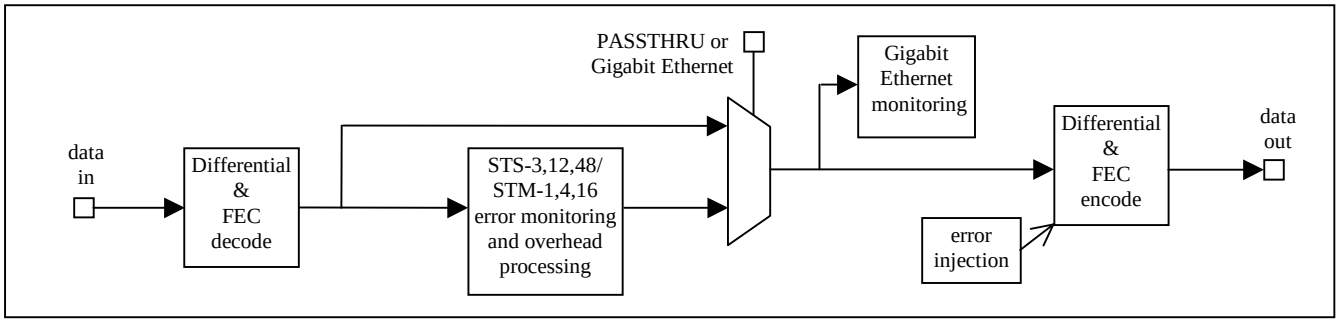
IEEE Draft P802.3z/D5.0, May 6, 1998

IEEE 1149.1b-1994 JTAG standard

2 S3062 OVERVIEW

The S3062 Performance Monitor optionally performs forward error correction on any data format. If the data is in SONET/SDH format, the S3062 implements all required features to check the data stream and allow for the extraction and insertion of the section and line overhead bytes. It also implements Gigabit Ethernet 8B/10B monitoring of the data stream. The data stream may run at any frequency from 155.52 to 2500Mb/s without FEC, which includes STS-3/STM-1, STS-12/STM-4, STS-48/STM-16 and Gigabit Ethernet rates. All modes use a 16-bit parallel single-ended LVPECL data path that is compatible with the AMCC MUX/DeMUX chipsets. The S3062 implements forward error correction, SONET/SDH section and line overhead monitoring and insertion, and Gigabit Ethernet monitoring. The diagram in Figure 3 shows the basic building blocks of the S3062.

Figure 3 Overview Block Diagram



2.1 Pass Through and Forward Error Correction Applications Overview

As shown in Figure 3 , data of any type may be passed through this chip without SONET/SDH or Gigabit Ethernet monitoring. The PASSTHRU I/O pin or register bit may be used for encoding and decoding forward error correction over data, that is in neither SONET/SDH nor Gigabit Ethernet format. In this mode of operation the performance monitors are turned OFF to reduce power consumption. PASSTHRU will have to be deselected to resume any performance monitoring functions regardless of the RATESEL settings. The differential and FEC encoder/decoder may also be turned OFF to further reduce the S3062's power consumption.

The FEC function is implemented with a variable-rate Reed Solomon codec based upon the Galois Field (2^8) symbols. Code rate and error correcting capability are selectable from rate = 238/255, 8 byte errors correctable, to rate = 248/255, 3 byte correctable. Error statistics are collected for a variety of conditions including total corrected bit errors, corrected ones, corrected zeros and uncorrectable blocks. The codec implementation encompasses the ITU G.975 recommendation for codec and rate, interleaved to four levels. A programmable frame synchronization byte is inserted for rapid and reliable acquisition of the coding frame boundary.

To select the pass-through mode, assert the PASSTHRU I/O signal pin or its corresponding register bit (the Micro Present byte should be loaded with a value of 59h for the register bit to take affect). FEC encoding/decoding may be enabled by asserting the FEC_ENC/FEC_DEC I/O pins. The FEC_ENC/FEC_ DEC I/O pins are ANDed with the complement of the associated FEC encoding/decoding register bits when the Micro Present byte is loaded with a value of 59h. Thus, the FEC encoder/decoder may only be enabled if the I/O pins are tied high.

NOTE: Pass-through mode has priority over all modes of operation (except differential and FEC encoding/decoding) and will negate their selection if pass-through mode is enabled. See sections 3.3.2.14 and 3.3.2.15 for a transmit multiplexer priority listing.

2.2 Gigabit Ethernet Application Overview

The Gigabit Ethernet circuitry monitors the received data stream for:

- Loss of synchronization.
- 8B/10B code violations.
- Disparity errors.

These errors are flagged and available at the I/O signal pins. Error counts are also accumulated over 1 second periods and are available via the processor interface.

The Gigabit Ethernet mode may be selected by setting the RATESEL[1:0] I/O signal pins or the corresponding register bits to the appropriate values seen in address tables and pin list. Differential encoding and decoding, as well as forward error correction, may also be implemented in this mode. NOTE: Pass-through mode has priority over RATESEL and will negate any RATESEL selections if pass-through mode is enabled.

2.3 SONET/SDH Application Overview

In SONET/SDH mode, all received section and line overhead bytes are captured and placed in a memory. The memory is accessible from either a processor or an FPGA. The overhead bytes that are defined by the SONET/SDH standards are also monitored for errors and performance monitoring (PM) statistics. The results are accessible from the processor or FPGA interface.

In addition to being stored in an accessible memory, received section overhead is managed as follows:

- A1 and A2 bytes are checked for framing and byte alignment.
- J0 byte is monitored for section trace messages.
- B1 byte is monitored for bit interleaved parity errors, which are accumulated over 1 second periods.
- E1 byte is optionally serialized and output on an I/O pin.
- D1-3 bytes are optionally serialized and output on an I/O pin.
- The data can be descrambled in accordance with SONET/SDH standards.

Section errors -- LOS, LOF, OOF and B1 -- are output on I/O pins and are available to the processor and FPGA interfaces.

In addition to being stored in an accessible memory, received line overhead is managed as follows:

- B2 byte is monitored for bit interleaved parity errors, which are accumulated over 1 second periods.
- K1 and K2 bytes are monitored for new or inconsistent values. K2 is also monitored for line AIS and RDI.
- D4-12 bytes are optionally serialized and output on an I/O pin.
- S1 byte is monitored for inconsistent values and for mismatches with a software programmable value.
- M1 byte is monitored for REI errors, which are accumulated over 1 second periods.
- E2 byte is optionally serialized and output on an I/O pin.

Line error indicators – line AIS, line RDI, line REI, B2, signal fail, signal degrade, K1, K2 and S1 changes are only accessible via the processor or FPGA interfaces; they are not output on I/O pins.

All transmitted section and line overhead bytes can be written through the FPGA or processor interface. In addition, data transmission can be modified as follows:

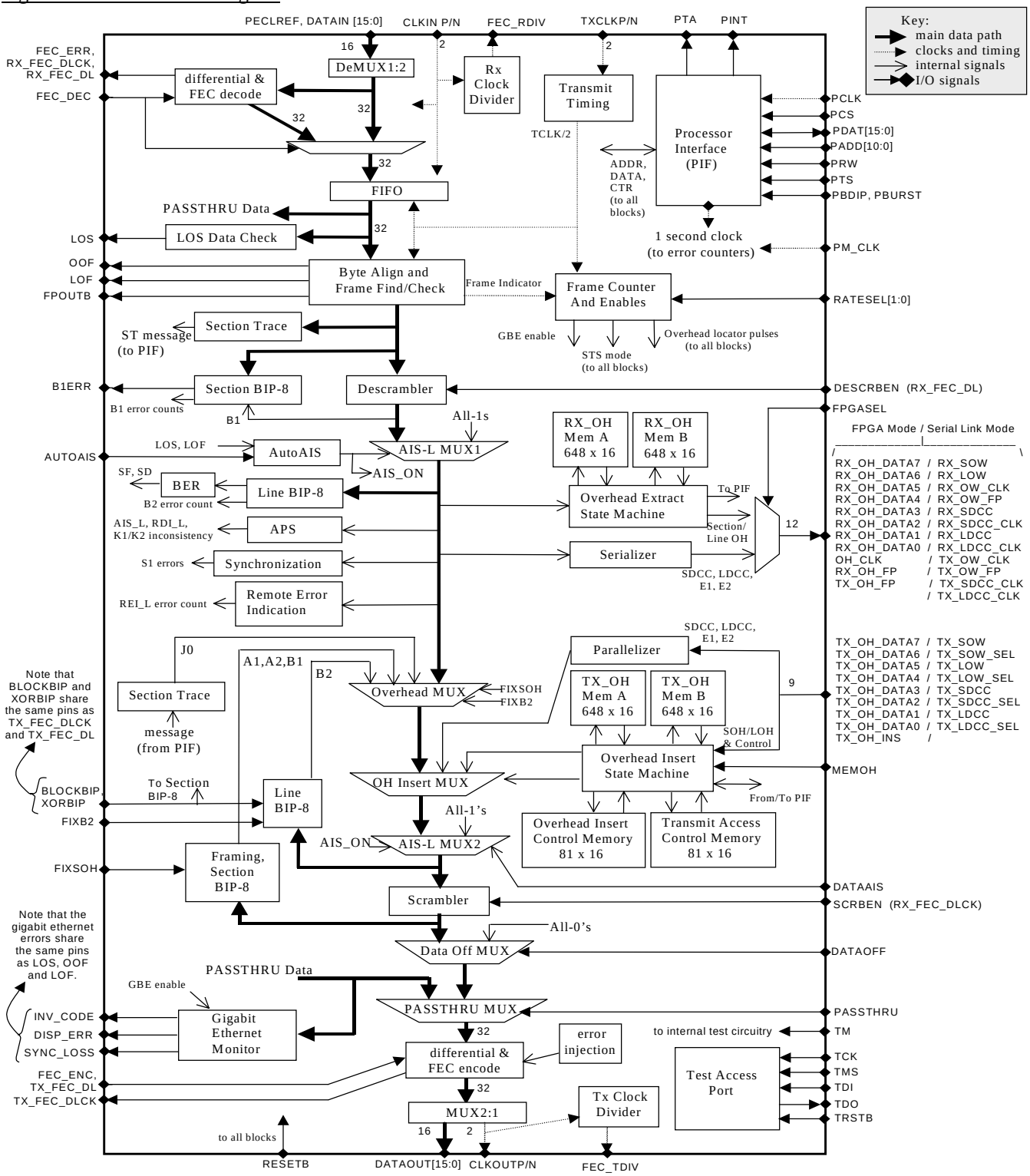
- Framing bytes can be regenerated with values A1 = F6h and A2 = 28h.
- J0 byte may be filled with section trace bytes from a memory.
- B1 and B2 bytes can be recalculated.
- E1, D1-3, D4-12 and E2 bytes can be sourced, serially from S3062 I/O pins.
- The data can be scrambled in accordance with SONET/SDH standards.
- Line AIS can be activated automatically when LOS or LOF conditions are detected, or the user may force the transmitter to output line AIS.
- The entire data stream can be turned off (all zeros output).

The SONET/SDH application is designed to monitor incoming SONET/SDH data streams and optionally modify them. It can also be used as a SONET/SDH generator. The S3062 transmit clock (TXCLKP/N) will generate correct section (regenerator) overhead and line AIS if the receive clock (CLKINP/N) is absent. If the receive clock is present, any data format may be turned into SONET/SDH frame. The frame counter does not need to find byte alignment to begin running. They start counting after the S3062 comes out of reset. To complete the frame, correct section and line overhead may be inserted from the TX_OH or any other S3062 method. When using the S3062 as a SONET/SDH generator with the receive and transmit clocks present, random data should be avoided at the input due to possibility of false framing, which would cause the internal framing counters to jump.

To select the SONET/SDH mode, choose the desired rate by using the RATESEL[1:0] pins, or by writing the corresponding register bits. Differential encoding and decoding, as well as forward error correction, may also be implemented in this mode.

NOTE: Pass-through mode has priority over RATESEL and will negate any RATESEL selections if pass-through mode is enabled.

Figure 4 Detailed Block Diagram



3 ARCHITECTURE/FUNCTIONAL DESIGN

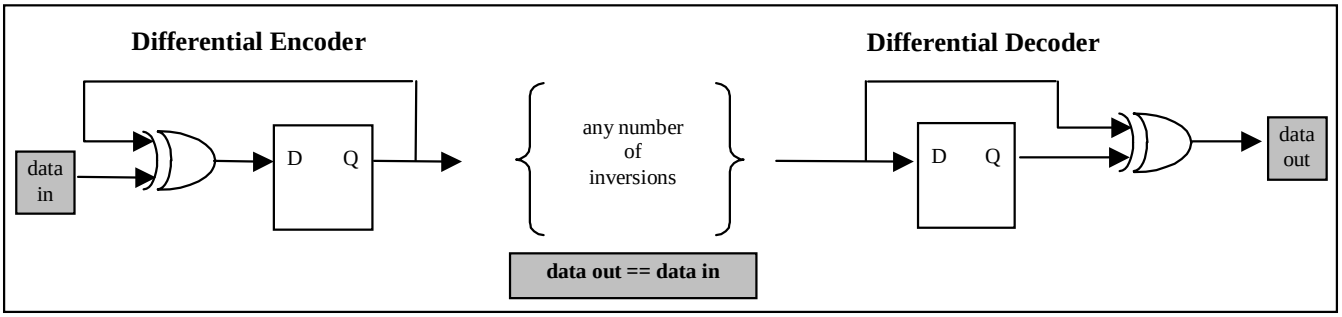
3.1 Detailed Operation -- Pass Through, Differential Encoding, Forward Error Correction

As shown in Figure 4 , the received data enters the chip and is de-multiplexed from 16-bits to 32-bits. The data goes to the decode block, if it has been differentially or FEC encoded, or it bypasses the decode block and travels to the re-synchronizing FIFO.

3.1.1 Differential Decoding

The first circuit in the decode block is the differential decoder. It can only be enabled if the 'Differential Decode ON' register bit has been set. The user may wish to differentially encode and decode the data stream if the data outside the S3062 is inverted an unknown number of times. Regardless of the number of inversions, the decoder will always output the exact data that was received by the encoder.

Figure 5 Serial Differential Encoder and Decoder

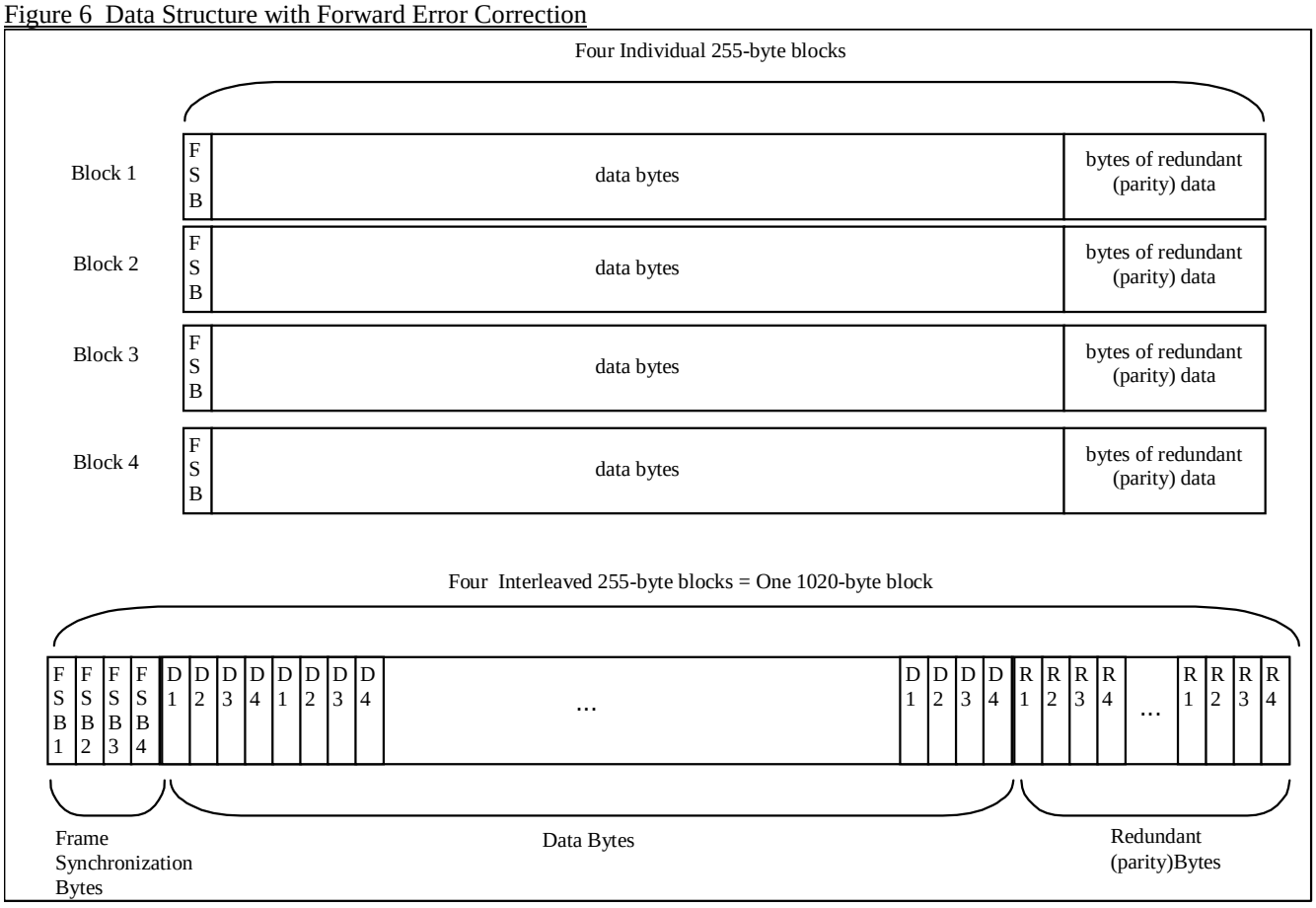


3.1.2 Forward Error Correction (FEC) Decoding

Data may pass from the differential decoder to the FEC decoder. The FEC_DEC signal pin must be tied high to power-up this block and enable this feature. The FEC_DEC signal has an internal weak pull-down on it to disable decoding if the input pin is not connected. Once the pin has been tied high, software, if present, may disable the feature through the 'FEC Decode OFF' register bit.

The decoder locates the FEC byte boundaries by aligning to the Frame Synchronization Byte (FSB). The default value for this byte is 3Ch, but it is reprogrammable through the 'FSB' register. A FSB is sent as the first byte of a 255-byte block. In the S3062, the blocks are interleaved such that 4 FSBs will be received one after the other followed by the rest of the four interleaved 255-byte blocks. The following figures show the FEC encoded data structure.

Figure 6 Data Structure with Forward Error Correction



The decoder synchronizes to the four FSBs, going in-frame after receiving 2 consecutive groups, spaced the correct distance apart (4*255 bytes). By default, all of the bits in the 4-FSB group are checked. If some of the FSB bits are being robbed for a data link, software can program the S3062 to only check the remaining real FSB bits for the framing value.

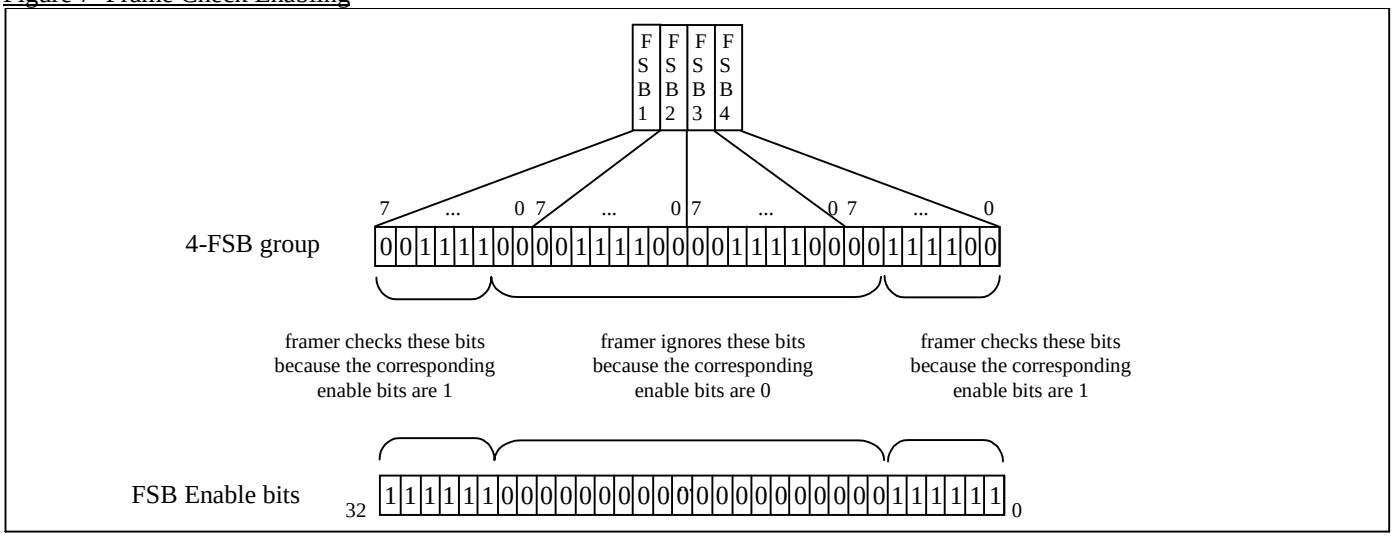
After frame has been found, the framer keeps looking for the 4-FSB groups at the correct spacing. It goes out of sync after seeing 4 consecutive bad groups. To make the algorithm more robust to bit errors, by default, only the 6 most and 6 least significant bits in the 4-byte group are checked once the framer is in-frame. For example, in Figure 6 above, the bits checked would be the 6 most significant bits of FSB1 and the 6 least significant bits of FSB4. This, again, can be changed by software.

The defaults, used in the framing algorithm, which software can change are as follows.

- The number of consecutive error-free groups required to go in-frame, default 2, can be changed to any value from 0-15.
  If the value 0 is selected, framing will not occur correctly.
- The bits within the 4-FSB group to check when out-of-frame can be changed by writing to the 'FEC Out-of-Frame FSB Check Enable' register. The default register value is FFFF FFFFh, check all bits.
  If too few bits are selected, framing will not occur correctly.
- The number of consecutive erred groups required to go out-of-frame, default 4, can be changed to any value from 0-15.
  If the value 0 is selected, framing will not occur correctly.
- Which bits within the 4-FSB group to check when in-frame can be changed by writing to the 'FEC In-Frame FSB Check Enable' register. The default register value is fc00 003fh, check 12 bits.
  If too few bits are selected, framing will not occur correctly. If too many bits are selected, the framer will be more likely to go out-of-frame when the bit error rate is high.

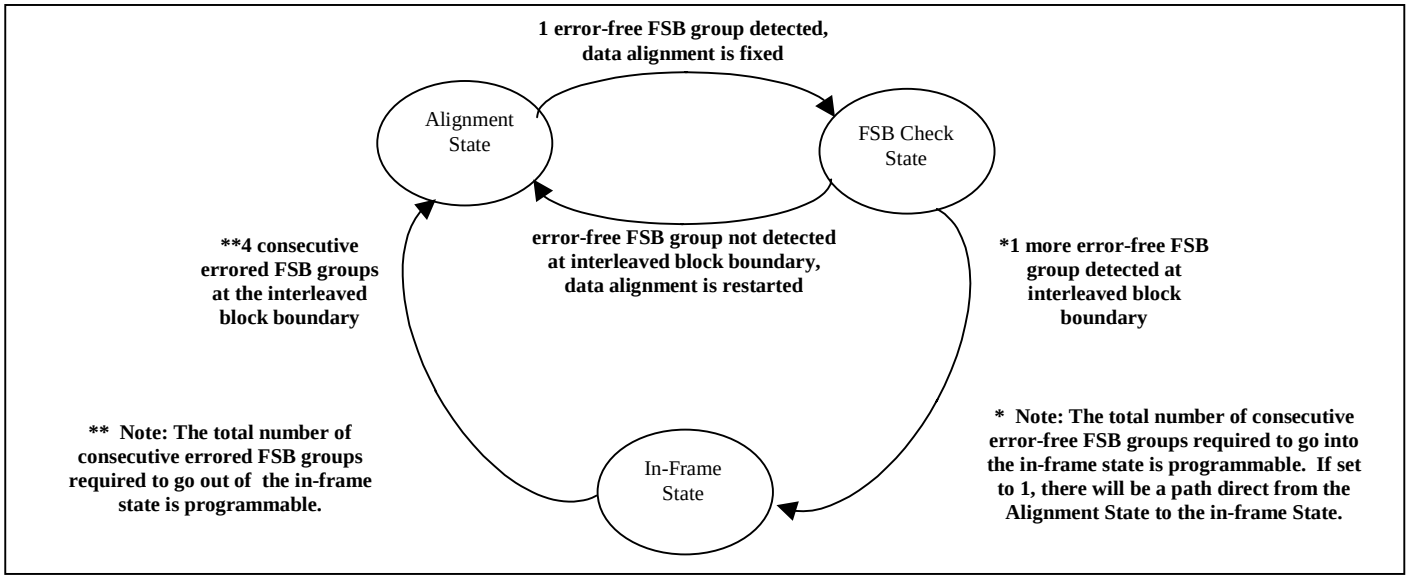
The frame check enable registers work as follows: each bit in the 32-bit register represents a bit in the 4-FSB group. If the enable for a particular bit is on (1), the bit will be checked. See the following figure.

Figure 7 Frame Check Enabling



The FEC_ERR signal pin is asserted when the decoder is out-of-frame. An interrupt is also asserted in the interrupt registers upon transitions to and from out-of-frame. The following figure shows the framing state machine:

Figure 8 Forward Error Correction Framing State Machine



Once the data is aligned, it is checked with the S3062 Reed Solomon (RS) decoder. Reed Solomon encoding consists of generating parity bytes that are an algebraic function of the user data. There are 2*T parity bytes added to the payload data, where "T" is the number of correctable bytes in the block. The decoder computes 2*T syndromes of the received FEC block, including the FSB, and

computes an error locator polynomial as well as a magnitude polynomial from the 2*T syndromes. These latter two polynomials provide the information necessary to detect and correct the erred bytes (up to T bytes per FEC block).

If the decoder detects an error it can correct, it does so whether the error is in the FSB, the data or the parity bytes themselves. It also keeps statistics on the number of errors and the error type. There is a count for the number of 1s corrected, the number of 0s corrected and the total number of bits and the number of bytes corrected. Since up to 8 errors can be corrected per byte, the number of bytes corrected can be as much as 8 times less than the number of bits corrected.

There is also a count for uncorrectable frames, those that have more than T errors in them. In those frames, the bits and bytes, which are corrected, are still counted and the uncorrectable frame count is incremented. The user should be aware that it is not possible to guarantee that the circuit will be able to find all of the uncorrectable frames. If the frame has been corrupted in such a way that it still looks like a valid frame, it will be treated as such. Therefore, if the user sees uncorrectable frames, there is a reasonable chance that there were more uncorrectable frames than those which were counted. Furthermore, the corrected bit and byte counts become suspect since some of the bits and bytes "corrected" may have been corrupted instead.

All of the error counts run continuously, regardless of whether the FEC decoder is in or out-of-frame. Software must ignore the counts when the decoder is out-of-frame and ignore the first count read when the decoder goes in-frame. The counts accumulate for a period delineated by the 1-second tick, which can be sourced from the PM_CLK signal pin or the ‘PM Tick’ register bit. Upon receiving each tick, the count is transferred to a software-readable register and the count is cleared. The counters do not saturate at a maximum value, they reset to zero and begin counting again when the maximum value is reached. The user must transfer the values from the FEC counters to the FEC count register within the recommended one-second time interval. This will insure that the transferred value accurately represents the number of errors that had occured.

The number of bytes corrected is also indicated on the FEC_ERR pin. It is held high for two CLKOUTP/N clock periods for each byte corrected. It is held high for the whole of an uncorrectable frame. A whole 1020-byte frame is output in 510 ticks since the S3062 has a 2-byte wide interface (16 bits). The FEC_ERR pin is also held high when the decoder is out-of-frame. Between errors, the FEC_ERR pin is held low for two CLKOUTP/N ticks. Thus, if a FEC uncorrectable frame is followed by a FEC frame with 2 corrected bytes, the signal will be high for 510 ticks, low for 2, high for 2, low for 2, high for 2 and then low until the next error is seen.

3.1.3 FEC Data Link

The FEC framer can be programmed to ignore certain bits in the 4-byte FSB group when those bits are used for a data link. The data link bits, used for the received data link, are defined by the ‘FEC Out-of-Frame FSB Check Enable/Data Link Bit Selection’ register. If the ‘RX FEC Data Link ON’ register bit is enabled, the appropriate bits are copied from the FSB group and shifted serially out, LSB first, of the ‘FEC Receive Data Link Out’ pin (RX_FEC_DL) along with a clock (RX_FEC_DLCK). The clock only runs when there is data to be output; it is a gapped clock with a frequency of CLKINP/N divided by 12. Since the S3062 may accept input clocks from 155.52MHz/16 to 2678.57MHz/16, the serial clock output can vary from 810kHz to 13.95MHz.

NOTE: The in-frame data link availability should match the out-of-frame data link selection for the received data link to function properly. Also, the data link may only be enabled when a processor is connected and active by loading the Micro Present byte with a value of 59h.

In the reverse direction, if the ‘TX FEC Data Link ON’ bit is enabled, a serial clock is provided on the TX_FEC_DLCK pin, which is the TXCLKP/N divided by 12, and data is brought in from the ‘FEC Transmit Data Link’ (TX_FEC_DL) I/O pin. The data is inserted into the 4-byte outgoing FSB group in the locations specified by the ‘FEC Encode FSB/Data Link Bit Selection’ register.

If data link bits have been defined in both the decode and encode FSBs, but the data link add has not been enabled, the data in the link will be passed through. For this to work correctly, the data rate entering the link must be the same as the data rate going out. Therefore, both the FEC decode and FEC encode must be enabled with the same number of bits and error correction rate for the data

link to be identical in both receive and transmit FSBs. Note that the number of bits in the FSBs must be the same, not the actual locations of the bits. Table 1 shows a summary of how the data link works given that the appropriate FSB bits have been enabled.

Table 1 Data Link Enable

RX FEC Data Link ON	TX FEC Data Link ON	Data Link Description
0	0	Pass-through: data link bits in RX FSBs are copied to the bits in the TX FSBs
0	1	Insert Only: data link information is taken from the TX_FEC_DL pin and inserted in the TX FSBs
1	0	Drop and Continue: data from the RX FSBs goes out on RX_FEC_DL and is copied into the TX FSBs
1	1	Drop and Insert: data from the RX FSBs goes out on RX_FEC_DL. Data from TX_FEC_DL is inserted into the TX FSBs

The user may define anywhere from 0 to 32 of the FSB bits to be used for the data link. The more bits used for the data link, the fewer there will be available for the FSB framer. If all bits are used for the data link, the framing will not work. It is recommended that the user limit their bit selections. To determine the data link rate obtained from the chosen data link bits, use the following equation:

LINK RATE = (number of bits chosen for the link / (4*255 bytes * 8bits/byte)) * data rate in bits/sec

For example, consider a 1.25GHz Gigabit Ethernet link encoded with FEC providing 8 bytes/255 bytes error correction capability. FEC encoding increases the data rate as shown in the FEC Algorithm section 3.1.8. In this example, the data rate is 1.25GHz * 255/238 = 1.34GHz. If 8 bits are stolen from the FSB for the data link, the data link bit rate is 8/(4*255*8) * 1.34Gb/s = 1.3Mb/s.

3.1.4 FIFO†

Regardless of whether or not the data goes through the FEC decode, differential decode, both or neither, it must run through the FIFO to become aligned with the transmit clock. The transmit clock may be identical to the receive clock or it may have a different phase or different frequency. It is recommended that the transmit clock (TXCLKP/N) be derived from the receive clock to minimize unintentional FIFO recentering. In all cases, the FIFO free-runs when the receive clock is missing. The FIFO is simply a 256 x 32 bit circular memory with the write address running on the receive clock (divided down CLKINP/N) and the read address running on the transmit clock (divided down TXCLKP/N). When the S3062 is reset the addresses also reset, offset by 180 degrees. The FIFO is used as follows:

1) If FEC is not enabled, the transmit clock is the same frequency as the receive clock and the FIFO handles the possible phase difference between the two clocks.

2) If data coming into the S3062 is FEC encoded, but the data going out is not, the frequency of the receive clock is higher than the transmit clock because of the extra frame synchronization and parity bytes. Those extra bytes are not sent through the FIFO. The FIFO acts like an elastic store, passing data bytes, but not the FSB or parity bytes. This shows how the frequency difference is handled internally by the FIFO.

3) If data entering into the S3062 is not FEC encoded, but the data going out is, the frequency of the transmit clock is higher than that of the receive. The extra FSB and parity bytes, however, are not added to the data stream until after the FEC encode block. Prior to that block, there are fewer data bytes than clock ticks so that an internal signal is used to stop the data flow when the

† Specific revisions of the silicon will require an external reset if the clock inputs to the S3062 become unstable. Please consult Errata 7.5, FIFO Recentering, in the back of the data sheet for details.

FSB and parity bytes are being sent out. The FIFO again acts like an elastic store, receiving data bytes with the slower receive clock and only sending them out with the faster transmit clock when not halted. Thus it handles the frequency difference.

4) If data entering into and leaving the S3062 is FEC encoded, the receive side stores data bytes into the FIFO as mentioned in point (2) and the transmit side only takes data out when it is not halted by the internal stop signal, as mentioned in point (3). The FIFO again works as an elastic store.

Since the transmit clock is derived from the receive clock externally to the S3062, the FIFO's read and write addresses will not normally overtake each other. However, if the addresses do come within 2 to 6 addresses of each other, the S3062 will force them back apart and indicate the re-centering with an interrupt. At reset, the addresses start 180 degrees apart. If the FEC decoder is OFF, data starts passing through the FIFO immediately. If the decoder is ON, no data goes through until the FEC framer is synchronized and one frame has been decoded.

Note that if the transmit clock has the capability of free running when the receive clock has failed, all but the FEC and differential decoding portions of the chip will continue to function. This will permit a signal (in the case of SONET/SDH, a valid line AIS signal) to be sent out so that downstream devices will not also lose clock.

3.1.4.1 FIFO Re-Centering

If the S3062 is operating with the use of an external PLL (and FEC decode is OFF), the FIFO pointers may have to be re-centered to avoid an unexpected address collision due to clock drift or another unexpected event.

When the transmit clock is generated from the receive clock through an external PLL circuit, it may drift from the receive clock's frequency until the PLL has locked. While the clocks are drifting, the FIFO pointers will move closer to each other. When the PLL circuit has finally locked, the pointer positions relative to each other are unknown and should be pushed 180 degrees apart to prevent unexpected collisions due to clock drift or another unexpected event. If the FEC_ENC pin is enabled, software may force the FIFO to re-center by changing the FEC capability in the 'FEC Encode General Controls' register – see Tables 2 & 3 below for a FEC capability change list. A valid but incorrect value in these registers will cause the S3062 to remove more, or fewer, bytes than it should within the FIFO, forcing the read and write pointers to collide. The collision will trigger an interrupt indicating that the FIFO has re-centered. Software may then service the interrupt and change the 'FEC Capability' bits to their normal values before the pointers move significantly from their initialized positions, 180 degrees apart.

For example, if the FEC capability is set to 8-byte correction, each 255-byte block has 238 bytes of data, 1 FSB byte and 16 redundant bytes. If the capability is set to 7-byte correction, each 255-byte block has 240 bytes of data, 1 FSB byte and 14 redundant bytes. Therefore, if the chip is supposed to be generating 8-byte correction and the user changes it to 7-byte correction, 2 (240-238) extra data bytes will be removed from the FIFO each time a 255-byte block passes through the FIFO. The read pointer will move 2 locations closer to the write pointer per 255-byte block. If the read pointer starts 180 degrees (256 locations) away from the write pointer, they will collide within 128 (256/2) 255-byte blocks. When a collision occurs, the hardware forces the pointers 180 degrees apart again.

The system designer may wish to initiate FIFO re-centering when the PLL loses lock and re-finds it again. The PLL must find lock for the first time after a power-up or anytime the receive clock fails. When the receive clock is determined to be valid, the software should:

- Check that the chip's controls are set correctly or initialize the chip. (To initialize, set all the control bits and then enable software control by writing 59h to the Micro Present byte.)
- Wait for the PLL to lock (TBD seconds after power-up or TBD seconds after the receive clock is applied).
- Force the FIFO to re-center by changing the encode 'FEC Capability' bits.
- Wait for the FIFO re-centering interrupt located in the 'Special Interrupt Register'.
- Quickly fix the 'FEC Capability' bits before the pointers have time to move apart.

Depending on how fast the pointers are moving apart, software may wish to simply wait for the FIFO re-center interrupt and then respond to it, or it may wish to stop all other processes and run a tight polling loop waiting for the FIFO re-center interrupt to occur. See the following tables to determine how fast the pointers will be moving apart.

- If the byte correction is changed by 1, the pointers will move apart 2 locations every 255 bytes (as described in the example above). This is the slowest the pointers will move.
- If the byte correction is changed by 8, (i.e. from FEC encode ON, 8 byte correction to FEC encode OFF), the pointers will move apart 17 locations every 255 bytes. (255 bytes of data will be removed from the FIFO every block instead of 238. 255 - 238 = 17.) This is the fastest the pointers will move.
- The time required to output 255-bytes is 255 * 2 * TXCLK = 510 * TXCLK.

The pointer location change is given by Table 2 and Table 3 for 1 255-byte frame (510*TXCLK), 2 255-byte frames (1020*TXCLK) and 3 255-byte frames (1530*TXCLK).

Table 2 FIFO LOCATION CHANGE: To or From 'ENCODER OFF'

POINTER LOCATION CHANGE CAUSED BY CHANGING TO/FROM THE BYTE CORRECTION VALUE TO/FROM 'ENCODER OFF'						
	Each Column Headers Specifies the Change in Correction Value to or from 'ENCODER OFF'					
TIME	**8-BYTE CORRECTION**	**7-BYTE CORRECTION**	**6-BYTE CORRECTION**	**5-BYTE CORRECTION**	**4-BYTE CORRECTION**	**3-BYTE CORRECTION**
510*TXCLK	17 FIFO Locations	15 FIFO Locations	13 FIFO Locations	11 FIFO Locations	9 FIFO Locations	7 FIFO Locations
1020*TXCLK	34 FIFO Locations	30 FIFO Locations	26 FIFO Locations	22 FIFO Locations	18 FIFO Locations	14 FIFO Locations
1530*TXCLK	51 FIFO Locations	45 FIFO Locations	39 FIFO Locations	33 FIFO Locations	27 FIFO Locations	21 FIFO Locations

Table 3 LOCATION CHANGE: To or From Byte Correction Values

LOCATION CHANGE CAUSED BY CHANGING THE ENCODER BYTE CORRECTION VALUE BY THE NUMBER OF LISTED BYTES					
	Each Column Header Specifies the Byte Correction Value Change				
TIME	**1-BYTE CHANGE**	**2-BYTE CHANGE**	**3-BYTE CHANGE**	**4-BYTE CHANGE**	**5-BYTE CHANGE**
510*TXCLK	2 FIFO Locations	4 FIFO Locations	6 FIFO Locations	8 FIFO Locations	10 FIFO Locations
1020*TXCLK	4 FIFO Locations	8 FIFO Locations	12 FIFO Locations	16 FIFO Locations	20 FIFO Locations
1530*TXCLK	6 FIFO Locations	12 FIFO Locations	18 FIFO Locations	24 FIFO Locations	30 FIFO Locations

Examples:

- The fastest the pointers could move is in a system with 2.5Gbps data and when the byte correction value is changed from FEC encode OFF to FEC encode ON, 8-byte correction. At 2.5Gbps the TXCLK will be running at 156.25MHz (6.4ns) and the read pointer will move closer to the write pointer by 17 locations every (510 * TXCLK) = (510 * 6.4ns) = 3.264µs. Thus the pointer will move 17 locations every 3.264µs.

- The slowest that the pointers could move is in a system with 155.52Mbps data and when you have a 1-BYTE correction value change. At 155.52Mbps the TXCLK will be running at 9.72MHz (102.88ns) and the read pointer will move closer to the write pointer by 2 locations every (510*TXCLK) = (510 * 102.88ns) = 52.47µs. Thus the pointer will move 2 locations every 52.47µs.

3.1.5 FEC Encode

After the FIFO, the data may be selected by the pass-through MUX to pass data to the FEC encode block. Like the FEC decode, this function can be turned ON or OFF from a signal pin (FEC_ENC). (The FEC_ENC signal has an internal weak pull-down on it to disable encoding if the input pin is not connected.) Once the pin has been tied high, software, if present, can disable the feature through the FEC Encode OFF register bit to permit encoding to be turned OFF and ON during tests. The encoder inserts the FSB at the front of each block of bytes and then generates the parity bytes required for error correction over the FSB and data bytes. Note that both the error correction capabilities of the encoded link and the FSB value sent by the encoder can be different than that expected by the decoder. By default, however, they are the same.

If the data link bits have been selected in the 'FEC Encode FSB/Data Link Bit Selection' register, the encoder brings data into the link from the 'FEC Transmit Data Link' (TX_FEC_DL) I/O pin or it is passed through from the received data link. The choice of which data is transmitted is determined from the 'TX FEC Data Link ON' register bit but both decode and encode data links must be defined for the data to be passed through. For this to work correctly, the data rate entering the link must be the same as the data rate going out. Therefore, both the FEC decode and FEC encode must be enabled with the same error correction rate and the number of bits defined for the data link must be identical in both receive and transmit FSBs. Note that the number of bits in the FSBs must be the same, not the actual locations of the bits. Table 1 shows a summary of how the data link works given that the appropriate FSB bits have been enabled.

3.1.6 Error Injection

Errors may be injected into the data if software is present. The user may select:

- which stream(s) to corrupt out of the 4 interleaved streams
- whether to corrupt the FSB or the data bytes
- which bits in a byte should be corrupted

If data bytes are to be corrupted, the user may also select:

- the number of bytes in each 255-byte block to be corrupted (up to 15).

The FEC encoder must be enabled to inject errors into the FSB. When the encoder is enabled and the 'FSB/DATA Errors' register bit is enabled (FSB error injection is selected), errors will only appear in the FSB (up to 4 bytes). If the 'FSB/DATA Errors' register bit is disabled (data error injection is selected), errors will only appear in the data (up to 15 bytes) and the state of the FEC encoder is ignored.

Without the FEC turned ON, the notion of streams does not exist, but the data is still arranged inside the chip as a 4-byte wide path. For Example: If the user specifies 4-bytes of corruption on stream #4, the least significant byte of the internal data path will be corrupted for the first four words every 255-bytes. If the data is looked at externally to the S3062, byte by byte after the streams have been interleaved, the errors will show up every 1020-bytes in byte numbers 4, 8, 12 and 16.

NOTE: When injecting errors in the data and FEC encoding is enabled, the error injection circuit always chooses the first 15 data bytes (in the selected streams) after the FSB to corrupt. Thus, it will never corrupt the FEC parity bytes.

3.1.7 Differential Encode

Following the error injection is the differential encoder which, may only be enabled from the 'Differential Encode ON' register bit. If there is no device connected to the processor interface, neither differential encoding nor differential decoding may be turned ON.

After leaving the differential encoder the data is multiplexed back up to 16 bits and exits the chip. All the SONET/SDH and Gigabit Ethernet monitoring circuits shown in Figure 4 are powered down if the S3062 is in pass-through mode; thus, less power is consumed than in other modes. The FEC blocks are also powered down if they are not enabled. To select pass-through mode without a processor connected to the chip, assert the PASSTHRU signal on the I/O pin. With a processor connected, write a '1' to the 'Pass-Through' register bit and enable software register control by writing a 59h to the Micro Present byte. Controls set by the processor override signals on the I/O control pins when the Micro Present byte contains a value of 59h.

3.1.8 Forward Error Correction (FEC) Algorithm

The S3062 algorithm is based upon the (n,k) Reed Solomon Code where n is the block length of the code and k is the number of user symbols per block. The code is defined over the Galois field (2^8) resulting in symbols of eight bits, i.e. a byte. It belongs to the family of systematic[‡] linear cyclic[§] block codes[**] based on the generator polynomial given by:

$$G(x) = \prod_{i=0}^{2T-1} (x-\alpha^i)$$

where T = (error correcting capability of the RS-Code)
and α^0 = 01 hex and α^1 = 02 hex, over the primitive polynomial
$P(x) = x^8 + x^4 + x^3 + x^2 + 1$ on $GF(2^8)$

Where α is a root of the primitive polynomial $x^8 + x^4 + x^3 + x^2 + 1$. A data byte ($d_7$, d_6 . . . d_0) is identified with the element $d_7 * \alpha^7 + d_6 * \alpha^6 + \ldots + d_0$ in GF(256), the finite field with 256 elements. The "rate" of the code is defined as the ratio of the total symbols in a block to the user data symbols. Since, in this case, symbols are bytes, the code rate is the total number of bytes in a block divided by the number of the user's data bytes in the block. The S3062 supports six different code rates, all based on the same generator polynomial.

Table 4 RS Code Rate Expansion

Reed-Solomon Code	Error Correcting Capability	Code Rate Showing Bandwidth Expansion due to Code Words & FSB	Example of Increased Input Clock Frequency for STS-48/STM-16 (MHz)
(255,239)	8 bytes per 255-byte block	255/238 = 7.14% increase	155.52*255/238 = 155.52 * 15/14 = 166.63
(255,241)	7 bytes per 255-byte block	255/240 = 6.25% increase	155.52*255/240 = 155.52 * 17/16 = 165.24
(255,243)	6 bytes per 255-byte block	255/242 = 5.37% increase	155.52*255/242 = 163.87
(255,245)	5 bytes per 255-byte block	255/244 = 4.51% increase	155.52*255/244 = 162.53
(255,247)	4 bytes per 255-byte block	255/246 = 3.66% increase	155.52*255/246 = 155.52 * 85/82 = 161.21
(255,249)	3 bytes per 255-byte block	255/248 = 2.82% increase	155.52*255/248 = 159.91

NOTE: The Frame Synchronization Byte is not defined as a user data byte in the code rate bandwidth expansion definition above.

The S3062 internally divides the data down into four steams to reduce the internal clock speed. Each stream has a dedicated RS codec that may correct up to 8 erred bytes. Since the four codecs are running in parallel, a burst of 32 erred bytes may be corrected.

[‡] With a 'systematic' code, the encoder does not modify the user's data, it just uses it to generate redundant bytes which it then appends to each block. See figure 6.

[§] Given a 'cyclic' code, the data bytes and redundant bytes can be rotated as a unit and error correction will still work. This is just of interest to theorists since the user will find the data unrecognizable with each block of bytes having some of the parity bits shifted into them.

[**] A 'block code' divides the data up into blocks as shown in figure 6.

Thus, the error correcting capability of the S3062 is four times better than what might be expected by looking at the simple error correction capability of the RS algorithm. In the S3062, the RS(255,239) code provides a burst error correcting capability of 32 bytes (4 x 8-bytes) or 256 bits.

The default code used by the S3062 is the RS(255,239). This algorithm puts 1 FSB, 238 data bytes and 16 parity bytes into a block. See Figure 6 for the block format. As shown in the above table, this version of the algorithm can correct up to 8 erred bytes in the 255-byte block. The choice of other code rates allows the user to optimize overall system performance by balancing error-correcting capability against the channel degradation due to rate expansion. The default error correcting code may only be changed by programming the 'FEC Capability' register bits.

When FEC is bypassed or when full FEC (both decoding and encoding) is enabled, the input clock rate to the device is equal to the output clock rate and no external clock circuitry is required as shown in Figure 10 . When the S3062 is used for encoding only, or for decoding only, the input clock rate and output clock differ in proportion to the rate expansion factor listed in bold face in Table 4 . To simplify the generation of the appropriate clock rates, the S3062 provides internal dividers driven from both the receive clock signal (CLKINP/N) and the transmit clock (TXCLKP/N). The result of the receive clock divider is output on the FEC_RDIV signal pin. The transmit clock divider output runs to the FEC_TDIV signal pin. They should be connected to an external phase detector, loop filter and VCO as shown in Figure 9 .

The default values for the dividers are set for the default (255, 239) code and adjusted based on the state of the FEC_DEC and FEC_ENC signal pins.

Table 5 RX/TX Clock Divider Default Values

FEC_DEC	FEC_ENC	RX Clock Divider	TX Clock Divider	Description
0	0	4	4	Neither encode nor decode: data stream without FEC
0	1	14	15	Encode only: start of system-wide FEC data stream
1	0	15	14	Decode only: end of system-wide FEC data stream
1	1	4	4	Encode and Decode: middle of system-wide FEC data stream

If the Micro Present byte is active and the dividers are required, software must program the required values into the divider's registers. Normally the clock dividers should be programmed to be either 255/248, 85/82, 255/244, 255/242, 17/16 or 15/14 to match the error corrections of 3, 4, 5, 6, 7 or 8 respectively. If the user has supplied a different clock to the transmit section of the chip than the one derived from the receive clock, the dividers may need to be programmed with different values. Software is permitted to program in any value in the range of 1 to 255. The programmer should bear in mind, however, that the output pins are not capable of sourcing any signal faster than 83.7MHz; therefore, if the RX clock is 155MHz, the RX divider must not be programmed to 1.

Figure 9 Required External Circuits for FEC Modes: Encode-Only or Decode-Only

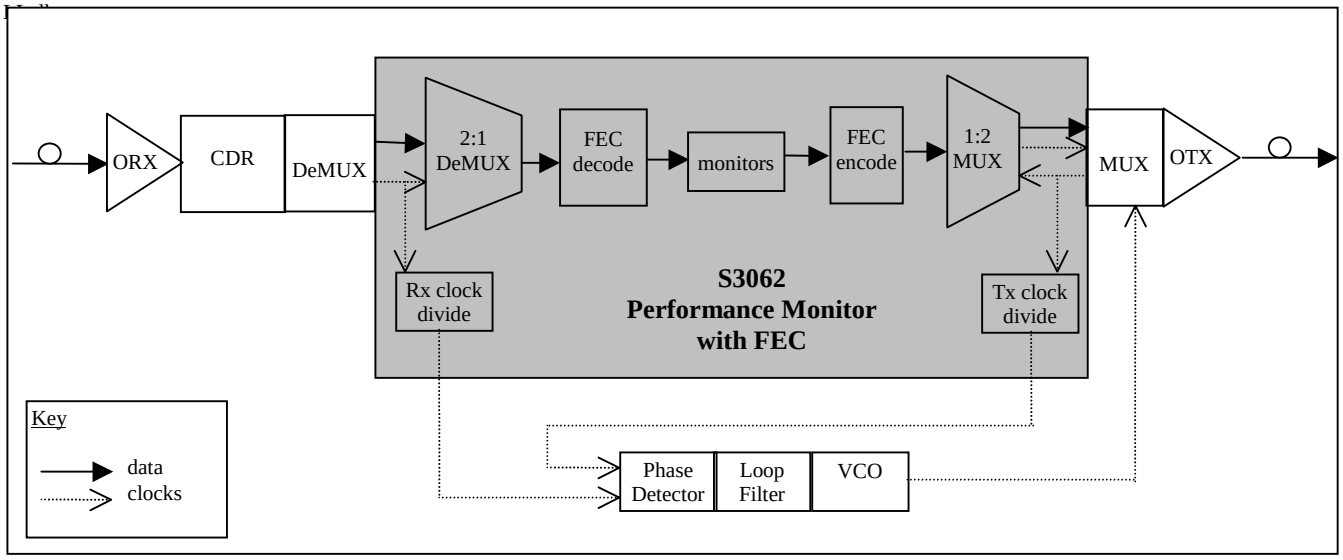
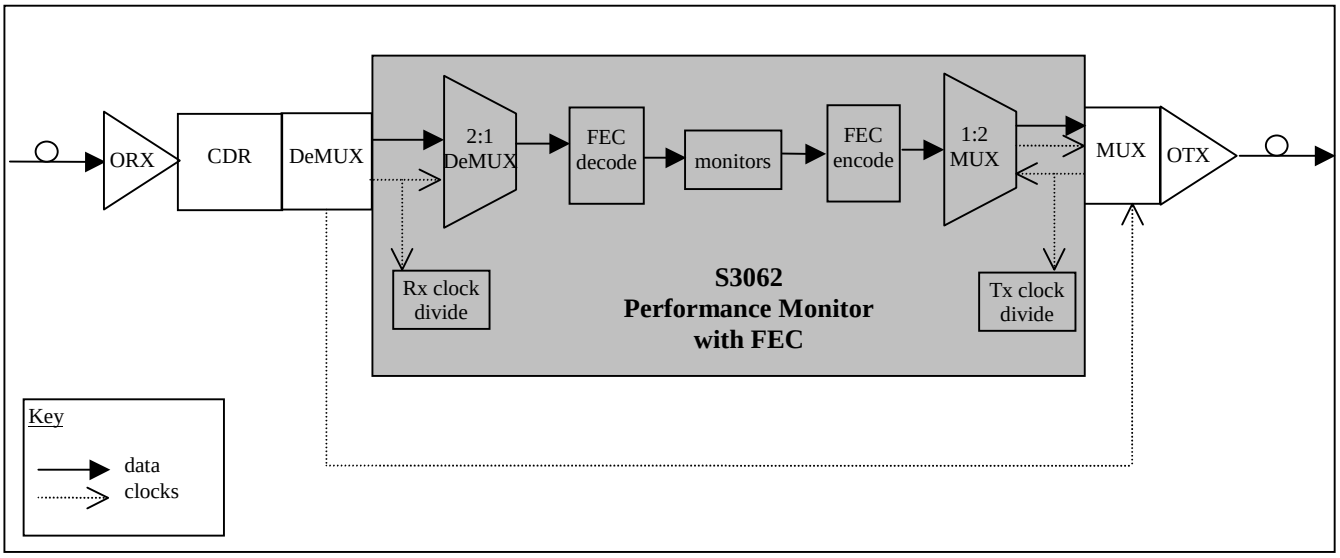


Figure 10 Required External Circuits for FEC Modes: Both Encode and Decode, or Neither Encode nor Decode



3.2 Detailed Operation – Gigabit Ethernet (GBE)

To select Gigabit Ethernet monitoring in the S3062 without a processor connected, assert a '1' on both the RATESEL[1:0] pins. To select this mode via a processor, write a '1' to both rate selection bits and then enable software register control by writing a 59h to the Micro Present byte. Note that the register bits override the signals on the I/O control pins when the Micro Present byte contains a 59h value.

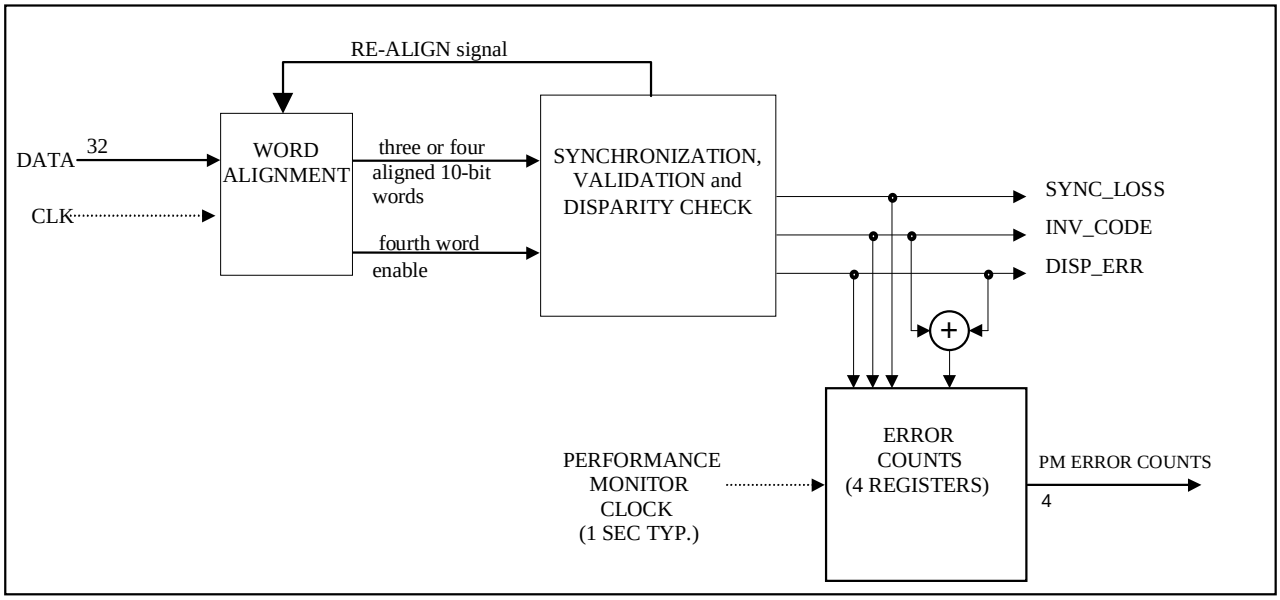
In this mode, the data flows through the chip as if it were in pass-through mode, but it is also routed to the Gigabit Ethernet monitors from the 32-bit internal bus.

NOTE: Pass-through mode has priority over RATESEL and will negate any RATESEL selections if pass-through mode is enabled.

3.2.1 Alignment

To find the 10-bit Gigabit Ethernet words, the alignment block searches the 32-bit data either for the 10-bit K28.5* word or for a comma*. The K28.5 alignment value is the default for the S3062 but may be changed to a comma by enabling the IEEE synchronization method, with the 'IEEE ON' register bit. The error monitors run continuously (except when reset is asserted) and are not dependent on the alignment block. Note that the data entering the GBE block is in 32-bit words, while GBE data is aligned on 10-bit boundaries. To handle this difference, the alignment block either outputs three or four 10-bit words, using an enable signal to notify the downstream blocks that the fourth 10-bit word is present.

Figure 11 Gigabit Ethernet Block Diagram



* The K28.5 has two values depending on the current disparity: it is 0011111010 (0fah) if the running disparity is negative and the inverse, 1100000101 (305h) if the running disparity is positive. A comma (0011111 or 1100000) is the most significant 7 bits of the K28.1, K28.5 and K28.7 special characters. K28.1 is 0f9h if the running disparity is negative and 306h if the disparity is positive. Similarly, K28.7 is either 0f8h or 0f7h.

3.2.2 Synchronization

This block checks for synchronization. It is a circuit searching for another K28.5 byte. If one is found with a different alignment, the circuit pulses the SYNC_LOSS signal for 2 CLKOUTP/N periods, sets the sync loss interrupt bit and signals the alignment block to change to the new alignment.

This circuit may be changed to the standardized, IEEE 802.3z state machine if the'IEEE ON' register bit is set. A diagram of the state machine is included in Figure 13 . The IEEE algorithm generates a SYNC_LOSS error indication that is a level signal as opposed to the pulsed signal described above. SYNC_LOSS will be active while synchronization is lost and will be inactive once the state machine synchronizes. When synchronization is lost, the alignment block searches for comma characters with new alignments.

3.2.3 Validation

An error monitor checks the 10-bit words for invalid codes. It indicates that the received character is not a valid codeword considering the current running disparity. Even if the codeword appears in the Valid Code Group Table 36-1&2 in IEEE 802.3z, the current running disparity might disqualify the codeword from being valid. If the codeword does not appear in the IEEE 802.3z table, the codeword is not valid. When an invalid code is found, the INV_CODE I/O pin pulses for two CLKOUTP/N periods.

Only errors in the data stream (i.e. invalid code words) can cause characters composed of more than 6 ones or 6 zeros. The received codeword is used to calculate the new value of running disparity, regardless of the character's validity. The S3062 Running Disparity (RD) determination is defined in Figure 12 . If the received codeword is found in a different column of the 802.3z Valid Data Character table than expected by the Figure 12 flow chart, a RD error will be discovered and an INV_CODE will be declared. This is independent from the parity calculation described in Section 3.2.4.

The RD calculation is only used for codeword validation. A separate RD error count/flag is not available to the user. The user may, however, correlate the parity error count in Section 3.2.4 to the invalid code count to determine the cause of the failure. Consult Table 6 for a failure description.

Figure 12 802.3z RD Column Determination

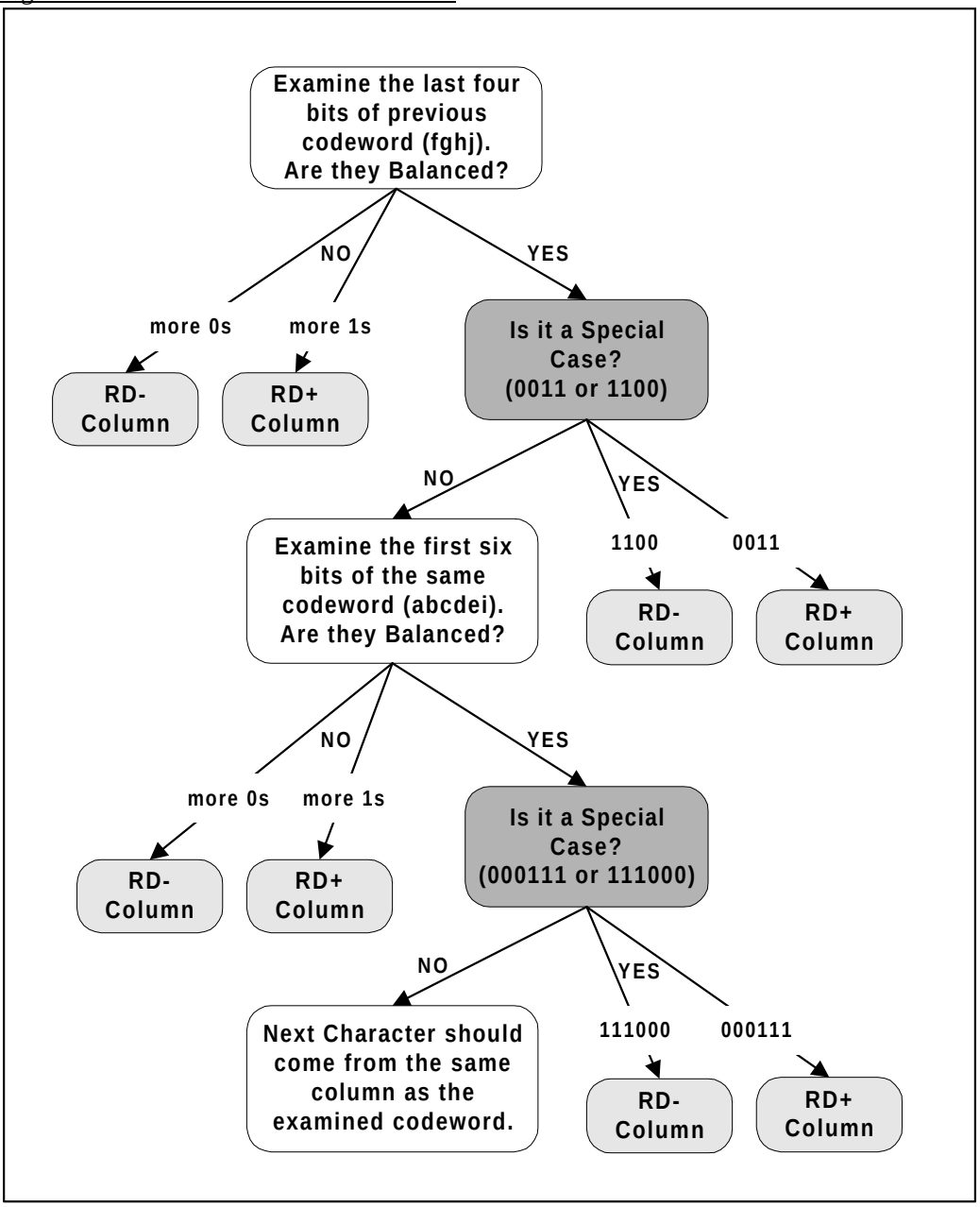


Figure 12 provides the method to determine which running disparity column (RD- or RD+) of the IEEE 802.3z Valid Data Character table to find the next received/sent 8B/10B code word. The last four bits (f g h j) of the previous received/sent codeword are examined first. If the codeword is determined to have more ones or zeros, the desired RD column is determined and the examination of that character may stop. If the bits are balanced (has the same number of ones and zeros) and are NOT a special case (1100 or 0011), the first six bits (a b c d e i) of that codeword must also be examined to determine the RD column location of the next codeword. If the examined six bits turn out to be balanced and are NOT a special case (000111 or 111000), the next codeword will come from the same running disparity column as the examined codeword.

3.2.4 Parity Error

An additional check is performed on the receive codeword which relates to the running disparity properties of the 8B/10B code. Any two occurrences of 10 bit characters composed of 4 logic ones (i.e. 010010 1001), without the occurrence of a character composed of 6 ones (i.e. 111010 0101) in between, is flagged as a parity error. Any number of characters with equal numbers of ones and zeros are allowed between the two characters composed of 4 ones, with no parity error. The same method applies to the alternate case where a character composed of 4 ones is required to separate any two characters composed of 6 ones, each. This mechanism ensures that both the ones and zeros density of the serial data stream are never more than a single bit from 50%, at the boundaries of any two characters. Parity error checking provides simple testing of dc balance but does not perform a full IEEE 802.3z Table 36-1&2 lookup based on an IEEE compliant RD calculation. The parity error checking provides a means of verification of non-IEEE compliant codes, which achieve DC-balance in a similar fashion. The parity error indicator is labeled as DISP_ERR below.

3.2.5 Error and Performance Monitoring Indications.

The error status points (SYNC_LOSS, INV_CODE, and DISP_ERR) are output on individual I/O pins. Additionally, each one of these points generates a maskable interrupt to the processor. In the case of an INV_CODE, DISP_ERR, and a SYNC_LOSS created by the single K28.5 algorithm, an interrupt is generated each time one of the signals pulses. When SYNC_LOSS is created by the IEEE algorithm, an interrupt is generated on both transitions into and out of the synchronization state. The user should note that the only GBE I/O pin indicator that is entirely accurate is the SYNC_LOSS I/O pin. The monitors for invalid codes and parity errors each check up to four words during each clock cycle, but only output one error per clock cycle. Thus, when INV_CODE is active, it represents up to 4 invalid codes. Similarly, when DISP_ERR is active, it represents up to 4 parity errors.

Activity counts for each of these status points are accumulated, individually. SYNC_LOSS activity is only counted when it transitions from in-sync to loss-of-sync for the IEEE mode and counts the number of new alignments found for the default mode. A count of the combined invalid codes and parity errors are also generated. The activity counts are 100% accurate, unlike the error signals on the INV_CODE and DISP_ERR I/O pins.

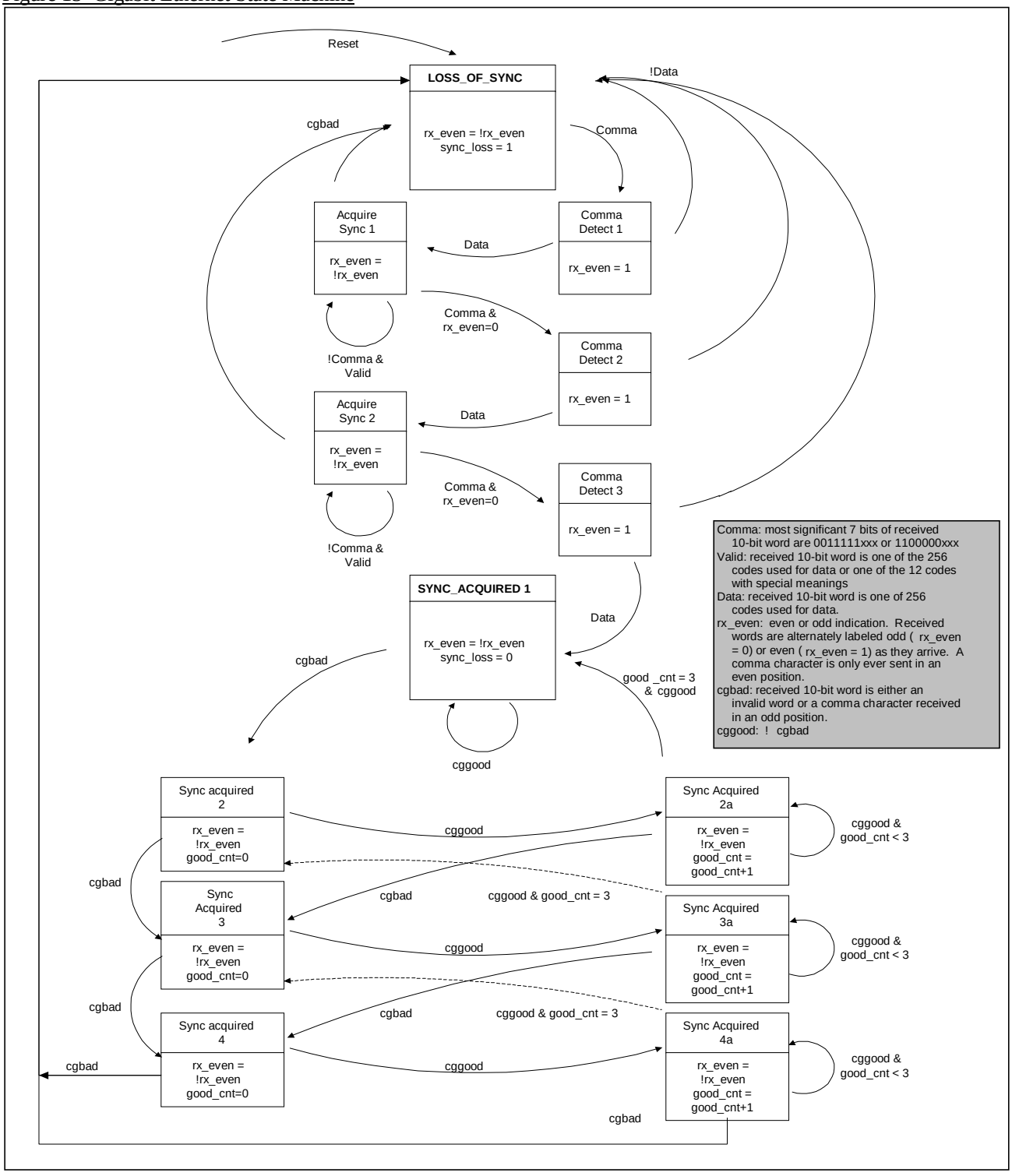
A performance monitoring tick is used to transfer accumulating counts from the count registers into static holding registers that can be read via the processor interface. All count registers are set to zero at the start of a given count cycle. The tick, which typically occurs every second, can come from a clock connected to the PM_CLK I/O pin or, in the case where a clock is not available, from a software write. To enable the tick to come from software, the user must activate the Micro Present byte and enable ‘PM Tick ON’ register bit. Then the user must generate the tick by, every second, writing to the ‘PM Tick’ bit. Note that, in the case that the tick is late, these counters may only hold a maximum of FFFFh errors, after which, they stop counting and maintain the maximum value.

Table 6 describes the effect of certain types of corrupted characters on the invalid codeword and parity error counts. It is intended to be an aid in correlating the corruption type to the error count.

Table 6 Invalid Codeword/Parity Error Correlation

Corruption Type	Invalid Codeword Count	Parity Error Count
Received character appears in IEEE 802.3z table 36-1 or 36-2 and is the correct disparity for the current RD (i.e. it appears in the correct disparity column of the IEEE 802.3z tables). The parity of the character is either neutral or NOT neutral.	No Change	No Change
Received character appears in IEEE 802.3z table 36-1 or 36-2 but does **NOT** match the current RD (i.e. the character appears in the wrong disparity column of the IEEE tables). The parity of the character is neutral (i.e. the character is composed of an equal number of ones and zeros).	Add	No Change
Received character appears in IEEE 802.3z table 36-1 or 36-2 but does **NOT** match the current RD. The parity of the character is **NOT** neutral (i.e. the character does not contain an equal number of ones and zeros).	Add	Add
Received character does **NOT** appear in IEEE 802.3z table 36-1 or 36-2. The parity of the character is neutral.	Add	No Change
Received character does **NOT** appear in IEEE 802.3z table 36-1 or 36-2. The parity of the character is **NOT** neutral.	Add	Parity OK: No Change Parity Error: Add

Figure 13 Gigabit Ethernet State Machine



3.3 Detailed Operation -- SONET/SDH

To turn ON the SONET/SDH functions in the S3062 without a processor connected, connect the RATESEL[1:0] pins to power or ground as shown in the pin description. To select this mode via a processor, write the appropriate value to the 'Rate Select' bits and then enable software register control by writing a 59h to the Micro Present byte. Note that the register bits override the signals on the I/O control pins when the Micro Present byte contains a value of 59h.

NOTE: Pass-through mode has priority over RATESEL and will negate any RATESEL selections if pass-through mode is enabled.

In SONET/SDH mode, the data enters the device through the de-multiplexer or the differential/FEC decoder and enters the FIFO as described in the pass-through section. The data then continues on to the transport overhead monitoring blocks that are described, block by block, in the following sections. The locations of the transport overhead bytes within the SONET/SDH frame are shown in the following two figures.

Figure 14 SONET STS-3c and SDH STM-1 Frames Showing the Transport Overhead

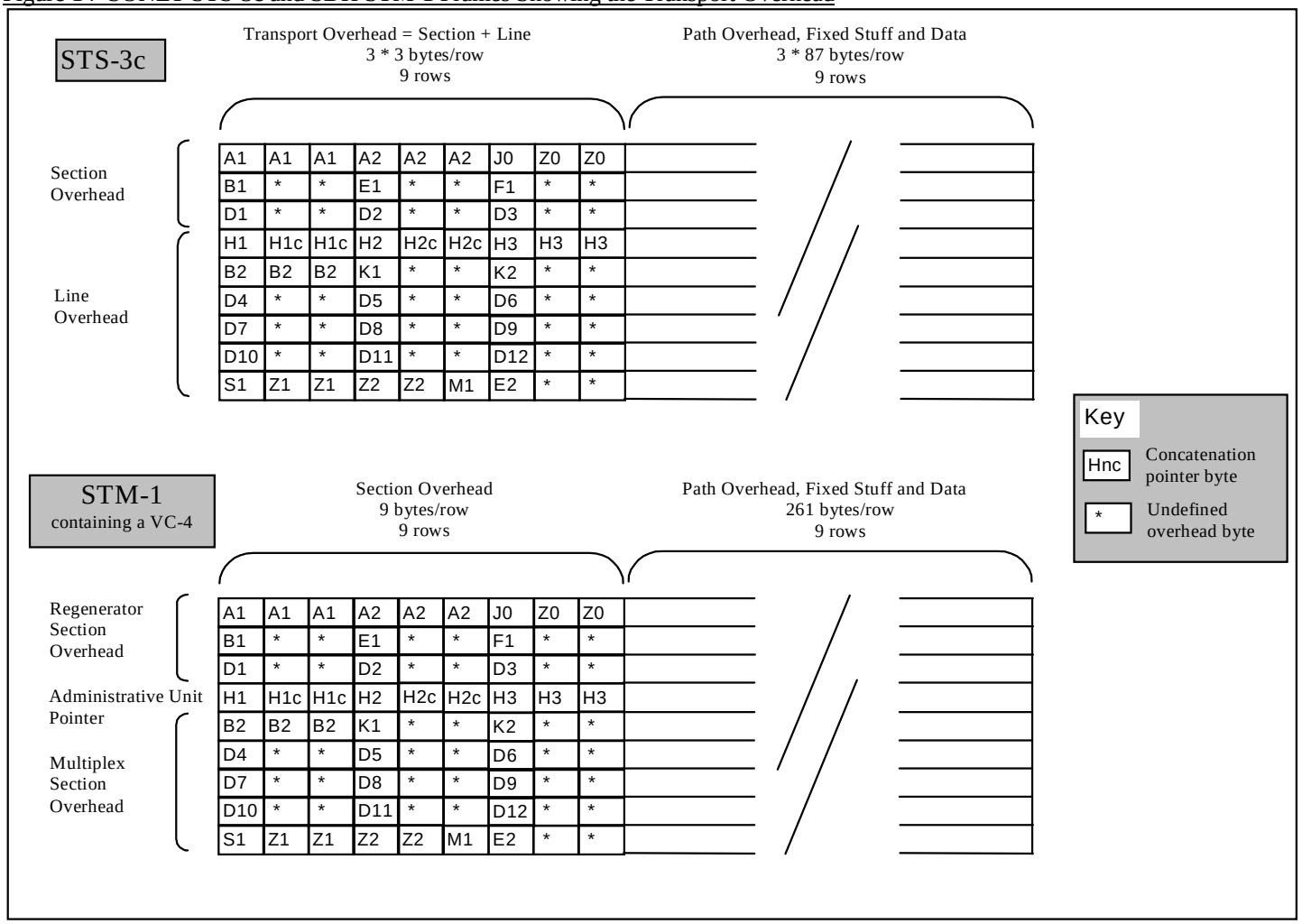
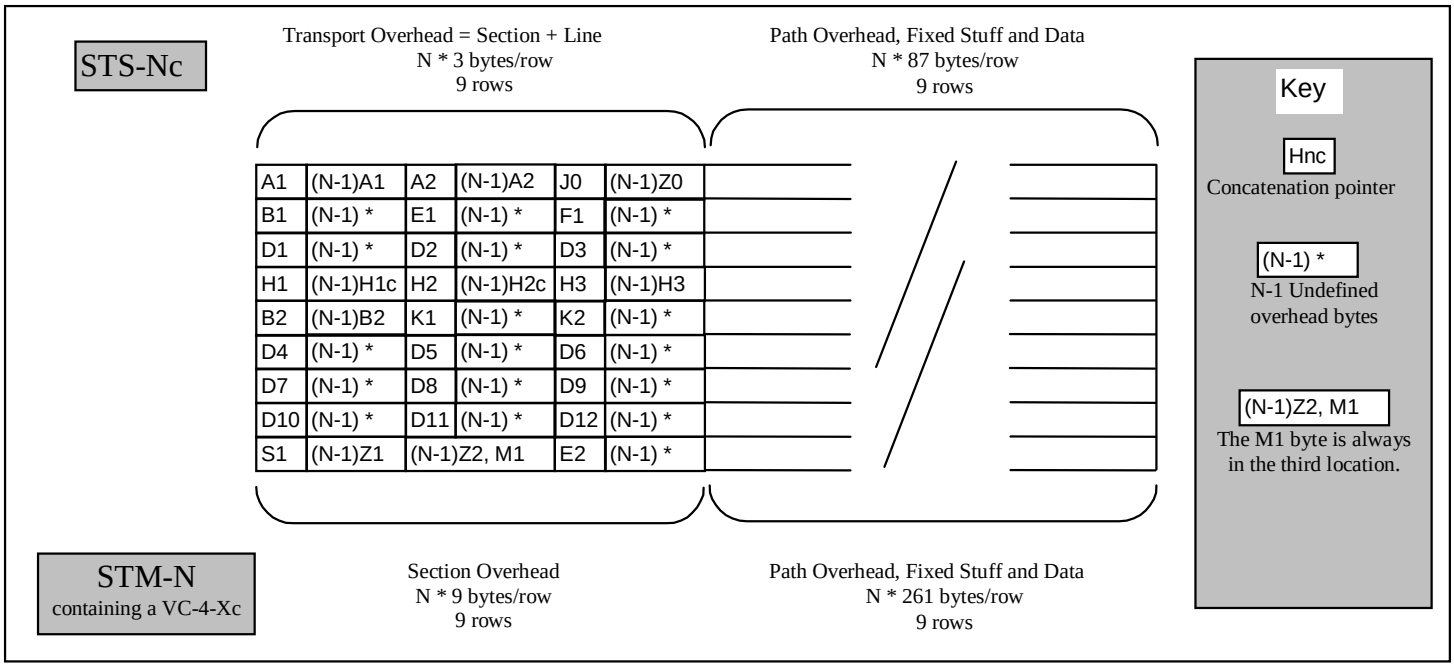
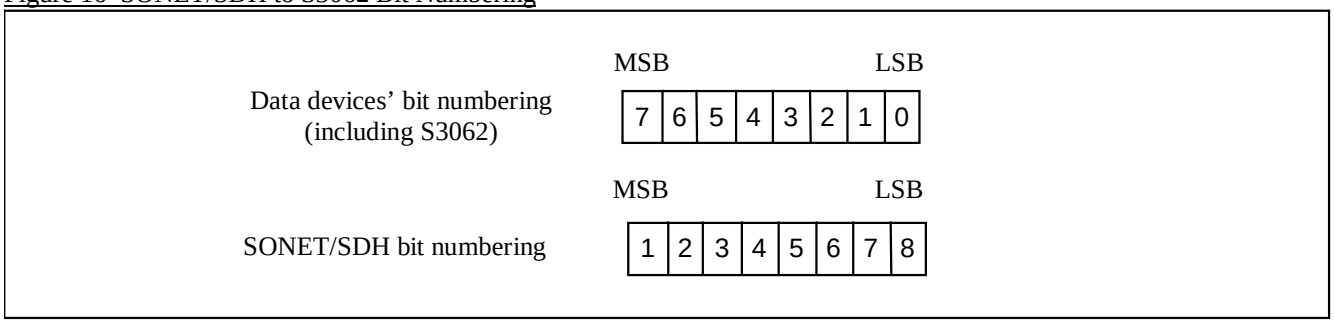


Figure 15 SONET STS-Nc and SDH STM-N Frames Showing the Transport Overhead



Note: SONET/SDH specifications define the most significant bit of a byte to be 1 while the least significant bit is 8. Data processing devices, this one included, define the most significant bit to be 7 while the least significant is 0:

Figure 16 SONET/SDH to S3062 Bit Numbering



3.3.1 SONET/SDH Receive Data

3.3.1.1 Loss of Signal (LOS)

After the receive data has run through the FIFO, the LOS block monitors it for all zeros. When 26.337µs have passed with only zeros being detected, a loss of signal (LOS) is declared (active high) and sent to both an I/O pin and an interrupt bit in a software register. LOS is de-activated following the detection of two valid, consecutive frame alignment patterns without a LOS re-occurring.

A performance monitoring tick is used to transfer to the PM register a single-bit indication of whether or not LOS has occurred since the last tick. This register is provided to simplify the gathering of performance monitoring statistics according to the SONET/SDH standards.

The performance monitoring tick, which typically occurs every second, can come from a clock connected to the PM_CLK I/O pin or, in the case where a clock is not available, from a software write. To enable the tick to come from software, the user must enable the 'PM Tick ON' register bit and activate the Micro Present byte. Then the user must generate the tick by, every second, setting and unsetting the 'PM Tick' bit.

3.3.1.2 Frame and Byte Alignment

The Frame and Byte Alignment block examines the data stream coming from the FIFO for 3 A1s and 3 A2s, which determine both the byte and the frame boundaries. Having found the boundaries, the block then sends a frame pulse to the Frame Counter and arranges the data stream so that it is byte aligned for the following blocks. Then the block stops monitoring the data until the Frame Check block indicates that it is Out-of-Frame (OOF) and a search for a new alignment and frame must be started. Note that while this block is searching, the data continues to pass with the previous alignment. Data is unaffected until this block sets the new boundaries.

3.3.1.3 Frame Check

The Frame Check block determines whether the receiver is in-frame or out-of-frame. In-frame is defined as the state where the frame boundaries are known. Out-of-Frame (OOF) is defined as the state where the frame boundaries of the incoming signal are unknown. OOF is declared when a minimum of four consecutive erred framing patterns have been received. The maximum OOF detection time is 625µs for a random signal. The SONET specification requires that the framing algorithm used to check the alignment is designed such that a $1x10^{-3}$ BER does not cause an OOF more than once every 6 minutes. The S3062 algorithm examines the last A1 byte and the first four bits of the first A2 byte for a total of 12-bits to guarantee this requirement.

When in an OOF condition, this block moves back to the in-frame condition upon detecting two successive error-free framing patterns. This implementation of the frame check circuit clears OOF within the required 250-µs interval. Failure to obtain a frame within 3 ms (OOF persists for 3 ms) results in a Loss-of-Frame (LOF). Both OOF and LOF signals are connected to I/O pins and register bits to keep the user informed of the S3062's state. Similarly to LOS, the performance monitoring tick transfers to the 'PM register' a single-bit indication of whether or not OOF occurred since the last tick.

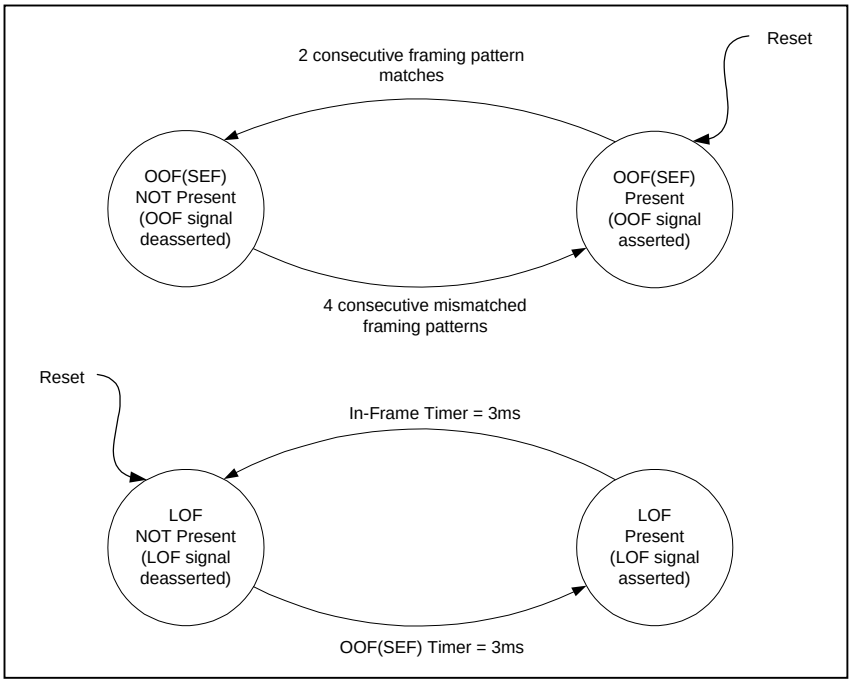
NOTE: OOF is also referred to as Severely Erred Frame (SEF) in the SONET standards.

The LOF error indication is implemented by using a 3 ms integration timer to deal with intermittent OOFs when monitoring for LOF. The 3 ms integration timer consists of an OOF timer and an in-frame timer that operates as follows:

1. The in-frame timer is activated (accumulates) when in-frame is present. It stops accumulating and is reset to zero when OOF is present.
2. The OOF timer is activated (accumulates) when OOF is present. It stops accumulating when the signal goes in-frame. It is reset to zero when the signal remains in-frame continuously for 3 ms (i.e., the in-frame timer reaches 3 ms).

The LOF state will be entered if the accumulated OOF timer reaches the 3 ms threshold. The LOF state will be exited when the in-frame timer reaches 3 ms. The following figure depicts the LOF and OOF (SEF) state machine that is implemented.

Figure 17 LOF and OOF (SEF) State Machine Diagram††



3.3.1.4 Frame Counter and Enables

The frame pulse from the Frame and Byte Alignment block resets the counter within this block to the frame boundary. The counter operates at STS-3/STM-1, STS-12/STM-4, or STS-48/STM-16, depending on RATESEL[1:0] inputs. It counts bytes (9 rows x 90 columns x N STS-1s) to find the location of all overhead bytes and generate the timing signals and enables required by all of the other blocks. As an example, it generates a signal to tell the scrambler block when to scramble the bytes and when not to scramble the bytes. It also generates an enable for the insertion of the B1 byte at the correct time and another for the insertion of the B2 byte, etc.

3.3.1.5 Section Trace

The Section Trace block receives a signal from the Frame Counter block indicating the location of the J0 byte. This block checks the J0 byte for a repeating message which is either 1, 16 or 64 bytes long, as defined by the 'Length' register bits. A programmable register also defines the required number of repetitions (either 3 or 5) that must be seen before the J0 message is considered valid. Messages are compared against a message specified by the expected section trace memory and mismatches are flagged. Inconsistent errors are also flagged when no repeating messages are seen. Similarly to LOS, the performance monitoring tick transfers to the 'PM Register' a single-bit indication of whether or not a mismatch and/or an inconsistent error occurred since the last tick.

To help software sort out the meaning of a message, the block can, if requested, search for a message start and put it in the first location in memory. By default, 16-byte messages are expected to have a 1 in the most significant bit of the first byte of the message and 0s in that bit position for the other 15 bytes. Therefore, if a message is 16 bytes long, the byte to go in the first memory location will contain a value of 1 in the MSB. This is compliant with SDH Section Trace Messaging as stated in G.707. By default, 64-byte

†† The OOF/LOF State Machine has changed with respect to the different revisions of silicon. Please consult Errata 7.2 OOF/LOF in the back of the data sheet for details.

messages are expected to be ASCII strings terminated by a carriage return and a line feed (0x0d and 0x0a). Therefore, if the message is 64 bytes long, the byte to go in the first location in memory will be the one following the line feed. This is compliant with SONET Path Trace Messaging as stated in GR-253-CORE. Software may override the default starts for both message lengths by setting the 16-byte message to SONET format instead of SDH, and vice versa for the 64-byte message.

If the start of the message is unknown, or the defined message start is neither of the two possibilities described above, hardware may store the messages using the Section Trace memory as a circular buffer. The circular buffer may be enabled by setting the 'Circular Buffer' bit in the 'Section Trace Control: Receive and Transmit' register. The message length may also be set to 1, 16 or 64 bytes by setting the 'Length' bits.

3.3.1.6 Section Trace Algorithm

The algorithm used to detect problems in the trace message must be robust to bit errors. This block's algorithm defines valid messages, mismatches and inconsistent errors as follows:

Table 7 Section Trace Definitions

EXPECTED MESSAGE	The value stored in the 'Expected Section Trace Message' register. This is user programmable.
MATCHED MESSAGE	A MATCHED MESSAGE is an incoming message that is identical to the EXPECTED MESSAGE.
MISMATCH MESSAGE	A MISMATCHED MESSAGE is an incoming message that differs from the EXPECTED MESSAGE.
VALID MISMATCH MESSAGE	A VALID MISMATCHED MESSAGE is an incoming MISMATCHED MESSAGE that differs from the expected message but has been received 3 (default) or 5 consecutive times. The number of received, consecutive values is programmable with the 'Check 5' register bit. The times required to receive a VALID MISMATCHED MESSAGE of length 1, 16, 64 in a system with a BER of 0 or $1x10^{-3}$ are shown in Table 10 .
VALID MATCHED MESSAGE	A VALID MATCHED MESSAGE is an incoming MATCHED MESSAGE that has been received 3 (default) or 5 times, without a VALID MISMATCHED MESSAGE received in between. The number of received, consecutive values is programmable with the 'Check 5' register bit. The times required to receive a VALID MATCHED MESSAGE of length 1, 16, or 64 in a system with a BER of 0 or $1x10^{-3}$ are shown in Table 8 . Permitting validation of expected messages to occur without requiring the messages to arrive consecutively shortens the validation time when the bit error rate is high. See Table 8 and Table 10 .
INCONSISTENT ERROR	An inconsistent error is declared if neither a VALID MISMATCHED MESSAGE nor a single MATCHED MESSAGE have been seen in 4 times the time which would normally be required to detect 3 or 5 MATCHED MESSAGES in the presence of a BER of $1x10^{-3}$. Reception of a VALID (MATCHED OR MISMATCHED) MESSAGE clears the inconsistent error. Table 9 shows the length of time hardware spends in searching for a valid mismatch or a single expected message before declaring an inconsistent error. Note that the values of Table 9 are 4 times the worst-case values in Table 8 .

Table 8 Time Required to Receive a VALID MATCHED MESSAGE

BER	1-byte Message	16-byte Message	64-byte Message
BER = 0, detect = 3	375µs	6ms	24ms
BER = 0, detect = 5	625µs	10ms	40ms
BER = $1x10^{-3}$, detect = 3	750µs	22ms	192ms
BER = $1x10^{-3}$, detect = 5	1ms	28ms	224ms

Probability > 99.9999%

Table 9 Time Required to Detect an INCONSISTENT ERROR

BER	1-byte Message	16-byte Message	64-byte Message
BER = $1x10^{-3}$, detect = 3	3ms	88ms	768ms
BER = $1x10^{-3}$, detect = 5	4ms	112ms	896ms

It is unlikely that a false INCONSISTENT ERROR will be raised if the expected message is being sent. Note, however, that when the bit error rate is high, and an incorrect message is being sent, it is more likely that an INCONSISTENT ERROR will be raised than a MISMATCH, especially in the case of a 64-byte message. The reason being is that the probability of receiving three consecutive sets of 64-bytes with no errors is small when in the presence of a BER of $1x10^{-3}$. To increase the probability of receiving a VALID MISMATCHED MESSAGE, one must increase the amount of time one is willing to wait. For a probability > 99.9999%, one must wait the times shown in Table 10 below. Compare Table 10 to Table 9 to verify that the probability of receiving an INCONSISTENT ERROR is greater than a MISMATCH in the presence of a high bit error rate. Software must keep this in mind when determining the cause of a section trace interrupt.

Table 10 Time Required to Detect a VALID MISMATCHED MESSAGE

BER	1-byte Message	16-byte Message	64-byte Message
BER = 0, detect = 3	375µs	6ms	24ms
BER = 0, detect = 5	625µs	10ms	40ms
BER = 10^{-3}, detect = 3	2.2ms	120ms	2.4s
BER = 10^{-3}, detect = 5	2.6ms	280ms	24s

Note that the times during the BER of $1x10^{-3}$ are approximate. There is a small probability ($1x10^{-10}$) that the messages still will not be received, in the times shown.

Examples

1. BER = 0, expected 16-byte message = 'A', the expected message is being received, no section trace errors are showing and the message detect time has been set to 3. The S3062 sees:

   ... AAAAAAAAAAAAAAA ...

2. The network connections upstream of this node are changed and this device starts seeing 16-byte message 'B':

   ... AAAABBB

   After the third B, it declares a mismatch and interrupts software which then reads 'B' in the receive section trace memory. (The time taken to discover the mismatch after the connection was switched is, in this example, 6ms: 3 messages * 16bytes/message * 1 frame/msgbyte * 125µs/frame.)

3. Software informs the network of the problem and the connections are fixed, but now there is a BER of $1x10^{-3}$ on the line. The S3062 sees large numbers of random garbage messages ('g') because of all the bit errors:

   ... BBBBggAggggAgA

   After the third expected message, the S3062 clears the mismatch and interrupts the software to tell it of the change. The software can then read 'A' in the receive section trace memory. (The time taken to clear the mismatch after the connection fix is, in this example, 10 messages * 16bytes/message * 1 frame/msgbyte * 125µs/frame = 20ms.)

4. Now the connections get disturbed again and message 'B' is once more being sent, but the line still has a BER of $1x10^{-3}$ on it.

   ... ggAgBggBgBBgBgBggBgggBgggBBggBBgBgggBBggBgBBggB

   The S3062 needs to see 3 'B's in a row to be able to say with certainty that it is getting a valid, mismatched message, not just a bunch of noise. In this example, it does not get 3 'B's in a row before hitting the inconsistent error's timeout value of 88ms. Therefore, an inconsistent error is declared. Note that there is no reason for software to read the receive section trace message memory -- with the bytes changing inconsistently, there is no message to store so that whatever the last valid message was (in this example, 'A') will still be there.

A software 'As-is' option allows the received J0 message to be written into the receive section trace memory without validation. If the circular buffer is not enabled the message start search may be used. When a new message start is seen, the old message will be written into the received memory and a new message collection started. If no message start is seen, then the message will be written to memory when the correct length (1, 16 or 64) has been received. This will permit messages, which are less than 16 or less than 64 bytes long, to be lined up correctly in the receive memory.

If the circular buffer is enabled in 'As-is' mode, the messages will be transferred to the receive memory after the specified bytes (1, 16 or 64) have been received. In this case, if software selects a 64-byte message, it will only have to read the memory once every 8ms (64*125µs) to see new values. To create an 8ms timer synchronized to the S3062, connect FPOUTB to an interrupt and count 64 frames. NOTE: Wait for 500ns after FPOUTB before reading the receive memory to be sure that hardware is not updating it.

3.3.1.7 Descrambler

All the bytes in the SONET/SDH data stream, with the exception of A1, A2 and J0/Z0, are normally scrambled and must be descrambled before further overhead processing can be completed. The descrambler and scrambler algorithms are identical, using a generator polynomial of $1 + x^6 + x^7$ with a sequence length of 127. The algorithm is frame synchronous, being reset to "1111111" on the most significant bit of the first byte following the last byte of the first row (last Z0 byte) of the STS-N/STM-M section overhead. This bit and all subsequent bits to be scrambled are added modulo 2 to the output from the X^7 position of the scrambler.

To disable descrambling without a processor connected to the S3062, de-assert the DESCRBEN I/O pin. With a processor connected, write a '1' to the 'Descr OFF' register bit and enable software register control by writing a 59h to the Micro Present byte. The controls set by the processor override the signals on the I/O pins when the Micro Present byte contains a value of 59h.

3.3.1.8 Section BIP-8 (B1)

The Section BIP-8 block receives data from both the scrambled and descrambled data streams. Bit interleaved parity (BIP)[‡‡] is calculated on the scrambled data. The result is then compared with the descrambled B1 byte. Mismatched bits are defined as errors and are shown at the B1ERR output pin and counted internally. If the user has selected block error counting, 1 error is counted and shown at the B1ERR output pin and for each erred B1 byte. If block error counting is not selected, 1 error is counted and shown at the B1ERR output pin for each bit that is mismatched (up to 8 errors possible per byte). To select block error counting without a processor connected to the chip, assert the BLOCKBIP I/O pin. With a processor connected, write a '1' to the 'Block B1s' register bit and enable software register control by writing a 59h to the Micro Present byte.

A performance monitoring tick is used to transfer the accumulating error count into a static holding register that can be read from the processor and FPGA interfaces. The accumulation counter is then reset to zero. The tick, which typically occurs every second, can come from a clock connected to the PM_CLK I/O pin or, in the case where a clock is not available, from a software write to the 'PM Tick' bit. To enable the tick to come from software, the user must enable the 'PM Tick ON' register bit and activate the Micro Present byte. Then the user must generate the tick by, every second, writing to the 'PM Tick' bit. Note that if the tick is late, the counter will stop at FF00h which is the maximum number of B1 errors that may be received on a STS-48/STM-16 link in 1.020 seconds.

The tick also transfers, to the 'PM Register', a single-bit indication of whether or not a B1 error has occurred within the last second. Thus software can read or not read the count registers based on whether or not the bit is set. Since all of the SONET/SDH counts have an indicator bit in the 'PM Register', one read of the 'PM Register' would let software know the necessity of further reads.

3.3.1.9 Line AIS Multiplexer #1[§§]

After the B1 byte has been checked, the data passes on to the line AIS Multiplexer #1. If the user has not requested that line AIS be automatically inserted then the data will go straight through the Line AIS Multiplexer #1. If LOS or LOF has been detected and automatic AIS insertion has been selected, the section overhead bytes[***] A1, A2 and B1 will be recalculated and the entire line overhead and payload will be replaced with 1s. The SONET/SDH specifications require the insertion of AIS upon the receipt of LOS or LOF to prevent downstream blocks from monitoring bad data. To select automatic line AIS insertion without a processor connected to the chip, assert the AUTOAIS I/O pin. With a processor connected, write a '1' to the 'AUTOAIS' bit and enable software register control by writing a 59h to the Micro Present byte. The controls set by the processor override signals on the I/O control pins when the Micro Present byte contains a value of 59h. When AUTOAIS is selected, a line AIS will be generated upon receipt of a LOS or LOF until the LOS or LOF ends.

A user-requested AIS has no effect on this multiplexer; it only affects the downstream Line AIS Multiplexer #2. This is so that the user may request a downstream line AIS and still monitor the line overhead.

3.3.1.10 Line BIP-8 (B2)

Given that the Line AIS Multiplexer #1 has not turned all the line overhead bytes into FFh, the Line BIP-8 block can check the B2 bytes. The B2 byte is allocated in each STS-1 frame for a line error monitoring function. In an STS-N there are therefore N B2s, each one the result of a BIP-8 calculation over a single STS-1 excluding its section overhead. To check that the incoming B2s have

[‡‡] Bit interleaved parity-8 (BIP-8) is a method of error monitoring. SDH standard G-707 specifies it as follows: "Even parity is generated by setting the BIP-8 bits so that there is an even number of 1s in each monitored partition of the signal. A monitored partition comprises all bits that are in the same bit position within the 8-bit sequences in the covered portion of the signal. The covered portion includes the BIP-8".

[§§] The AUTOAIS feature within specific silicon revisions require the FIXSOH feature to be enabled to deliver a valid frame to downstream devices. Please consult Errata 7.4 AUTOAIS in the back of the data sheet for details.

[***] To avoid runlength problems with the reception of a LOS, specific revisions of the silicon scramble the unscrambled J0 and Z0 bytes when a LOS is detected and AUTOAIS is enabled. Please consult Errata 7.4 AUTOAIS in the back of the data sheet for details.

been generated correctly, the BIP-8 values are recalculated over the line overhead and the SPE bytes for each STS-1 in each frame after descrambling. The results are then compared to the incoming B2s after descrambling.

If the user has selected block error counting, 1 error is counted for each erred B2 byte. If block error counting is NOT selected, 1 error is counted for each bit that is incorrect (up to 8 errors possible per B2 byte). To select block error counting without the processor interface being activated, assert the BLOCKBIP I/O pin. With a processor connected to the S3062, write a '1' to the 'Block B2s' register bit and enable software register control by loading the Micro Present byte with a value of 59h. The controls set by the processor override signals on the I/O control pins when the Micro Present byte contains a value of 59h.

A performance monitoring tick is used to transfer the accumulating error count into a static holding register that can be read from the processor and FPGA interfaces. The counter is then reset to zero. The tick, which typically occurs every second, can come from a clock connected to the PM_CLK I/O pin or, in the case where a clock is not available, from a software write to the 'PM Tick' bit. To enable the tick to come from software, the user must enable the 'PM Tick ON' register bit and activate the Micro Present byte. Then the user must generate the tick by, every second, writing to the 'PM Tick' bit. Note that if the 'PM Tick' is late, the counter stops at 300000h, which is the maximum number of B2 errors that may be received on a STS-48/STM-16 link in 1.024 seconds.

The tick also transfers, to the 'PM Register', a single-bit indication of whether or not a B2 has error occurred within the last second. Thus software can read or not read the count registers based on whether or not the bit is set. Since all of the SONET/SDH counts have an indicator bit in the 'PM Register', one read of the 'PM Register' would let software know the necessity of further reads.

3.3.1.11 Bit Error Rate (BER)

The Bit Error Rate block accumulates all B2 bit errors and asserts Signal Fail (SF) or Signal Degrade (SD) to the processor and FPGA interfaces if the number of errors cross pre-set thresholds after pre-set times. If the B2 BLOCKBIP feature is enabled, the SD and SF values will be relative to the block values, not bit values. The tables below contain sample Threshold and Accumulation Period values that may be set in the register map.

Table 11 Sample Values for SF

BER Rate	**STS-3 / STM-1**		**STS-12 / STM-4**		**STS-48 / STM-16**	
	Threshold Number HEX/DECIMAL	Accumulation Period (ms) HEX / DECIMAL	Threshold Number HEX/DECIMAL	Accumulation Period (ms) HEX / DECIMAL	Threshold Number HEX/DECIMAL	Accumulation Period (ms) HEX / DECIMAL
$1x10^{-3}$	266h / 614d	8h / 8d	99Ah / 2458d	8h / 8d	2666h / 9830d	8h / 8d
$1x10^{-4}$	B8h/184d	Dh / 13d	1C6h / 454d	8h / 8d	71Bh / 1819d	8h / 8d
$1x10^{-5}$	99h/153d	64h / 100d	99h / 153d	19h / 25d	C3h / 195d	8h / 8d
$1x10^{-6}$	99h/153d	3E8h / 1000d	99h / 153d	Fah / 250d	99h / 153d	3Eh / 62d

Table 12 Sample Values for SD

BER Rate	**STS-3 / STM-1**		**STS-12 / STM-4**		**STS-48 / STM-16**	
	Threshold Number HEX/DECIMAL	Accumulation Period (ms) HEX / DECIMAL	Threshold Number HEX/DECIMAL	Accumulation Period (ms) HEX / DECIMAL	Threshold Number HEX/DECIMAL	Accumulation Period (ms) HEX / DECIMAL
$1x10^{-5}$	10h / 16d	Ah / 10d	3Eh / 62d	Ah / 10	F9h / 249d	Ah / 10
$1x10^{-6}$	10h / 16d	64h / 100d	3Eh / 62d	64h / 100	F9h / 249d	64h / 100
$1x10^{-7}$	10h / 16d	3E8h / $1x10^{3}$d	3Eh / 62d	3E8h / $1x10^{3}$d	F9h / 249d	3E8h / $1x10^{3}$d
$1x10^{-8}$	10h / 16d	2710h / $1x10^{4}$d	3Eh / 62d	2710h / $1x10^{4}$d	F9h / 249d	2710h / $1x10^{4}$d
$1x10^{-9}$	10h / 16d	186A0h / $1x10^{5}$d	3Eh / 62d	186A0h / $1x10^{5}$d	F9h / 249d	186A0h / $1x10^{5}$d
$1x10^{-10}$	10h / 16d	F4240h / $1x10^{6}$d	3Eh / 62d	F4240h / $1x10^{6}$d	F9h / 249d	F4240h / $1x10^{6}$d

The threshold and time values default to $1x10^{-3}$ for signal fail and $1x10^{-5}$ for signal degrade so that this circuit can still be useful if a processor is not connected. Note that the settings assume a uniform distribution of errors. If this is not the case, the values may have to be changed or software may be required to interpret the findings.

Software must implement SONET/SDH fault clearing, after receiving an indication of SF or SD by:

1. Setting the Threshold and Accumulation Period registers to one tenth of the existing BER value.
2. Polling the SD and SF interrupts to see if an interrupt occurs.
3. If an interrupt still occurs, software will need to repeat the process.
4. If an interrupt does not occur, software may declare that the fault condition has cleared.

After the fault has cleared, software can then set the SF or SD Threshold and Accumulation Period registers back to their normal values. Consult the S3062 Software Appliations Note for details.

3.3.1.12 Automatic Protection Switching (APS)

This block monitors the least significant 3 bits of the K2 line overhead byte for the Line Alarm Indication Signal (AIS_L: 111) and the Line Remote Defect Indication (RDI_L: 110). If a specified number of consecutive AIS_L values are seen, AIS_L is asserted in a status register, which is accessible by the processor and FPGA. The AIS_L indication is removed when the same number of consecutive non-AIS_L values are seen. RDI_L is handled the same way. The number of consecutive values can be either 3 (for the SDH standard) or 5 (for the SONET standard). This number of consecutive values is configurable via a processor interface control register (default value is 5). Changes of state in AIS_L and RDI_L (to/from AIS_L/RDI_L present/not present to not present/present) indications generate interrupts. Similarly, the performance monitoring tick transfers to the 'PM Register' a single-bit indication of whether or not AIS_L and/or RDI_L occurred since the last tick.

The block also monitors K1 and K2 for new values. If a new value of K1 or K2 is seen for 3 consecutive frames, it is latched for software to read and an interrupt is raised. If no consistent K1 value is seen for 12 frames, an "inconsistent K1" alarm is flagged to software.

K1 and K2 are used for protection switching. If the S3062 device is installed in an unprotected system, the user may simply ignore these indications, or at the most keep track of AIS-L and RDI-L for performance monitoring statistics.

3.3.1.13 Synchronization

The synchronization block monitors the S1 line overhead byte for 8 consecutive identical values in the least significant 4 bits. If the nibble differs from the previously acquired S1, the new value replaces the old in a register accessible through the processor and FPGA interfaces. If the new nibble is different from an expected value written in by software, a mismatch is flagged. If the new nibble is the same as the expected value the mismatch is cleared. If 32 frames go by without 8 consecutive identical values, an inconsistent value indication is flagged. To decide that the synchronization source has truly failed, as defined by the standards, software must start a 10s counter as soon as it receives the inconsistent value indication. If no valid message is detected before the counter runs out, the software must consider that the synchronization reference failed.

The standards specify a 10-second invalid S1 value, not the 32-frame inconsistent value indicator. The 32-frame inconsistent value indicator was designed to assist software and to create a function similar to the K1/K2 standard. The S1 byte is considered valid after 8 consecutive frames and inconsistent after 4 times this interval, or 32 frames.

The S1 value and its error indications are only of use if there are 2 synchronization sources to choose from. If the S3062 device is being used in a repeater, there will only be one clock source available, and no action will be taken if the synchronization reference fails. The user will simply ignore all the S1 information.

3.3.1.14 Remote Error Indication (REI)

The STS-N/STM-M M1 byte contains the addition of all the B2 errors that were detected at the far-end. This count is called the Remote Error Indication (REI). The way REI works is as follows: System X is connected to System Y. Data flows from X to Y and also from Y to X. There is a problem with X's transmitter causing intermittent bit errors. Y sees these errors when it checks B2. It counts them up and sends the count back to X in the M1 byte. X looks at the M1 byte, sees the errors and checks its transmitter. It finds the fault and repairs it.

Since REI tells the user what the far-end is seeing, it is only useful if the S3062 chip resides in a system where traffic is bi-directional. In a uni-directional system, the user may ignore this value or keep the data for performance monitoring statistics.

For statistics, the block adds up the REI values until the performance monitoring tick is received. Just like the B1 and B2 counts, the tick transfers the count to a register accessible by the processor or the FPGA and clears the counter. If no tick is received, the counter stops counting when it reaches a maximum value of 1FE000h errors which is the maximum number of errors that could be received on a STS-48/STM-16 link in a 1.024 seconds. The tick also transfers, to the 'PM Register', a single-bit indication of whether or not a REI error occurred within the last second.

The capability of transmitting a user defined value for the M1 byte using overhead insertion via the TX_OH memory is supported if the user wishes to supply the B2 error count arriving in the other direction.

3.3.1.15 Serializer

This block serializes onto pins the section and line orderwire (E1 and E2) and the section and line data communication channels (D1-3 and D4-12). The block also generates a gapped 9.72MHz clocks for the output serial streams. (The 9.72MHz frequency increases by the FEC encode bandwidth expansion factor if FEC encode is ON.) The orderwire also requires a frame pulse from this block to mark the most significant bit of the byte. Since the DCCs are bit, not byte oriented, no frame pulses or byte markers are required.

The orderwire must go to an external circuit designed especially for it, but the DCCs may be connected directly to serial HDLC processors such as the MPC860. If the protocol on the DCCs is not standard HDLC, the MPC860 SCC ports may still be used; program them in transparent mode. If the protocol is byte-oriented, the orderwire frame pulses may be used to indicate the first DCC's most significant bit. In this case, however, an external circuit will likely be needed because the orderwire frame pulse is not lined up directly with the DCCs' most significant bits. See Figure 36 .

Twenty user accessible pins are used by this block and the parallelizer (2 orderwire clocks, 2 orderwire frame pulses, 2 section DCC clocks, 2 line DCC clocks, 4 data out, 4 data in and 4 enable data in). They are also shared by the FPGA port. A FPGA may be connected to extract and insert all the overhead bytes, or, individual devices may be connected to the serial orderwire and DCC ports. An active signal on the FPGASEL pin selects the FPGA port.

If the FPGA port is not selected, all the DCC signals generated by this block will continue to run, even when the chip is in LOS or LOF. If the data is extracted during a LOS or LOF condition, the data will be garbage. Upon re-acquisition of byte alignment following a LOS or LOF, the location of the frame relative to the previous alignment may have changed. This may lead to extra/fewer bits and serializer clocks in a frame, but the clock period will not be affected.

3.3.1.16 Receive Overhead Memory (RX_OH)

All received section and line overhead bytes are captured frame-by-frame in the Receive Overhead Memory (RX_OH). The memory is divided into 2 pages, X and Y. During the first frame, the overhead bytes are written into page X while the processor and/or the FPGA interface read out of page Y. At the beginning of the next frame, the two pages are swapped and bytes are written into page Y while page X can be read by the processor and/or FPGA. At the beginning of the next frame the pages are swapped again.

The two pages are transparent to the user. If the overhead data is going out the FPGA interface, it looks like a steady stream of overhead data. If software is reading the transport overhead from memory via the processor interface, it always uses the same address to access a particular overhead byte; the address does not change with the page swap. If timing delays are important, however, the user must be aware of the 2 pages because they do cause a full frame delay between the time the overhead arrives on the chip and the time that it can be read out of the RX_OH memory.

3.3.1.17 Overhead Extract State Machine and Receive FPGA Interface

The Overhead Extract State Machine block controls all of the accesses to the Receive Overhead Memory (RX_OH). Write addresses are generated as required to one of the RX_OH pages (page X, for example) while the entire frame of section, and line overhead bytes are written in from the receive data stream. If the FPGA interface is selected (FPGASEL), then at the same time as page X is being written, the state machine generates read addresses for page Y. 32 bits are read at a time, then held and output to the 8-bit, FPGA interface. All 1296 overhead bytes (N x 27) for an STS-48/STM-16 signal are sent out, in order from the first A1 to the last byte in the E2/undefined column. Following the last byte, the values in the SONET/SDH fault and performance monitor registers (registers 010h to 019h) are sent out, in the order they are shown in the register map, most significant byte first. The rate of the FPGA interface is 19.44MHz for STS-12/STM-4 and STS-48/STM-16 and 1.62MHz for STS-3/STM-1. The frequency increases by the FEC encode bandwidth expansion if FEC encode is ON.

When the FPGA port is selected, the FPGA signals generated by this block will run continuously, even when the chip is in LOS or LOF. However, the data extracted during a LOS or LOF condition will be garbage. Upon re-acquisition of byte alignment following a LOS or LOF, the location of the frame relative to the previous alignment may have changed. This may lead to extra/fewer bits and FPGA clocks in a frame, but the clock period will not be affected.

The Overhead Extract State Machine arbitrates access to the RX_OH memories between the FPGA port and the MPC860, giving the FPGA priority. If both the microprocessor and the FPGA port request a read, the processor's read will be delayed until the FPGA read is complete. If no FPGA is present (indicated by the FPGASEL signal being inactive), then the processor interface has exclusive read access of the RX_OH memories.

3.3.2 SONET/SDH Transmit Data

After all of the receive data and overhead has been monitored and read, the transmit blocks may modify or overwrite the data.

3.3.2.1 Framing and Section BIP-8

The user may request that errors in the framing bytes, A1 and A2, be corrected to improve the chances that downstream devices will be able to frame to the signal. Touching the framing bytes will affect the section BIP-8 so that if they are corrected, the B1 byte will be recalculated. To select Fix Section Overhead without a processor connected to the chip, assert the FIXSOH I/O pin. With a processor connected, write a '0' to the 'Don't Fix SOH' register bit and enable software register control by writing a 59h to the Micro Present byte. The controls set by the processor override signals on the I/O control pins when the Micro Present byte contains a value of 59h. NOTE: If the FIXSOH feature will be used to correct unframed data when coming out of reset, it is recommended that FIXSOH only be enabled after the reset has been completed.

Changes in any of the other overhead bytes or in the data will force this block to recalculate the B1 for all subsequent frames regardless of the state of FIXSOH. Section BIP-8 is calculated over the entire scrambled STS-N/STM-M frame, after the overhead has been modified, and inserted into the B1 byte location of the next frame before going through the scrambling process.

3.3.2.2 Section Trace

If the 'Send J0 Msg' register bit is enabled, the Section Trace block will repeatedly send out, one byte per frame, the data which was written into the 'Transmit Section Trace Memory'. Software must be sure that the data is in the correct message format (SDH or SONET), since this block simply writes out what was written in. The message length (1,16 or 64 bytes) is set in the section trace register and is the same for both transmit and receive messages.

3.3.2.3 Line BIP-8

Individual B2 BIP-8s are calculated over all of the bytes, with the exception of the section overhead, for each STS-1 in the previous STS-N/STM-M frame before scrambling and after any overhead byte insertions or modifications. They are supplied to the Overhead Multiplexer in the appropriate B2 locations of the current frame before scrambling. The multiplexer checks the various enable signals to decide whether to accept the B2s for insertion or keep the received B2s. Note that changes in any of the line overhead bytes or the data will cause the multiplexer to choose the regenerated B2 for all subsequent frames regardless of the state of enable signals.

3.3.2.4 Overhead Multiplexer

This block overwrites the received A1, A2 and B1 with the fixed framing bytes and recalculated B1 if the FIXSOH, Fix Section Overhead, feature has been requested. It also accepts the recalculated B1 if any changes to overhead or data are being or have been made by any of the other transmit blocks. If the Micro Present byte is active and transmit section trace enabled, the multiplexer will overwrite the received J0 byte with the byte from the 'Transmit Section Trace Memory'. B2 bytes are taken from the Line BIP-8 block rather than the receive stream if (a) B2 re-calculation has been enabled, or, regardless of the enable, if (b) any of the line overhead or data bytes are being or have been changed by up stream blocks within the S3062. The enable for B2 re-calculation comes from the FIXB2 I/O signal if the processor's Micro Present byte is inactive, or from a register control bit.

3.3.2.5 Parallelizer

The parallelizer block brings serial orderwire (E1 and E2) and data communication channels (DCCs) into the chip and organizes them into byte format to be inserted into the transmit data stream. It generates frame pulses for the orderwire and gapped 9.72MHz clocks for all the input serial streams. The 9.72MHz frequency increases by the FEC encode bandwidth expansion if the FEC encoder is activated. It uses the enables provided for each stream to determine whether or not to overwrite the orderwire and DCC with the received data. If the processor is activated, the enable I/Os are ORed with the software enables so that either hardware or

software can control the data insertion. Note that if the orderwire or DCC bytes in the TX_OH memory are enabled for insertion into the transmit data stream, they will have precedence over data from the parallelizer.

Since the FPGA and parallelizer share pins, the parallelizer is only enabled if the FPGASEL pin is inactive. Like the serializer, as long as the FPGA is not selected, the parallelizer will run, even during LOS and LOF.

3.3.2.6 Overhead Insert State Machine and Transmit FPGA Interface

If the FPGASEL pin is selecting the FPGA, the Overhead Insert State Machine block generates a frame pulse to the FPGA and a 19.44MHz* clock for STS-12/STM-4 or STS-48/STM-16 and a 1.62MHz* clock for STS-3/STM-1 rate data. This block receives 8-bit wide overhead data bytes and overhead enables from the FPGA. If permitted, the block then writes the data into the Transmit Overhead Memory (TX_OH) and writes the enables into the 'Overhead Insert Control Memory' (OIC).

To get permission to write the FPGA data and enables into memory, the block checks the Micro Present byte. If the byte is not active, the FPGA data is written into the TX_OH and the FPGA enables are written into the OIC. If the Micro Present byte is active, the FPGA enables are completely ignored and the block checks the 'Transmit Access Control Memory' to see whether or not the FPGA data should be written into the TX_OH.

The Overhead Insert State Machine block must also take care of arbitrating the timing of accesses to the TX_OH. FPGA accesses have priority over processor accesses, which are held off until the FPGA is done. This can add a wait state to the processor access. Also, the TX_OH is divided into two pages, just like the RX_OH. This block ensures that the write and read address are directed to the correct pages.

Similarly to the Overhead Extract State Machine and Receive FPGA Interface, this block runs and produces signals for the FPGA interface even during LOS and LOF (given that the FPGASEL signal is active).

3.3.2.7 Transmit Overhead Memory (TX_OH)

The Transmit Overhead Memory is composed of two pages just like the RX_OH. While one page is being written, either from the FPGA or the microprocessor, the other page is being read and the data sent to the Overhead Insert Multiplexer. The pages are swapped at the beginning of every frame. The user must be aware of this if the delay between writing an overhead byte and having it inserted into the data stream is important. With the two-page scheme, there is a guaranteed frame delay.

Software must also take the 2 pages into account if it wants to write an overhead byte and have it transmitted in multiple frames. For example, suppose software is running a protection exercise and wishes to change the value in the K1 byte to "exercise" (4 in the most significant nibble). It wishes to keep this value for the duration of the test, which takes several frames. It must write 4 into K1 in one page, then wait for the frame pulse to indicate that the frames have swapped, and write 4 into the second. Once that is done, it writes a '1' to the OIC to enable the value to go out. For every frame thereafter, K1 will be replaced with 4.

Suppose the test is done and software changes the value to 0, but it only writes the 0 in one of the 2 pages. Then the K1 being sent out will be 0 in the first frame, 4 in the second, 0 in the third, 4 in the fourth, etc. as the pages swap with each other. This will certainly cause problems for downstream devices. If software cannot guarantee that it will be able to write both pages within a few frames of each other, it should probably disable the byte insertion (write '0' to the OIC enable bit) before making any TX_OH change and only re-enable the insertion after both pages match.

3.3.2.8 Transmit Access Control Memory (TAC)

The contents of the 'Transmit Access Control Memory' determines whether a given overhead byte location in the TX_OH memory is written via the FPGA port, or from the processor interface. This memory contains 1296 (STS-48 x 27) single bit enables,

* The frequency increases by the FEC Encode bandwidth expansion if FEC Encode is ON.

organized as 81 words x 16 bits. Each bit controls processor/FPGA access to one overhead byte location in the TX_OH memory. A logic "1" in a given bit indicates that the corresponding overhead byte location in the TX_OH memory can only be written to by the processor. Any data bound for this location from the FPGA will be ignored. A logic "0" in a given bit indicates that only the FPGA data can be written into the corresponding TX_OH memory byte. Accesses from the processor will be prevented. (The processor transfer will be acknowledged, but no data will be written.)

The contents of this memory will only function in the manner described above if a processor is actually present, as indicated by the Micro Present byte being active. If this byte is not active, then the contents of the 'Transmit Access Control Memory' will be ignored, and the TX_OH memory will be written exclusively from the FPGA port. The 'Transmit Access Control Memory' itself is exclusively accessible from the processor interface.

3.3.2.9 Overhead Insert Control Memory (OIC)

The 'Overhead Insert Control Memory' contains 1296 (STS-48 x 27) single bit enables, organized as 81 words x 16 bits. Each bit controls whether or not an overhead byte which is stored in the TX_OH memory will be inserted into the transmit data stream, overwriting the received byte. The OIC memory has two ports, one read-only port on which the insert enables are read out and sent to control the Overhead Insert Multiplexer, and one read/write port which is written, either via the FPGA port, or from the processor interface. If the Micro Present byte is active, then only the processor will be allowed 16-bit read/write access to this memory, even if an FPGA is also present. If the Micro Present byte is NOT active, then the FPGA will write this memory. Each overhead byte received from the FPGA is accompanied by a TX_OH_INS signal, which is the enable for that byte. These single-bit enables are accumulated into 16-bit words and written into the 'Overhead Insertion Control Memory'. The Overhead Insert State Machine controls the sequencing of these operations.

3.3.2.10 Overhead Insert Multiplexer

This block uses the enables generated from the OIC to determine whether the received data must be passed through or replaced by data from the TX_OH. If the OIC does not enable TX_OH data, and the FPGASEL signal is inactive, the block checks the enables from the Parallelizer block to determine if data from there should replace the received data. In any case, if any data is being inserted, this block signals the Section BIP-8 block to re-generate the B1. If any data other than the section overhead is being inserted, the block signals the Line BIP-8 block to re-generate B2.

This block also handles the special insertion of B1 and B2. If these bytes are enabled to come from the TX_OH, the user can request that the TX_OH value be inserted directly into the data stream or be XORed with the actual B1 or B2 value. If the Micro Present byte is not active, the XORBIP pin controls this choice; otherwise, a register bit controls it. If the B1 and B2 are not enabled to come from the TX_OH, this multiplexer will not touch them. They will have been passed through or inserted correctly by the Overhead Multiplexer and will pass through this multiplexer with the data.

There are global controls to disable insertion of overhead from the TX_OH memory regardless of the contents of the OIC. If the Micro Present byte is not activated, this control comes from the MEMOH I/O signal; otherwise it comes from the 'Insert OH' register bit. Because the OIC is not reset to a default state, one of these signals must be activated if neither processor nor FPGA are present, or if the OIC has not been written.

If the S3062 is used with a processor, the MEMOH I/O pin should be tied to ground. Then when the part is reset, no overhead will be inserted until (1) software has started up, (2) filled the OIC correctly, (3) enabled the 'Insert OH' register bit, (4) written the Micro Present byte with a value of 59h. All should occur in this order. If the S3062 is being used with an FPGA and no processor, the user must be aware that overhead data will be inserted randomly until the FPGA has started up and written a frame's worth of data. The assumption here is that the FPGA will NOT control the MEMOH pin which will be tied high (active). Thus, when the S3062 is initialized, the OIC (with its random start-up values) will control the overhead insertion. It will be a full frame before the FPGA writes correct values into the OIC (through the TX_OH_INS I/O pin). This will not be a problem if the FPGA starts up within a few frames because, in any case, a couple of frames are required for the S3062 to find correct framing and byte alignment and start

passing data through correctly. However, if the user wishes to be absolutely sure of a clean start, the FPGA can, on reset, drive the MEMOH pin low until it has sent a frame of data in. Then it can drive the pin high to activate overhead insertion.

3.3.2.11 Line AIS Multiplexer #2

After getting through the Overhead Insert Multiplexer, the data passes on to the line AIS Multiplexer #2. The first line AIS multiplexer blocked bad data from getting through to the line overhead blocks in the presence of LOS or LOF as required by standards. This multiplexer repeats the process on any newly generated overhead and allows the user to force an AIS. Thus, if LOS or LOF has been detected, or line AIS is being forced, all but the section overhead bytes will be replaced with 1s. The user has two ways to request automatic AIS insertion: either through the AUTOAIS I/O pin or, if the Micro Present byte has been written, through the 'AUTOAIS' register bit. Similarly, the user can request the line AIS forced through the DATAAIS signal pin or the 'Force AIS' register bit.

Software must be aware that line AIS is not automatically forced if it is received through an indication of 111 in the 3 least significant bits of K2. If neither the FPGA nor processor are inserting data into the K2 byte, then it will pass through the S3062 and the line AIS indication, contained in the least significant bits of K2, will pass through also. If, however, the K2 byte is being over-written with data that does not indicate that an AIS has occurred, downstream nodes will not recognize that a line AIS was received upstream. In this case, software has three options when it receives a line AIS interrupt. It can:

(a) turn OFF the K2 insertion in the OIC and thus let the received K2 pass
(b) write 111 to the 3 least significant bits of K2, thus emulating the line AIS indication and not affecting the other bits of the byte
(c) turn ON the 'Force AIS' register bit.

Software must also be aware that in the SDH standard (not the SONET standard), line AIS may be transmitted if a BER of $1x10^{-3}$ is received. If software wishes to do this, it should program a write to the 'Force AIS' register bit in its signal fail interrupt service routine.

3.3.2.12 Scrambler

After going through the line AIS Multiplexer, the data is optionally scrambled with the frame synchronous SONET scrambler. The scrambler is used to guarantee that the bit pattern does not have a long sequence of 1s or 0s in it. The generating polynomial is: $1 + x^6 + x^7$. It is reset to "1111111" on the most significant bit of the byte following the last byte of the first row (last Z0 byte) of the STS-N/STM-M section overhead. This bit and all subsequent bits to be scrambled are added modulo 2 to the output from the X^7 position of the scrambler, which runs continuously throughout the complete STS-N/STM-M frame stopping at the first bit of A1. The A1, A2, and J0/Z0 bytes are not scrambled. A set of signals from the frame counter control when the scrambler is ON, OFF, or reset.

To disable scrambling without a processor connected to the S3062, de-assert the SCRBEN I/O pin. With a processor connected, write a '1' to the 'Scrmbl OFF' register bit and enable software register control by writing a 59h to the Micro Present byte. The controls set by the processor override the signals on the I/O pins when the Micro Present byte contains a value of 59h.

3.3.2.13 Data Off Multiplexer

After scrambling, the data arrives at this block. The multiplexer chooses between the data and all-zeros according to either the state of the DATAOFF signal if the Micro Present byte is not active or the 'Force LOS' register bit.

Finally the data runs through the Pass-Through MUX, FEC Encoder and lastly the 2:1 MUX before exiting the chip. Note that all encoding happens after the all-zero multiplexer. The result of encoding all-zero data is the FSB followed by the all-zero data followed by non-zero parity bytes.

3.3.2.14 Transmit Multiplexer Summary: Line Overhead and Data

The transmitter multiplex priority is (from highest to lowest):

1. Differential encoding and decoding and FEC encoding and decoding (highest priority)
2. Low power Pass-Through Data
3. Data OFF (unscrambled, all zeros)
4. Force line AIS (initiated by user)
5. Automatic line AIS (initiated by a received LOS, LOF condition if enabled by user)
6. Overhead Insert Data (from TX Overhead memory)
7. Overhead Insert Data (from Serial Links)
8. Regenerated B2 insertion
9. Received line overhead and data (lowest priority)

For example, if the user turns the Data OFF (to all-zeros), all of the enables and disables and selections in points 4-9 are irrelevant; the data becomes zero. The selections in points 1 and 2 will still have an effect, however, since they are higher in priority than point 3. This means that if the FEC encode is ON, the data will be all-0s encoded with forward error correction. The end result will be (with T=8) 4 FSB bytes whose value is specified by the Encode FSB register, followed by 238*4 bytes of zeros, followed by 4*16 bytes of non-zero FEC parity information.

3.3.2.15 Transmit Multiplexer Summary: Section Overhead

Since line AIS does not affect the section overhead, the transmit multiplexer only changes section overhead as follows:

1. Differential encoding and decoding and FEC encoding and decoding (highest priority)
2. Low power Pass-Through Data
3. Data Off (unscrambled, all zeros)
4. Overhead Insert Data (from TX Overhead memory)
5. Overhead Insert Data (from Serial Links)
6. Regenerated A1, A2, B1, and J0 (section trace) insertion
7. Received section overhead (lowest priority)

For example, if the user turns the data OFF (to all-zeros), all of the enables and disables and selections in points 4-7 are irrelevant; the data becomes zero. The selections in points one and two will still have an effect, however, since they are higher in priority than point three.

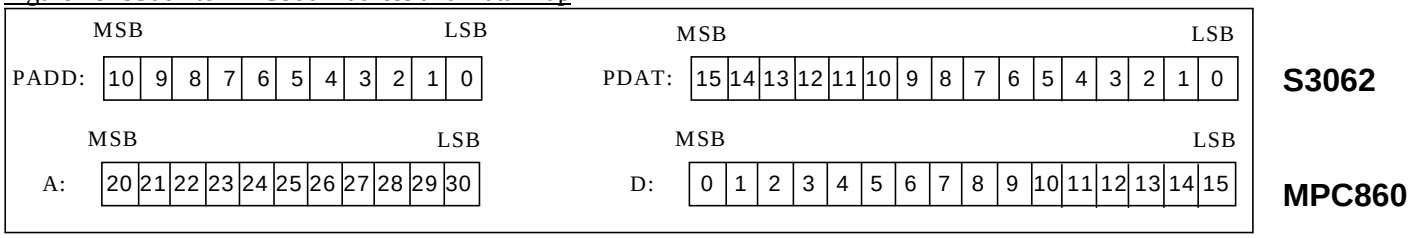
3.3.3 SONET/SDH Generation-only Mode

For testing purposes, the S3062 may be used to generate valid transport overhead for SONET/SDH. The user must supply the input clocks (CLKINP/N and TXCLKP/N) and must be sure that the FIXSOH, FIXB2, and AUTOAIS are selected either through software or hardware. Overhead insertion from the TX_OH memory must also be OFF for the A1, A2, B1 and B2 bytes. The output will be SONET/SDH frames showing line AIS. The user may then also generate correct J0, E1 and section DCC bytes through software or hardware if desired.

3.4 Detailed Operation – Processor Interface

The processor interface operates, synchronously, as a slave to the MPC860 Communications Controller with a maximum bus speed of 50MHz. Access to the S3062 registers is provided for the purposes of OAM&P (operations, administration, maintenance, and provisioning). All S3062 registers, including the overhead memories, are addressed as 16-bit entities by the MPC860. All memories can be accessed with both normal, single beat, as well as burst cycle transfers. Registers, however, can only be accessed one address at a time. Since the MPC860 will always be accessing registers on the S3062 as 16-bit words, then the least significant bit of MPC860 address bus (used to address byte-wide registers), will not be connected. The address and data buses of the S3062 (PADD[10:0] and PDAT[15:0]) will be connected to the MPC860 address and data buses (A[20:30] and D[0:15]) as shown in Figure 18 .

Figure 18 S3062 to MPC860 Address and Data Map



The synchronous, 8-word, burst mode of operation can be used in order to achieve the required <48 ns cycle times (125 us / (1296 reads + 1296 writes)) for access of all of the receive, and transmit overhead bytes within a frame time. All burst accesses must be synchronized to the frame pulse signal (FPOUTB) to insure that all bytes are extracted from a single frame, and all bytes are inserted into a single frame.

Non-burst (normal single beat) access of the section trace, RX_OH, and TX_OH Memories is also provided via the MPC860 interface. For the purpose of arbitration, the FPGA (if present) will have priority over the MPC860 (if present) in gaining access to the Overhead Data Memories. Access of the 'Transmit Overhead Data Memory' (TX_OH) is further restricted by the enables contained in the 'Transmit Access Control Memory', as described in the TAC description, section 3.3.2.8.

The S3062's processor transfer acknowledge signal (PTA) is re-timed internally with the transmit clock (TXCLKP/N) for all accesses except the Special Clock-Independent registers. If the transmit clock fails, a processor access of any location, other than Special Clock-Independent registers, will result in a bus error. If the transmit clock fails, software should wait 18 processor bus clock cycles for the clock monitors to run, and then check the 'Special Interrupt Register' bits to see if a clock failure was the reason for the bus error. Not all of the S3062 registers are independent of the receive clock (CLKINP/N). The receive clock and the transmit clock are required to access the FEC decode registers.

Bus errors will also occur if the processor accesses registers/memories that do not exist, belong to an unselected mode or if the processor attempts to access any registers in burst mode. The Section Trace, TX_OH, RX_OH, OIC and TAC memories are accessible in burst mode.

Software should program the MPC860 to expect an external transfer acknowledge when accessing the S3062. Make sure the processor's bus error timeout is slightly longer than the longest access time. The worse case access times for the various modes are as follows:

Table 13 Worse Case Access Times

Processor Bus Speed	STS-48	STS-12	STS-3
50MHz	348ns	1.515us	4.576us
40MHz	400ns	1.425us	4.475us

3.5 Detailed Operation -- Reset

The reset (RESETB) input is routed to all the internal circuits of the S3062, forcing them into the reset state and holding them there for as long as it is active. The RESETB input is implemented using a Schmitt type receiver. It is asynchronous to the input clock. RESETB should be asserted for at least 40ns to allow for propagation through the chip.

The S3062 reset should be kept separate from the physical layer chips that provide clocking for the S3062. The S3062 may then be held in reset when power is applied, until the input clocks to the S3062 are present and stable.

If the Micro Present byte is active, software can also reset the chip from the 'Force Reset' bit. In this case, however, the processor interface block is not reset nor is the Micro Present byte nor the software-written reset bit. To terminate the software-initiated reset, the software must clear its reset-enable bit.

Warning:

- As detailed in section Table 93 , the S3062 must not touch CLKOUTP after the MUX has sampled and locked to it. If the S3062 is reset after this point, then the user must pulse the PHINIT input on the MUX to force it to re-check the TXCLK alignment.

3.6 Detailed Operation --Testability

The S3062 has a slave Test Access Port (TAP) run from the JTAG standard test pins, TCLK, TMS, TDI, TDO, TRSTB. Through the TAP, the user can access the ID register and turn ON and OFF boundary scan. The S3062 also has internal scan and Memory BIST capability, but these cannot be run from the JTAG TAP. Instead, the user must activate a set of test mode pins according to the Table 14 . Since this is a single path, through-data device, it has no capability for loopbacks. Test coverage on the chip is 97%. See Table 15 for an explanation of the JTAG ID number.

Table 14 TAP Test Modes

TM	TRSTB	TST_SE	LV_TM	BIST_EN	CLOCKS USED	DESCRIPTION
0	0	0	0	0	TXCLK, CLKIN, PCLK	Normal mode: no test features active, the chip runs in GBE, SONET/SDH or PASSTHRU modes as specified by the pins or software. Memory BIST and TAP are not active in this mode. Also hold BIST_CLK low during this mode of operation.
1	0	May change state.	1	0	TXCLK, CLKIN, PCLK	Internal Scan mode: vectors are scanned in and out of test pins (see TST_IN_ and TST_OUT_ pins in the pin list) to verify the structural integrity of the device
1	0	0	0	1	BIST_CLK, TXCLK, CLKIN	Memory BIST: the internal memories are automatically tested in this mode. While the test is running, the MBIST_ON signal is active. When the test is complete, MBIST_DONE activates and MBIST_GO is valid. MBIST_GO is high if the test has passed or low if the test has failed.
x	May change state.	x	x	x	TCLK	JTAG TAP mode: instructions are scanned in to activate boundary scan, by-pass modes or to read the ID register. Then the boundary pads can be scanned, scan data can be passed through the chip or the ID register can be read.

Table 15 JTAG ID Number and Bit Definitions

JTAG ID Number:	0000	0000	0000	0000	0011	0001	1110	0001
8-bit Version Number	0000							
16-bit Part Number		0000	0000	0000	0011			
11-bit MFG ID Number						0001	1110	000
Indicates JTAG Standard								1

3.7 Detailed Operation -- Register Map

NOTES:

- Bit numbers are in decimal. All other values are in hex.
- All accesses are 16 bits wide; however, counts that require more than a word have been lined up with the most significant word in the even address so that software can access them as long words. The MPC860 will take care of changing the long word access into two word accesses.
- The least significant bit of a register is bit 0. The most significant is bit 15.
- Unless otherwise stated, an active signal is always a '1'. A cleared signal is always a '0'.
- Register descriptions are described for an active high signal. For example, in register 001, bit 5 “select[s] pass-through mode”. This means that if bit 5 is a ‘1’, the chip will be in pass-through mode; otherwise, it will not be.
- All registers, with the exception of the Special Clock-Independent registers, require the TXCLKP/N clock to be present or software will be unable to access them. The FEC decode registers are dependent on the presence of both the RXCLKP/N (CLKIN) and the TXCLKP/N.
- All undefined register addresses will cause bus errors (will not return Transfer Acknowledge) if accessed.

Register Mode Definitions: The register modes are listed by bit in the register map: Table 18 – Table 72 .

- RW = read/write (owned by software)
- RO = read only (owned by hardware)
- RC = read clear (set by hardware, cleared by software reads)

Table 16 Register Map Summary

Address	Accessible in†††	Default value‡‡‡	Description
000	all modes	0000	ID Register
001	all modes	A610	Global Control
002	SONET mode	0060	Receive SONET/SDH Overhead Control
003	SONET mode	0000	Transmit SONET/SDH Overhead Control
004	SONET mode	0000	Section Trace Control: Receive and Transmit
005	SONET mode	00f9	SD BER Threshold
006	SONET mode	0000	SD BER Accumulation Period: MSB
007	SONET mode	000a	SD BER Accumulation Period: LSB
008	SONET mode	2666	SF BER Threshold
009	SONET mode	0008	SF BER Accumulation Period
00A	SONET mode	1abb	Clock Enable and APS Interrupts
00B	SONET mode	02d5	Enable BIP-8, S1, RDI and Section Trace Interrupts
00C	Gigabit Ethernet mode	0000	Gigabit Ethernet Control, Failures and PMs
00D	all modes	0000	Test Register
00E	all modes	<values on pins>	Status of the External Control Pins
00F	all modes	<values on pins>	External FEC Control Pins Status

††† Bus errors will occur if the chip is in the wrong mode for a particular address.

‡‡‡ The default values shown as <status> actually start as 0000 (with the exception of register 071 which starts as 0001 and the memories which start in a random state), but they will change as soon as a new status or interrupt or PM is received; thus, the default value may never be read and should not be expected.

Address	Accessible in†††	Default value‡‡‡	Description
010	SONET mode	<status>	Clock and APS failures
011	SONET mode	<status>	BIP-8, S1, RDI and Section Trace failures
012	SONET mode	<status>	PM Register
013	SONET mode	<status>	B1 Error PM Count
014	SONET mode	<status>	B2 Error PM Count – MSB
015	SONET mode	<status>	B2 Error PM Count – LSB
016	SONET mode	<status>	REI_L PM Count – MSB
017	SONET mode	<status>	REI_L PM Count – LSB
018	SONET mode	<status>	Validated K1 and K2 Values
019	SONET mode	<status>	Validated S1 Value
01A	Gigabit Ethernet mode	<status>	Gigabit Ethernet Failures
01B	Gigabit Ethernet mode	<status>	Gigabit Ethernet Invalid Code Word PM Count
01C	Gigabit Ethernet mode	<status>	Gigabit Ethernet Disparity Error PM Count
01D	Gigabit Ethernet mode	<status>	Gigabit Ethernet Sync Loss PM Count
01E	Gigabit Ethernet mode	<status>	Combined Gigabit Ethernet PM Count
01F	-- no modes --	--	-- undefined --
020	FEC decode on	0000	FEC Decode General Controls
021	FEC decode on	243c	FEC Decode Synchronization Controls
022	FEC decode on	ffff	FEC Out-of-Frame FSB Check Enable/Data Link Bit Selection(MSB)
023	FEC decode on	ffff	FEC Out-of-Frame FSB Check Enable/Data Link Bit Selection(LSB)
024	FEC decode on	fc00	FEC In-Frame FSB Check Enable (MSB)
025	FEC decode on	003f	FEC In-Frame FSB Check Enable (LSB)
026	FEC encode on	0000	FEC Encode General Controls
027	FEC encode on	003c	FEC Encoding Synchronization Controls
028	FEC encode on	ffff	FEC Encoding FSB/Data Link Bit Selection (MSB)
029	FEC encode on	ffff	FEC Encoding FSB/Data Link Bit Selection (LSB)
02A	all modes	0000	Clock Dividers
02B	all modes	0000	Encoding and Decoding General Controls
02C	all modes	0000	Error Injection
02D	all modes	0000	Data Error Injection
02E-02F	-- no modes --	--	-- undefined --
030	FEC decode on	<status>	Corrected Ones Count (MSB)
031	FEC decode on	<status>	Corrected Ones Count (LSB)
032	FEC decode on	<status>	Corrected Zeros Count (MSB)
033	FEC decode on	<status>	Corrected Zeros Count (LSB)
034	FEC decode on	<status>	Total Corrected Bits Count (MSB)
035	FEC decode on	<status>	Total Corrected Bits Count (LSB)
036	FEC decode on	<status>	Total Corrected Bytes Count (MSB)
037	FEC decode on	<status>	Total Corrected Bytes Count (LSB)
038	FEC decode on	<status>	Uncorrectable 255-Byte Block Count (MSB)
039	FEC decode on	<status>	Uncorrectable 255-Byte Block Count (LSB)
03A-06F	-- no modes --	--	-- undefined --
070	all modes	001e	Special Interrupt Enables
071	all modes	<status>	Special Interrupt Register
072-07F	-- no modes --	--	-- undefined --
080-09F	SONET mode	x	Expected Section Trace Message
0A0-0BF	SONET mode	<status>	Received Section Trace Message

Address	Accessible in†††	Default value‡‡‡	Description
0C0-0DF	SONET mode	x	Transmit Section Trace Message
0E0-0FF	-- no modes --	--	-- undefined --
100-3FF	SONET mode	<status>	Receive Overhead Memory (RX_OH)
400-6FF	SONET mode	x	Transmit Overhead Memory (TX_OH)
700-77F	SONET mode	x	Overhead Insert Control Memory (OIC)
780-7FF	SONET mode	x	Transmit Access Control Memory (TAC)

3.7.1 Register map details: Control

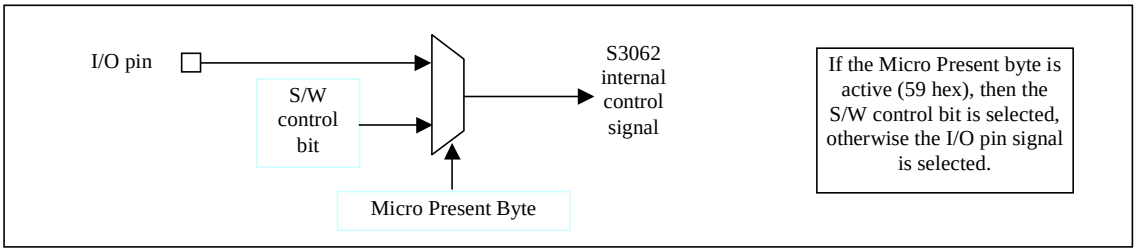
3.7.1.1 Control Bits vs. I/O Pins

Control bits are available through the processor port only. If software enables processor control by writing 59h to the Micro Present byte, the register bits, and not the I/O pins, will affect the chip. There are three exceptions to this rule to permit both hardware and software control even when the software is present. When the Micro Present byte is activated:

- Force Reset register bit will be ORed with the inverted hardware RESETB bit.
- Orderwire and DCC enables will be ORed with their respective I/O enables.
- Inverted FEC disable bits will be ANDed with their respective I/O enables.

If the Micro Present byte is not programmed with a value of 59h, control of the chip will only be available on all of the I/O pins and through the registers bits that are not shared with a pin. Only the pins listed in following three tables are affected by the value of the Micro Present byte.

Figure 19 Micro Present Byte Control MUX



Note from the above diagram that the Micro Present byte does not affect whether or not a bit can be written. If the Micro Present byte is programmed to a value other than 59h and the PASSTHRU pin is active, the S3062 will be in pass-through mode. When the user writes a "0" to the 'Pass-Through' register bit, to de-select pass-through mode, the chip will remain in pass-through mode until the user programs the Micro Present byte to the desired value of 59h or de-selects the PASSTHRU I/O pin. Thus, the bit can be written, but it has no effect if the Micro Present byte has not been programmed with a value of 59h.

The Global control register bits and the I/O pins that provide similar functions are in the following table. All signals are active high except where noted.

Table 17 Shared Functions: Register Bit and I/O Pins

Address	Bit	Bit Name	Description	I/O Pin
000	15	PM Tick	Transfers PM counts to registers on low to high transition.	PM_CLK
001	6	Force Reset	Forces a chip reset. When active low the pin resets the S3062, conversely, the bit clears a software reset.	RESETB
001	5	Pass-Through	Enable pass-through mode.	PASSTHRU
001	4-3	Rate Select	Selects the data rate. Bit selection corresponds to specific data rate.	RATESEL[1:0]
001	2	Force LOS	Forces SONET/SDH block output to all zeros.	DATAOFF
001	1	PM Tick ON	Enable for PM Tick.	Related to PM_CLK
001	0	Insert OH	Allows the selected bits in the OIC to determine which bytes from memory are inserted into the outgoing data stream.	MEMOH

The SONET/SDH register control bits and the I/O pins that provide similar functions are in the continuation of Table 17 . All signals are active high except where noted.

Address	Bit	Bit Name	Description	I/O Pin
002	9	Descr_OFF	Enables the SONET/SDH descrambler. When active high the pin enables the descrambler, conversely, the bit disables the descrambler.	DESCRBEN
002	8 7	Block B1s Block B2s	Count erred B1s (bit 8) and B2s (bit 7) by block. This means that if 6 errors occur in one byte, only 1 error is counted. A block is defined here as one byte.	BLOCKBIP
003	11	Scrmbl OFF	Enables the SONET/SDH scrambler. When active high the pin enables the scrambler, conversely, the bit disables the scrambler.	SCRBEN
003	10	Don't Fix SOH	Enables section overhead correction (A1, A2, B1). When high the pin fixes SOH while the bit does not fix SOH.	FIXSOH
003	9 4	XOR B1 XOR B2	XOR inserted B1 values from the TX_OH with the regenerated B1s. XOR inserted B2 values from the TX_OH with the regenerated B2s.	XORBIP
003	7	E1 ON	Enables the section orderwire to be inserted into the data stream from the external serial input pin, TX_SOW.	TX_SOW_SEL
003	6	SDCC ON	Enables the section DCC to be inserted into the data stream from the external serial input pin, TX_SDCC.	TX_SDCC_SEL
003	5	Fix B2	Recalculates the transmitted line BIP-8 (B2) byte.	FIXB2
003	3	E2 ON	Enables the line orderwire to be inserted into the data stream from the external serial input pin, TX_LOW.	TX_LOW_SEL
003	2	LDCC ON	Enables the line DCC to be inserted into the data stream from the external serial input pin, TX_LDCC.	TX_LDCC_SEL
003	1	Auto AIS	Automatically sends an AIS downstream upon the detection of a LOS or LOF.	AUTOAIS
003	0	Force AIS	Forces a line AIS to downstream devices after SONET/SDH monitoring and overhead insertion.	DATAAIS

The FEC control register bits and the I/O pins that provide similar functions are listed in the continuation of Table 17 . All signals are active high except where noted.

Address	Bit	Bit Name	Description	I/O Pin
02B	3	FEC Encode OFF	Enables FEC encoding. When active high the pin enables FEC encoding, conversely, the register bit disables FEC encoding.	FEC_ENC
02B	2	FEC Decode OFF	Enables FEC decoding. When active high the pin enables FEC decoding, conversely, the register bit disables FEC decoding.	FEC_DEC

3.7.1.2 Control Bit Tables

Table 18 ADDR=0x000: ID Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PM Tick	--unused--							Version Number							
Mode	rw	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- **PM Tick:** Transfers performance monitoring counts and bits to the PM registers. Software must write a value of 1 and then a value of 0 to this register. The PM statistics are transferred within 10 processor clock ticks after 0 to 1 transition.
  NOTE: The Micro Present byte must be loaded with a value of 59h and the 'PM Tick ON' bit must be enabled for this bit to take affect.

- **Version Number:** **XXXX XXXX:** These bits are loaded with the chip version number.

Table 19 ADDR=0x001: Global Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Micro Present								unused	Force Reset	Pass-Through	Rate Select		Force LOS	PM Tick ON	Insert OH
Mode	rw	rw	rw	rw	rw	rw	rw	rw	ro	rw	rw	rw	rw	rw	rw	rw
Default	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0

- **Micro Present:** **1010 0110:** Default. Value = A6h. I/O pins function as stated in the pin description list.
  0101 1001:. Value = 59h. Gives the user register control of the I/O pin functions.
  Any other value: I/O pins function as stated in the pin description list.

- **Force Reset:** **1:** Forces the chip into reset and keeps it there until it is cleared.
  0: Default. Clears the forced reset. Normal operation.[§§§]
  NOTE: This bit is ORed with the inverted RESETB control pin when the Micro Present byte is loaded with a value of 59h.

- **Pass-Through:** **1:** Enable pass-through mode.
  0: Default. Disable pass-through mode.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **Rate Select:** **(bit4 bit3)**
  (0 0): STS-3/STM-1
  (0 1): STS-12/STM-4
  (1 0): STS-48/STM-16 Default.
  (1 1): Gigabit Ethernet
  NOTE: The Micro Present byte must be loaded with a value of 59h for these bits to take affect. If pass-through mode is enabled these bits will also have no effect. Pass-through has a higher priority than Rate Select – see Sections 3.3.2.14 and 3.3.2.15 for a list of mode priorities.

- **Force LOS:** **1:** Forces the SONET/SDH block output to all-zeros (LOS).
  0: Default. Normal operation.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **PM Tick ON:** **1:** Enables the PM Tick register to generate the performance monitoring tick that transfers all PM counts and information to the PM registers.
  0: Default. Disables PM Tick from transferring the PM counts to the PM registers.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **Insert OH:** **1:** Inserts data from the overhead memory into the outgoing data stream using the OIC.
  0: Default. No overhead memory insertion.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

[§§§] See warning about reset in Section 3.5.

Table 20 ADDR=0x002: Receive SONET/SDH Overhead Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	--unused--					Force OOF	Descr OFF	Block B1s	Block B2s	SF ON	SD ON	SDH AIS	Expected S1			
Mode	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0

- **Force OOF:** **1:** Forces the framing circuit to go out-of-frame and start the search for a new frame alignment.
  0: Default. Clears forced OOF.
  NOTE: The hardware will clear this bit once it re-finds the frame (normally 125-250µs after the bit set).

- **Descr OFF:** **1:** Disables descrambling of the incoming data.
  0: Default. Enables descrambling on the incoming data.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **Block B1s:** **1:** Count erred B1s (block errors) instead of errors within the B1.
  0: Default. Count every error within each B1 block (1 byte).
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **Block B2s:** **1:** Count erred B2s (block errors) instead of errors within the B2.
  0: Default. Count every error within each B2 block (1 byte).
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **SF ON:** **1:** Default. Enables signal fail BER monitor.
  0: Disables signal fail BER monitor.

- **SD ON:** **1:** Default. Enable signal degrade BER monitor.
  0: Disables signal degrade BER monitor.

- **SDH AIS:** **1:** Detects AIS_L and RDI_L after 3 consecutive frames. SDH mode.
  0: Default. Detects AIS_L and RDI_L after 5 consecutive frames. SONET mode.

- **Expected S1:** **XXXX:** The expected value in the receive synchronization portion of the S1 byte (the 4 least significant bits).
  NOTE: This is the four least significant bits of the expected value.

Table 21 ADDR=0x003: Transmit SONET/SDH Overhead Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	--unused--				Scrmbl OFF	Don't Fix SOH	XOR B1	Send J0 Msg	E1 ON	SDCC ON	Fix B2	XOR B2	E2 ON	LDCC ON	Auto AIS	Force AIS
Mode	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- **Scrmbl OFF:**
  1: Disables scrambling the transmitted data stream.
  0: Default. Enables scrambling the transmitted data.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **Don't Fix SOH:**
  1: Disable section overhead correction (A1, A2, B1).
  0: Default. Enable section overhead correction (A1, A2, B1).
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **XOR B1:**
  1: XOR inserted B1 byte values from the TX_OH with the regenerated B1 byte values. The XOR value is inserted into the data stream.
  0: Default. Regenerated/Inserted B1 byte values are inserted into the transmitted data stream.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **Send J0 Msg:**
  1: Transmit the Transmit Section Trace Message in the J0 byte.
  0: Default. Do not transmit the Transmit Section Trace Message in the J0 byte.

- **E1 ON:**
  1: Enables the section orderwire (E1) to be inserted from the external serial input pin.
  0: Default. No section orderwire is inserted into the transmitted data stream from the serial inputs.
  NOTE: This bit is ORed with the TX_SOW_SEL control pin.

- **SDCC ON:**
  1: Enable the section DCC (D1-3) to be inserted from the external serial input pin.
  0: Default. No section DCC's are inserted into the transmitted data stream from the serial input.
  NOTE: This bit is ORed with the TX_SDCC_SEL control pin.

- **Fix B2:**
  1: Recalculates the transmitted line BIP-8 (B2) byte.
  0: Default. The B2 byte will be passed through as-is from the receive blocks. If any line overhead bytes are changed, the B2 byte will be recalculated and inserted regardless of the state of this bit.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **XOR B2:**
  1: XOR inserted B2 byte values from the TX_OH with the regenerated B2 values. The XOR value is inserted into the transmitted data stream.
  0: Default. Regenerated/Inserted B2 byte values are inserted into the transmitted data stream.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **E2 ON:**
  1: Enables the line orderwire (E2) to be inserted into the data stream from the external serial input pin.
  0: Default. No line orderwire is inserted into the transmitted data stream from the serial inputs.
  NOTE: This bit is ORed with the TX_LOW_SEL control pin.

- **LDCC ON:**
  1: Enables the line DCC (D4-12) to be inserted from the external serial input pin.
  0: Default. No line DCC's are inserted into the transmitted data stream from the serial input.
  NOTE: This bit is ORed with the TX_LDCC_SEL control pin.

- **Auto AIS:** **1:** A line AIS is automatically sent to downstream monitoring blocks upon the detection of a LOS or LOF.
  0: Default. If an LOS or LOF is detected the downstream monitoring blocks are not affected.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

- **Force AIS:** **1:** Forces a line AIS to downstream devices after SONET/SDH monitoring and overhead insertion. Note that this only affects the output of the SONET/SDH block. FEC encoding and scrambling will still affect the output out of the S3062.
  0: Default. Normal operation.
  NOTE: The Micro Present byte must be loaded with a value of 59h for this bit to take affect.

Table 22 ADDR=0x004: Section Trace Control: Receive and Transmit

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	--unused--									Check 5	As-is	SDH-64	SONET-16	Circular Buffer	Length	
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

- **Check 5:** **1:** Detect new J0 message after 5 repetitions.
  0: Default. Detect new J0 message after 3 repetitions.

- **As-is:** **1:** Write the received J0 message into the 'Receive Section Trace Memory' without validation.
  0: Default. Determine if the received J0 message is valid before writing it into the section trace memory.

- **SDH-64:** **1:** If 64 byte messaging is selected, SDH format for the message start is expected. The state machine will be looking for a 1 bit in the MSB of the first byte to indicate the first byte of the message. A zero will exist in the MSB of every byte except the first..
  0: Default. If 64 byte messaging is selected, SONET format for the message start is expected. The state machine will be looking for a CR character followed by a LF character to indicate that the next character is the first character of the message.

- **SONET-16:** **1:** If 16 byte messaging is selected, SONET format for the message start is expected. The state machine will be looking for a CR character followed by a LF character to indicate that the next character is the first character of the message.
  0: Default. If 16 byte messaging is selected, SDH format for the message start is expected. The state machine will be looking for a 1 bit in the MSB of the first byte to indicate the first byte of the message. A zero will exist in the MSB of every byte except the first.

- **Circular Buffer:** **1:** Treat the memory as a simple circular buffer, messages may start anywhere.
  0: Default. Find the defined message start byte and store the messages in memory accordingly.

- **Length:** **(bit1 bit0)**
  (0 0): 1 byte J0 message length. Default.
  (0 1): 1 byte J0 message length.
  (1 0): 16 byte J0 message length.
  (1 1): 64 byte J0 message length.

Table 23 ADDR=0x005: SD BER Threshold

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1

- The default is the STS-48/STM-16 $1x10^{-5}$ value.
- Goto Table 12 to determine the programmable value based on a uniform distribution of errors.

Table 24 ADDR=0x006-0x007: SD BER Accumulation Period

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	--unused--					MSB										
Mode	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	LSB															
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

- The default is the $1x10^{-5}$ value.
- Goto Table 12 to determine the programmable value based on a uniform distribution of errors.

Table 25 ADDR=0x008: SF BER Threshold

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	1	0	0	1	1	0	0	1	1	0	0	1	1	0

- The default is the STS-48/STM-16 $1x10^{-3}$ value.
- Goto Table 11 to determine the programmable value based on a uniform distribution of errors.

Table 26 ADDR=0x009: SF BER Accumulation Period

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

- The default is the $1x10^{-3}$ value.
- Goto Table 11 to determine the programmable value base on a uniform distribution of errors.

Table 27 ADDR=0x00A: Clock Enable and APS Interrupts

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused			RX Clk Ion	TX Clk Ion	unused	LOS Ion	unused	LOF Ion	unused	AIS Ion	SF Ion	SD Ion	unused	Inconsistent APS Ion	New APS Ion
Mode	ro	ro	ro	rw	rw	ro	rw	ro	rw	ro	rw	rw	rw	ro	rw	rw
Default	0	0	0	1	1	0	1	0	1	0	1	1	1	0	1	1

Ion = Interrupt ON = Enable Interrupt

- **RX Clk Ion[****]:** **1:** Default. Enable interrupt for RX input clock (CLKINP/N) failure.
  0: Disable interrupt.
- **TX Clk Ion[****]:** **1:** Default. Enable interrupt for TX input clock (TXCLKP/N) failure.
  0: Disable interrupt.
- **LOS Ion:** **1:** Default. Enable interrupt for a change of state in LOS.
  0: Disable interrupt.
- **LOF Ion:** **1:** Default. Enable interrupt for a change of state in LOF.
  0: Disable interrupt.
- **AIS Ion:** **1:** Default. Enable interrupt for a change of state of AIS_L.
  0: Disable interrupt.
- **SF Ion:** **1:** Default. Enable interrupt for signal fail (SF).
  0: Disable interrupt.
- **SD Ion:** **1:** Default. Enable interrupt for signal degrade (SD).
  0: Disable interrupt.
- **Inconsistent APS Ion:** **1:** Default. Enable interrupt for a change of state in inconsistent APS (K1) alarm.
  0: Disable interrupt.
- **New APS Ion:** **1:** Default. Enable interrupt for a new APS (K1/K2) received.
  0: Disable interrupt.

[****] The RX and TX Clk Interrupts are also located in register 0x071 Special Interrupt Register. Each location has separate Interrupt Enables so please verify that the proper enables are setup for all interrupts. The Interrupts for both RX Clk Intr and TX Clk Intr are contained in register 0x010 Clock and APS Failures.

Table 28 ADDR=0x00B: Enable BIP-8, S1, RDI and Section Trace Interrupts

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused			B1 Ion	B2 Ion	unused	Inconsistent S1 Ion	unused	Mismatch S1 Ion	New S1 Ion	unused	RDI Ion	unused	Inconsistent J0 Ion	unused	Mismatch J0 Ion
Mode	ro	ro	ro	rw	rw	ro	rw	ro	rw	rw	ro	rw	ro	rw	ro	rw
Default	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0	1

Ion = Interrupt ON = Enable Interrupt

- **B1 Ion:** **1:** Enable interrupt for a received B1 BIP-8 error.
  0: Default. Disable interrupt.
- **B2 Ion:** **1:** Enable interrupt for a received B2 BIP-8 error.
  0: Default. Disable interrupt.
- **Inconsistent S1 Ion:** **1:** Default. Enable interrupt for a change of state of inconsistent S1 message.
  0: Disable interrupt.
- **Mismatch S1 Ion:** **1:** Default. Enable interrupt for a change of state of mismatched S1.
  0: Disable interrupt.
- **New S1 Ion:** **1:** Default. Enable interrupt for a new S1.
  0: Disable interrupt.
- **RDI Ion:** **1:** Default. Enable interrupt for a change of state of RDI_L.
  0: Disable interrupt.
- **Inconsistent J0 Ion:** **1:** Default. Enable interrupt for a change of state of inconsistent RX J0 message.
  0: Disable interrupt.
- **Mismatch J0 Ion:** **1:** Default. Enable interrupt for a change of state of RX J0 message mismatch.
  0: Disable interrupt.

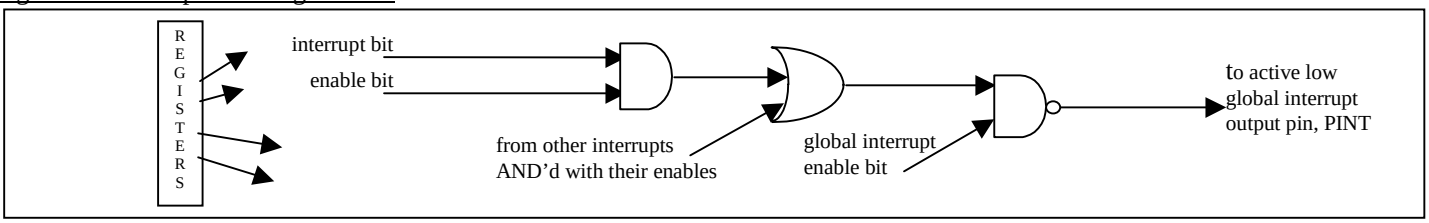
Table 29 ADDR=0x00C: Gigabit Ethernet Control, Failures and PMs

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused												IEEE On	Sync Loss Ion	Invalid Code Ion	Disparity Ion
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Ion = Interrupt ON = Enable Interrupt

- **IEEE On:** **1:** Use the IEEE Gigabit Ethernet synchronization state machine.
  0: Default. Synchronize to a single K28.5 byte per method described in Section 3.2.1.
- **Sync Loss Ion:** **1.** Enable interrupt for a change of state of Sync Loss.
  0: Default. Disable interrupt.
- **Invalid Code Ion:** **1:** Enable interrupt for a received Invalid Code.
  0: Default. Disable interrupt.
- **Disparity Ion:** **1:** Enable interrupt for a Disparity Error.
  0: Default. Disable interrupt.

Figure 20 Interrupt Enabling Method



As can be seen in Figure 20 , PINT is a level signal which remains present as long as the interrupt is present and enabled. To de-assert PINT, either clear the enable bit or attempt to clear the interrupt by reading the interrupt register.

Table 30 ADDR=0x00D: Test Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- This register is a scratch pad -- available for processor access tests. Any value can be written and read back.

Table 31 ADDR=0x00E: Status of the External Control Pins

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused	PASS THRU	RATESEL[1:0]		FPGA SEL	MEM OH	FIXSOH	SCR BEN	DESCR BEN	FIXB2	BLOCK BIP	XOR BIP	DATA AIS	AUTO AIS	DATA OFF	PM_ CLK
Mode	ro	ro	ro		ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
Default	0	x	x		x	x	x	x	x	x	x	x	x	x	x	x

- Reading this register returns the status of the listed input pins. If there is no signal connected to the input pin, the corresponding value in the register bit will be undefined.

Table 32 ADDR=0x00F: External FEC Control Pins Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused														FEC_ENC	FEC_DEC
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x

- Reading this register returns the status of the listed input pins. If there is no signal connected to the input pin, the corresponding value in the register bit will be undefined.

3.7.2 Register Map Details: SONET/SDH Status Registers for Failures, Alarms, PMs, and Validated Bytes

Software can read the values of the status registers for failures, alarms, PMs and validated bytes through the processor interface if the microprocessor is enabled by loading the Micro Present byte with a value of 59h. When the Micro Present byte is loaded with a value of 59h, the read-clear bits will only be cleared when the processor reads them. In the case where the microprocessor is not enabled, the read-clear bits will be cleared automatically by hardware. If the FPGA interface is enabled by FPGASEL and the Micro Present byte is not loaded with a value of 59h, the read-clear bits will be cleared automatically by hardware after they have been transmitted to the FPGA interface. All the SONET/SDH register values will be sent out of the FPGA interface, MSB first. The bytes will be sent in order from 010 to 019, after the RX_OH bytes.

3.7.2.1 Failures and Alarms

There are two type of interrupts shown in the tables that follow: Those, like B1, which only activate when an error condition occurs and those, like LOS, which activate both when the error condition starts and when it ends, i.e., upon “change of state”. In the latter case, the user needs to know what the current state of the error is as well as the fact that it changed. That information is provided in the read-only “current state” bits. In all cases, ‘1’ means that the interrupt or the condition is present. Thus, if the B1 interrupt bit is ‘1’, a B1 BIP error has occurred, if the LOS change of state interrupt is a ‘1’, the LOS condition has either started or ended, if the current state of LOS is now a ‘1’, there is a Loss Of Signal error, etc.

Note that the interrupt enables are in registers 00a-00c.

Table 33 ADDR=0x010: Clock and APS Failures

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused			RX Clk Intr	TX Clk Intr	LOS State	LOS Intr	LOF State	LOF Intr	AIS State	AIS Intr	SF Intr	SD Intr	Inconsistent APS State	Inconsistent APS Intr	New APS Intr
Mode	ro	ro	ro	rc	rc	ro	rc	ro	rc	ro	rc	rc	rc	ro	rc	rc
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: The Micro Present byte must be loaded with a value of 59h to use these read/clear interrupts. All read/clear bits in this register will be automatically cleared if the Micro Present byte is not loaded with a value of 59h.

- **RX Clk Intr††††:** **1:** Interrupt present: RX input clock (CLKINP/N) failed.
  0: No interrupt present.

- **TX Clk Intr††††:** **1:** Interrupt present: TX input clock (TXCLKP/N) failed.
  0: No interrupt present.
  NOTE: If the TX clock is still not running when this register is read, a bus error will occur. In that case, read the Special Interrupt Register to see the clock failure indication.

- **LOS State:** **1:** LOS has been detected and is still present.
  0: LOS is NOT present.

- **LOS Intr:** **1:** Interrupt present: Change of state in LOS.
  0: No interrupt present.

- **LOF State:** **1:** LOF has been detected and is still present.
  0: LOF is NOT present.

- **LOF Intr:** **1:** Interrupt present: Change of state in LOF.
  0: No interrupt present.

- **AIS State:** **1:** A line AIS has been detected and is still present.
  0: L_AIS is NOT present.

- **AIS Intr:** **1:** Interrupt present: Change of state of AIS_L.
  0: No interrupt present.

- **SF Intr:** **1:** Interrupt present: Signal Fail (SF).
  0: No interrupt present.

- **SD Intr:** **1:** Interrupt present: Signal Degrade (SD).
  0: No interrupt present.

- **Inconsistent APS State:** **1:** K1 is inconsistent.
  0: K1 is NOT inconsistent.

- **Inconsistent APS Intr:** **1:** Interrupt present: Change of state in inconsistent APS (K1) alarm.
  0: No interrupt present.

- **New APS Intr:** **1:** Interrupt present: New APS (K1/K2) received.
  0: No interrupt present.

†††† The RX and TX Clk Interrupts are also located in register 0x071 Special Interrupt Regester. Each location has separate Interrupt Enables so please verify that the proper enables are setup for all interrupts. The enables for both RX Clk Intr and TX Clk Intr are contained in register 0x00A Clock Enable and APS Interrupts.

Table 34 ADDR=0x011: BIP-8, S1, RDI and Section Trace Failures

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused			B1 Intr	B2 Intr	Inconsistent S1 State	Inconsistent S1 Intr	Mismatch S1 State	Mismatch S1 Intr	New S1 Intr	RDI State	RDI Intr	Inconsistent J0 State	Inconsistent J0 Intr	Mismatch J0 State	Mismatch J0 Intr
Mode	ro	ro	ro	rc	rc	ro	rc	ro	rc	rc	ro	rc	ro	rc	ro	rc
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: The Micro Present byte must be loaded with a value of 59h to use these read/clear interrupts. All read/clear bits in this register will be autmatically cleared if the Micro Present byte is not loaded with a value of 59h.

- **B1 Intr:** **1:** Interrupt present: B1 BIP-8 error received.
  0: Default. No interrupt present.
- **B2 Intr:** **1:** Interrupt present: B2 BIP-8 error received.
  0: Default. No interrupt present.
- **Inconsistent S1 State:** **1:** S1 is inconsistent. No validated value has been found 8 consecutive times in 32 frames.
  0: Default. S1 is NOT inconsistent.
- **Inconsistent S1 Intr:** **1:** Interrupt present: Change of state of inconsistent S1 message.
  0: Default. No interrupt present.
- **Mismatch S1 State:** **1:** S1 is mismatched. Validated value does not match S1expected message.
  0: Default. S1 is NOT mismatched.
- **Mismatch S1 Intr:** **1:** Interrupt present: Change of state of mismatched S1.
  0: Default. No interrupt is present.
- **New S1 Intr:** **1:** Interrupt present: A new S1 value has been validated.
  0: Default. No interrupt is present.
- **RDI State:** **1:** Line RDI has been detected and has not been cleared.
  0: Default. L_RDI is NOT present.
- **RDI Intr:** **1:** Interrupt present: Change of state of RDI_L.
  0: Default. No interrupt present.
- **Inconsistent J0 State:** **1:** J0 is inconsistent.
  0: Default. J0 is NOT inconsistent.
- **Inconsistent J0 Intr:** **1:** Interrupt present: Change of state of inconsistent RX J0 message.
  0: Default. No interrupt is present.
- **Mismatch J0 State:** **1:** J0 is mismatched.
  0: Default. J0 is NOT mismatched.
- **Mismatch J0 Intr:** **1:** Interrupt present: Change of state of RX J0 message mismatch.
  0: Default. No interrupt is present.

3.7.2.2 Performance Monitoring Bits and Counts

- All PM bits and counts are read-only and default to zero.
- All are updated on the 1 second tick. If there is no tick, the register value will not change.
- The "tick" is either the rising edge of PM_CLK or the change from 0 to 1 in bit 15 of register 000h, depending on which mode is enabled by the Micro Present byte and bit 1 of the Global Control register, address 001h
- If the tick is running, the first read of this register may not result in the default value of zero since PMs may have arrived between the time that the chip was reset with the default value and the time that the register was read.

Table 35 ADDR=0x012: PM Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused							LOS PM	OOF PM	B1 PM	B2 PM	AIS PM	REI PM	RDI PM	Inconsistent J0 PM	Mismatched J0 PM
	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
Mode	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Default																

- These bits are set if the corresponding failures occurred since the last 1 second tick.
- See GR-253 sections 6.2.2.3 and 6.2.2.4 for full descriptions of SONET/SDH PMs. Note that the J0 PMs are not defined in the SONET/SDH standards *yet*.

Table 36 ADDR=0x013: B1 Error PM Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Count															

- Contains the B1 error count.

Table 37 ADDR=0x014-0x15: B2 Error PM Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused										MSB					
Name	LSB															

- Contains the B2 error count.

Table 38 ADDR=0x016-0x17: REI_L PM Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused											MSB				
Name	LSB															

- Contains the REI_L count.

3.7.2.3 Validated Bytes

- If a new value is of K1/K2 or S1 is found and consecutively repeated (3 times for K1/K2 and 8 times for S1) the new value will be stored in the Validated Registers for software to read.
- The first read of these registers will likely result in the actual validated values rather than the default value.

Table 39 ADDR=0x018: Validated K1/K2 Value

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Validated K1								Validated K2							
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- Contains the validated K1 and K2 bytes.

Table 40 ADDR=0x019: Validated S1 Value

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused								Validated S1							
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- Contains the validated S1 synchronization byte.

3.7.3 Register Map Details: Gigabit Ethernet (GBE) Failures and Performance Monitoring Counts

3.7.3.1 Failures

There are two type of interrupts shown below: Disparity, which only activates when an error condition occurs and Sync Loss, which activates both when the error condition starts and when it ends, i.e., upon "change of state". In the latter case, the user needs to know what the current state of the error is as well as the fact that it changed. That information is provided in the read-only "current state" bits. In all cases, '1' means that the interrupt or the condition is present. Thus, if the Disparity interrupt bit is '1', a Disparity error has occurred, if the Sync Loss change of state interrupt is a '1', the Sync Loss condition has either started or ended, if the current state of Sync Loss is now a '1', there is a Sync Loss error.

Note that the interrupt enables are in register 0x00C.

Table 41 ADDR=0x01A: Gigabit Ethernet Failures

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused												Sync Loss State	Sync Loss Intr	Invalid Code Intr	Disparity Intr
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rc	rc	rc
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: the first read of this register may not result in the default value since states may have changed and interrupts may have arrived between the time that the chip was reset with the default value and the time that the register was read.

- **Sync Loss State:** **1:** Synchronization has been lost.
  0: Default. Synchronization has been found..
- **Sync Loss Intr:** **1:** Interrupt present: Change of state of sync loss.
  0: Default. No interrupt is present.
- **Invalid Code Intr:** **1:** Interrupt present: Invalid code received.
  0: Default. No interrupt is present.
- **Disparity Intr:** **1:** Interrupt present: Parity error occurred.
  0: Default. No interrupt is present.

3.7.3.2 PM Counts

- All PM counts are read-only and default to zero.
- All are updated on the 1 second tick. If there is no tick, the register value will not change.
- The "tick" is either the rising edge of PM_CLK or the change from 0 to 1 in bit 15 of register 000h, depending on which mode is enabled by the Micro Present byte and bit 1 of the Global Control register, address 001h
- If the tick is running, the first read of this register may not result in the default value of zero since PMs may have arrived between the time the chip was reset with the default value and the time the register was read.

Table 42 ADDR=0x01B: Gigabit Ethernet Invalid Code Word PM Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Count															

- Contains the number of GBE Invalid Code Words that were detected.

Table 43 ADDR=0x01C: Gigabit Ethernet Disparity Error PM Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Count															

- Contains the number of GBE Disparity Errors that were detected.

Table 44 ADDR=0x01D: Gigabit Ethernet Sync Loss PM Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Count															

- This is a count of the transitions from in-sync to out-of-sync

Table 45 ADDR=0x01E: Combined Gigabit Ethernet PM Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Count															

- The invalid-code and disparity errors are ORed together and the resultant error is counted

3.7.4 Register Map Details: Forward Error Correcting (FEC) Encoding/Decoding Control

Table 46 ADDR=0x020: FEC Decode General Controls

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused												RX FEC Data Link ON	FEC Capability		
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rw	rw		
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

- **RX FEC Data Link ON:** **1:** Enable receive FEC data link to be dropped to the serial output port, RX_FEC_DL.
  0: Default. Data link is not dropped to the serial port, RX_FEC_DL.

- **FEC Capability:** **(bit2 bit1 bit0)**
  (0 0 0): 8 bytes can be corrected. Default.
  (0 0 1): 7 bytes can be corrected
  (0 1 0): 6 bytes can be corrected
  (0 1 1): 5 bytes can be corrected
  (1 0 0): 4 bytes can be corrected
  (1 0 1): 3 bytes can be corrected
  (1 1 0): 8 bytes can be corrected
  (1 1 1): 8 bytes can be corrected

Table 47 ADDR=0x021: FEC Decode Synchronization Controls

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Check to go In-Frame				Check to go Out-of-Frame				FSB							
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	1	0	0	1	0	0	0	0	1	1	1	1	0	0

- **Check to go In-Frame:** **0010:** Default. Number of correct consecutive FSB groups required to go In-Frame. .
  Any Other Value: Programmable In-Frame check number.

- **Check to go Out-Of-Frame:** **0100:** Default. Number of incorrect consecutive FSB groups required to go Out-of-Frame.
  Any Other Value: Programmable Out-of-Frame check number.

- **FSB:** **0011 1100:** Default. 3Ch.
  Any Other Value: The programmable value of the Frame Synchronization Byte.

Table 48 ADDR=0x022-0x023: FEC Out-of-Frame FSB Check Enable/Data Link Bit Selection

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSB															
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	LSB															
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

- **MSB/LSB:**

1: The corresponding bit in the 4-byte FSB group is part of the FSB and will be checked for correct frame value when the framer is out-of-frame and trying to go in-frame.

0: The corresponding bit will not be checked for the correct frame value (and if the FEC data link is enabled) this bit will be part of the data link. The selected data link bits must match the selected data link bits in ADDR=0x024-0x025.

NOTE: The default of FFFF means check all framing bits -- no data link.

Table 49 ADDR=0x024-0x025: FEC In-Frame FSB Check Enable

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSB															
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	LSB															
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1

- **MSB/LSB:**

1: The corresponding bit in the 4-byte FSB group will be checked for the correct frame value when the framer is in-frame.

0: The corresponding bits will not be checked for the correct frame value. The unselected bits must include, but are not limited to, the unchecked bits in ADDR=0x022-0x023 for the data link to work properly.

NOTE: The default of FC00 003F mean that the most and least significant 6 bits are checked.

Table 50 ADDR=0x026: FEC Encode General Controls

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused												TX FEC Data Link ON	FEC Capability		
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- **TX FEC Data Link ON:** **1:** Enables transmit FEC data link to be added from the serial input port, TX_FEC_DL
  0: Default. Data link is not added from the serial input port, TX_FEC_DL. If the receive and transmit data links are defined and the identical bit rates are chosen (bit locations do not have to be identical), the RX FEC Data Link is passed through and out the TX FEC Data Link.

- **FEC Capability:** **(bit2 bit1 bit0)**
  (0 0 0): 8 bytes can be corrected. Default.
  (0 0 1): 7 bytes can be corrected
  (0 1 0): 6 bytes can be corrected
  (0 1 1): 5 bytes can be corrected
  (1 0 0): 4 bytes can be corrected
  (1 0 1): 3 bytes can be corrected
  (1 1 0): 8 bytes can be corrected
  (1 1 1): 8 bytes can be corrected

Table 51 ADDR=0x027: FEC Encode Synchronization Controls

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused								FSB							
Mode	ro	ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0

- **FSB:** **0011 1100:** Default. 3Ch.
  Any Other Value: The programmable value of the Frame Synchronization Byte.

Table 52 ADDR=0x028-0x029: FEC Encode FSB/Data Link Bit Selection

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MSB															
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	LSB															
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

- **MSB/LSB:** **1:** The corresponding bit is part of the FSB.
  0: The corresponding bit will be part of the data link. The number of encode data link bits must equal the number of decode data link bits for the data link to be passed through the S3062. The location of the bits do not have be the same, just the number/code rate.
  NOTE: The default of FFFF means that all bits are part of the FSB; there are no data link bits.

3.7.5 Register Map Details: Clock Dividers, Encoding/Decoding Enables, Error Injection

Table 53 ADDR=0x02A: Clock Dividers[‡‡‡‡]

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX Clock Divider								TX Clock Divider							
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- **RX Clock Divider:** **0000 0000:** Default. RX_DIV clock OFF.
  Any Other Value: The RX clock will be divided by this number.

- **TX Clock Divider:** **0000 0000:** Default. TX_DIV clock OFF.
  XXXX XXXX: The TX clock will be divided by this number.

Table 54 ADDR=0x02B: Encoding and Decoding General Controls

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused												FEC Encode OFF	FEC Decode OFF	Differential Encode ON	Differential Decode ON
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- **FEC Encode OFF:** **1:** Disables FEC encoding. The outgoing data stream will not be FEC encoded.
  0: Default. Enables FEC encoding.
  NOTE: The inverse of this register bit is ANDed with the FEC_ENC control pin when the Micro Present byte is loaded with a value of 59h.

- **FEC Decode OFF:** **1:** Disables FEC decoding. The incoming stream will not be FEC decoded.
  0: Default. Enables FEC decoding.
  NOTE: The inverse of this register bit is ANDed with the FEC_DEC control pin when the Micro Present byte is loaded with a value of 59h.

- **Differential Encode ON[§§§§]:** **1:** Enables differential encoding.
  0: Default. Disables differential encoding.

- **Differential Decode ON:** **1:** Enables differential decoding.
  0: Default. Disables differential decoding.

[‡‡‡‡] This register will only have an affect if software has activated the Micro Present byte (written 59h to register 001); otherwise, the RX and TX clocks will be divided down according to Table 5 .

[§§§§] Different versions of the silicon require that the Micro Present byte be loaded with a value of 59h for the Differential Encode ON bit to take affect. Please consult Errata 7.3 Differential Encode Enable in the back of the data sheet for details.

Table 55 ADDR=0x02C: Error Injection

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused		Inject Errors	FSB/Data Errors	Error Stream 4	Error Stream 3	Error Stream 2	Error Stream 1	Error Bit(s)							
Mode	ro		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0		0	0	0	0	0	0	0	0	0	0	0	0	0	0

- **Inject Errors:** **1:** Enables error injection.
  0: Default. Disables error injection.

- **FSB/Data Errors:** **1:** Enables FSB Error Injection into only the first 4 bytes. No errors are injected in the data.
  0: Default. Enables Data Error Injection into only the first data bytes of each selected stream (up to a maximum of 15). Errors will not be injected into FSB.

- **Error Stream 4:** **1:** Enables Stream 4 error injection. Block #4.
  0: Default. Disables Stream 4 error injection.

- **Error Stream 3:** **1:** Enables Stream 3 error injection. Block #3.
  0: Default. Disables Stream 3 error injection.

- **Error Stream 2:** **1:** Enables Stream 2 error injection. Block#2.
  0: Default. Disables Stream 2 error injection.

- **Error Stream 1:** **1:** Enables Stream 1 error injection. Block#1.
  0: Default. Disables Stream 1 error injection.

- **Error Bit(s):** **1:** Enables bit to be corrupted.
  0: Do not corrupt bit.

Table 56 ADDR=0x02D: Data Error Injection

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused												Erred Data Bytes per Block			
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- **Erred Data Bytes per Block: XXXX:** The number of data bytes to be corrupted per 255-byte block. Four 255-byte FEC blocks are interleaved to form one 1020-byte FEC frame. Each of the four streams carries a 255-byte block and the stream selection determines which blocks the errors will occur in. The maximum number of erred bytes per block is 15.

- The maximum number of erred bytes per each 1020-byte FEC frame is 60. That is 15 erred bytes per stream with 4 streams selected and data error injection enabled. If FSB Error Injection was enabled instead of Data Error Injection you would only have 4 erred bytes per each 1020-byte FEC frame.

3.7.6 Register Map Details: Forward Error Correcting (FEC) Performance Monitoring Counts

- All PM counts are read-only and default to zero.
- All are updated on the 1 second tick. If there is no tick, the register value will not change.
- The "tick" is either the rising edge of PM_CLK or the change from 0 to 1 in bit 15 of register 000h, depending on which mode is enabled by the Micro Present byte and bit 1 of the Global Control register, address 001h.
- If the tick is running, the first read of this register may not result in the default value of zero since PMs may have arrived between the time that the chip was reset with the default value and the time that the register was read.

Table 57 ADDR=0x030-0x031: Corrected Ones Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused				MSB											
	LSB															

- Contains the number of ones that were corrected by the FEC block.

Table 58 ADDR=0x032-0x033: Corrected Zeros Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused				MSB											
	LSB															

- Contains the number of zeros that were corrected by the FEC block

Table 59 ADDR=0x034-0x035 Total Corrected Bits Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused			MSB												
	LSB															

- Contains the total number of bits that were corrected by the FEC block.

Table 60 ADDR=0x036-0x037: Total Corrected Bytes Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused							MSB								
	LSB															

- Contains the total number of bytes that were corrected by the FEC block.

Table 61 ADDR=0x038-0x039: Uncorrectable 255-Byte Block Count

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused									MSB						
	LSB															

- Contains the total number of uncorrectable bytes that were detected by the FEC block.

3.7.7 Register Map Details: Special Clock-Independent Registers

These registers can be accessed even when the TX input clock has completely failed. Accesses to any other register during a clock failure will cause a bus error.

There are two types of interrupts shown below: The clock and FIFO interrupts, which only activate when an error condition occurs and the OOF interrupt which activates both when the error condition starts and when it ends, i.e., upon "change of state". In the latter case, the user needs to know what the current state of the error is as well as the fact that it changed. That information is provided in the read-only "current state" bit. In all cases, '1' means that the interrupt or the condition is present. Thus, if the FIFO interrupt bit is '1', a FIFO error has occurred, if the OOF change of state interrupt is a '1', the OOF condition has either started or ended, if the current state of OOF is now a '1', there is an Out-Of-Frame error.

Table 62 ADDR=0x070: Special Interrupt Enables

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												FEC OOF Ion	FIFO Ion	RX Clock Ion	TX Clock Ion	Enable Intr Pin
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0

Ion = Interrupt ON = Enable Interrupt

- **FEC OOF Ion:** **1:** Default. Enable interrupt for a change of state of the FEC decode out of sync.
  0: Disable interrupt.
- **FIFO Ion:** **1:** Default. Enable interrupt for FIFO re-centering.
  0: Disable interrupt.
- **RX Clock Ion*****:** **1:** Default. Enable Special Clock Fail interrupt for a failed RX input clock (CLKINP/N).
  0: Disable interrupt.
- **TX Clock Ion*****:** **1:** Default. Enable Special Clock Fail interrupt for a failed TX input clock (TXCLKP/N).
  0: Disable interrupt.
- **Enable Intr Pin:** **1:** Enables interrupt indications on the global output interrupt pin, PINT.
  0: Default. Disables interrupt indications on the global output interrupt pin, PINT.

***** The RX and TX Clock Interrupts are also located in register 0x10 Clock and APS Failures. Each location has separate Interrupt Enables so please verify that the proper enables are setup for all interrupts. The interrupts for both RX Clock Ion and TX Clock Ion are contained in register 0x071 Special Interrupt Regester.

Table 63 ADDR=0x071: Special Interrupt Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	unused										FEC OOF state	FEC OOF Intr	FIFO Intr	RX Clock Intr	TX Clock Intr	Reset Occurred
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	rc	rc	rc	rc	rc
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE: The first read of this register may not result in the default value since states may have changed and interrupts may have arrived between the time that the chip was reset with the default value and the time that the register was read.

- **FEC OOF State:** **1:** FEC is out-of-sync.
  0: FEC is NOT out-of-sync.
- **FEC OOF Intr:** **1:** Interrupt present: Change of state of FEC decode out of sync.
  0: No interrupt present.
- **FIFO Intr:** **1:** Interrupt present: FIFO re-centering.
  0:. No interrupt present.
- **RX Clock Intr†††††:** **1:** Special Clock Fail interrupt present: RX input clock (CLKINP/N) failed.
  0: No Special Clock Fail interrupt present.
- **TX Clock Intr†††††:** **1:** Special Clock Fail interrupt present: TX input clock (TXCLKP/N) failed.
  0: No Special Clock Fail interrupt present.
- **Reset Occurred:** **1:** The S3062 has been issued a software reset.
  0: No S3062 reset has occurred.

††††† The RX and TX Clock Interrupts are also located in register 0x10 Clock and APS Failures. Each location has separate Interrupt Enables so please verify that the proper enables are setup for all interrupts. The enables for both RX Clock Intr and TX Clock Intr are contained in register 0x070 Special Interrupt Enables.

3.7.8 Register Map Details: Section Trace Memories

Table 64 ADDR=0x080-0x09F: Expected Section Trace Message

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
080 **081** **...** **09f**	First byte of message Third byte of message ... 63rd byte of message								Second byte of message fourth byte of message ... 64th byte of message							
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- Contains the expected section trace message that was programmed via software.

Table 65 ADDR=0x0A0-0x0BF: Received Section Trace Message

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0a0 **0a1** **...** **0bf**	First byte of message Third byte of message ... 63rd byte of message								Second byte of message fourth byte of message ... 64th byte of message							
Mode	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- If there is a mismatch interrupt showing, this memory will contain the mismatched message.
- If there are no errors showing, this memory will show the expected message (unless a power-up reset has just occurred).
- If there is an inconsistent interrupt showing, this memory will contain the last valid message, or, if no valid messages have been received since the last reset, random data.

Table 66 ADDR=0x0C0-0x0DF: Transmit Section Trace Message

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0c0 **0c1** **...** **0df**	First byte of message Third byte of message ... 63rd byte of message								Second byte of message fourth byte of message ... 64th byte of message							
Mode	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- Contains the section trace message to be transmitted that was programmed via software.

3.7.9 Register Map Details: Overhead Memories (RX_OH and TX_OH)

3.7.9.1 Receive Overhead Memory (RX_OH) Notes

- Mode: ro (read only)
- Default value: After a power-up reset, and until two FPOUTB frame pulses have been asserted, this memory will contain random data.
- After the first 2 FPOUTB frame pulses, the locations in memory will contain the previous frame's overhead bytes. They will change to the next frame's values when the frame pulse is asserted.
- The whole of the address range from 100h to 3FFh can be read, but only those addresses defined below will ever have valid data in them.
- The STS-Ns are stored as they are received and the S3062 labels the STN-N locations in numerical order 1,2,3,….
- The 'undefined' locations may be read or written but their functions are not defined by the SONET/SDH standards.
- The 'x' placeholders represent locations that do not map to a valid SONET/SDH byte location.

3.7.9.2 Transmit Overhead Memory (TX_OH) Notes

- Mode: rw (read/write)
- Default value: After a power-up reset this memory will contain random data.
- If the TAC control bit for a particular byte is set, the byte can be written from the processor.
- If the OIC control bit is set, the byte will be inserted into the next frame.
- The whole of the address range from 400h to 6FFh can be accessed, but only those locations defined below will be inserted into the data stream.
- The number of STS's are in the order received, not as defined in ANSI T1.105-1995.
- The 'undefined' locations may be read or written but their functions are not defined by the SONET/SDH standards.
- The 'x' placeholders represent locations that do not map to a valid SONET/SDH byte location.

Table 67 ADDR=0x100-0x387: RX_OH_OR ADDR=0x400-0x687: TX_OH STS-48/STM-16 Memory

Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_OH Addr	**TX_OH Addr**	**Name**								**Name**							
100	400	A1#1								A1#2							
101	401	A1#3								A1#4							
...	...	...								...							
117	417	A1#47								A1#48							
118	418	A2#1								A2#2							
119	419	A2#3								A2#4							
...	...	...								...							
12f	42f	A2#47								A2#48							
130	430	J0								Z0							
131	431	Z0								Z0							
...	...	...								...							
147	447	Z0								Z0							
148	448	B1								undefined							
149	449	undefined								undefined							
...	...	...								...							
15f	45f	undefined								undefined							
160	460	E1								undefined							
161	461	undefined								undefined							
...	...	...								...							
177	477	undefined								undefined							
178	478	F1								undefined							
179	479	undefined								undefined							
...	...	...								...							
18f	48f	undefined								undefined							
190	490	D1								undefined							
191	491	undefined								undefined							
...	...	...								...							
1a7	4a7	undefined								undefined							
1a8	4a8	D2								undefined							
1a9	4a9	undefined								undefined							
...	...	...								...							
1bf	4bf	undefined								undefined							
1c0	4c0	D3								undefined							
1c1	4c1	undefined								undefined							
...	...	...								...							
1d7	4d7	undefined								undefined							
1d8	4d8	H1#1								H1#2							
1d9	4d9	H1#3								H1#4							
...	...	...								...							
1ef	4ef	H1#47								H1#48							
1f0	4f0	H2#1								H2#2							
1f1	4f1	H2#3								H2#4							
...	...	...								...							
207	507	H2#47								H2#48							
208	508	H3#1								H3#2							
209	509	H3#3								H3#4							
...	...	...								...							
21f	51f	H3#47								H3#48							
220	520	B2#1								B2#2							
221	521	B2#3								B2#4							
...	...	...								...							
237	537	B2#47								B2#48							
238	538	K1								undefined							
239	539	undefined								undefined							
...	...	...								...							
24f	54f	undefined								undefined							
250	550	K2								undefined							
251	551	undefined								undefined							

Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_OH Addr	**TX_OH Addr**	**Name**								**Name**							
...	...	...								...							
267	567	undefined								undefined							
268	568	D4								undefined							
269	569	undefined								undefined							
...	...	...								...							
27f	57f	undefined								undefined							
280	580	D5								undefined							
281	581	undefined								undefined							
...	...	...								...							
297	597	undefined								undefined							
298	598	D6								undefined							
29a	59a	undefined								undefined							
...	...	...								...							
2af	5af	undefined								undefined							
2b0	5b0	D7								undefined							
2b1	5b1	undefined								undefined							
...	...	...								...							
2c7	5c7	undefined								undefined							
2c8	5c8	D8								undefined							
2c9	5c9	undefined								undefined							
...	...	...								...							
2df	5df	undefined								undefined							
2e0	5e0	D9								undefined							
2e1	5e1	undefined								undefined							
...	...	...								...							
2f7	5f7	undefined								undefined							
2f8	5f8	D10								undefined							
2f9	5f9	undefined								undefined							
...	...	...								...							
30f	60f	undefined								undefined							
310	610	D11								undefined							
311	611	undefined								undefined							
...	...	...								...							
327	627	undefined								undefined							
328	628	D12								undefined							
329	629	undefined								undefined							
...	...	...								...							
33f	63f	undefined								undefined							
340	640	S1								Z1							
341	641	Z1								Z1							
...	...	...								...							
357	657	Z1								Z1							
358	658	Z2								Z2							
359	659	M1								Z2							
360	660	Z2								Z2							
...	...	...								...							
36f	66f	Z2								Z2							
370	670	E2								undefined							
371	671	undefined								undefined							
...	...	...								...							
387	687	undefined								undefined							

Table 68 ADDR=0x100-0x1a1: RX_OH_OR ADDR=0x400-0x4a1: TX_OH STS-12/STM-4 Memory

Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_OH Addr	**TX_OH Addr**	**Name**								**Name**							
100	400	A1#1								A1#2							
101	401	A1#3								A1#4							
...	...	...								...							
105	405	A1#11								A1#12							
106	406	A2#1								A2#2							
107	407	A2#3								A2#4							
...	...	...								...							
10b	40b	A2#11								A2#12							
10c	40c	J0								Z0							
10d	40d	Z0								Z0							
...	...	...								...							
111	411	Z0								Z0							
112	412	B1								undefined							
113	413	undefined								undefined							
...	...	...								...							
117	417	undefined								undefined							
118	418	E1								undefined							
119	419	undefined								undefined							
...	...	...								...							
11d	41d	undefined								undefined							
11e	41e	F1								undefined							
11f	41f	undefined								undefined							
...	...	...								...							
123	423	undefined								undefined							
124	424	D1								undefined							
125	425	undefined								undefined							
...	...	...								...							
129	429	undefined								undefined							
12a	42a	D2								undefined							
12b	42b	undefined								undefined							
...	...	...								...							
12f	42f	undefined								undefined							
130	430	D3								undefined							
131	431	undefined								undefined							
...	...	...								...							
135	435	undefined								undefined							
136	436	H1#1								H1#2							
137	437	H1#3								H1#4							
...	...	...								...							
13b	43b	H1#11								H1#12							
13c	43c	H2#1								H2#2							
13d	43d	H2#3								H2#4							
...	...	...								...							
141	441	H2#11								H2#12							
142	442	H3#1								H3#2							
143	443	H3#3								H3#4							
...	...	...								...							
147	447	H3#11								H3#12							
148	448	B2#1								B2#2							
149	449	B2#3								B2#4							
...	...	...								...							
14d	44d	B2#11								B2#12							
14e	44e	K1								undefined							
14f	44f	undefined								undefined							
...	...	...								...							
153	453	undefined								undefined							
154	454	K2								undefined							

Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_OH Addr	**TX_OH Addr**	**Name**								**Name**							
155	455	undefined								undefined							
...	...	...								...							
159	459	undefined								undefined							
15a	45a	D4								undefined							
15b	45b	undefined								undefined							
...	...	...								...							
15f	45f	undefined								undefined							
160	460	D5								undefined							
161	461	undefined								undefined							
...	...	...								...							
165	465	undefined								undefined							
166	466	D6								undefined							
167	467	undefined								undefined							
...	...	...								...							
16b	46b	undefined								undefined							
16c	46c	D7								undefined							
16d	46d	undefined								undefined							
...	...	...								...							
171	471	undefined								undefined							
172	472	D8								undefined							
173	473	undefined								undefined							
...	...	...								...							
177	477	undefined								undefined							
178	478	D9								undefined							
179	479	undefined								undefined							
...	...	...								...							
17d	47d	undefined								undefined							
17e	47e	D10								undefined							
17f	47f	undefined								undefined							
...	...	...								...							
183	483	undefined								undefined							
184	484	D11								undefined							
185	485	undefined								undefined							
...	...	...								...							
189	489	undefined								undefined							
18a	48a	D12								undefined							
18b	48b	undefined								undefined							
...	...	...								...							
18f	48f	undefined								undefined							
190	490	S1								Z1							
191	491	Z1								Z1							
...	...	...								...							
195	495	Z1								Z1							
196	496	Z2								Z2							
197	497	M1								Z2							
198	498	Z2								Z2							
...	...	...								...							
19b	49b	Z2								Z2							
19c	49c	E2								undefined							
19d	49d	undefined								undefined							
...	...	...								...							
1a1	4a1	undefined								undefined							

Table 69 ADDR=0x100-0x135: RX_OH_OR ADDR=0x400-0x435: TX_OH STS-3/STM-1 Memory

Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_OH Addr	**TX_OH Addr**	**Name**								**Name**							
100	400	A1#1								A1#2							
101	401	A1#3								x							
102	402	A2#1								A2#2							
103	403	A2#3								x							
104	404	J0								Z0							
105	405	Z0								x							
106	406	B1								undefined							
107	407	undefined								x							
108	408	E1								undefined							
109	409	undefined								x							
10a	40a	F1								undefined							
10b	40b	undefined								x							
10c	40c	D1								undefined							
10d	40d	undefined								x							
10e	40e	D2								undefined							
10f	40f	undefined								x							
110	410	D3								undefined							
111	411	undefined								x							
112	412	H1#1								H1#2							
113	413	H1#3								x							
114	414	H2#1								H2#2							
115	415	H2#3								x							
116	416	H3#1								H3#2							
117	417	H3#3								x							
118	418	B2#1								B2#2							
119	419	B2#3								x							
11a	41a	K1								undefined							
11b	41b	undefined								x							
11c	41c	K2								undefined							
11d	41d	undefined								x							
11e	41e	D4								undefined							
11f	41f	undefined								x							
120	420	D5								undefined							
121	421	undefined								x							
122	422	D6								undefined							
123	423	undefined								x							
124	424	D7								undefined							
125	425	undefined								x							
126	426	D8								undefined							
127	427	undefined								x							
128	428	D9								undefined							
129	429	undefined								x							
12a	42a	D10								undefined							
12b	42b	undefined								x							
12c	42c	D11								undefined							
12d	42d	undefined								x							
12e	42e	D12								undefined							
12f	42f	undefined								x							
130	430	S1								Z1							
131	431	Z1								x							
132	432	Z2								Z2							
133	433	M1								x							

Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RX_OH Addr	**TX_OH Addr**	**Name**								**Name**							
134	434	E2								undefined							
135	435	undefined								x							

- The ‘undefined’ locations may be read or written but their functions are not defined by the SONET/SDH standards.
- The ‘x’ placeholders represent locations that do not map to a valid SONET/SDH byte location.

3.7.10 Register Map Details: Overhead Insert and Transmit Access Control Memories (OIC and TAC)

3.7.10.1 OIC NOTES

- Mode: rw (read/write)
- Default value: After a power-up reset this memory will contain random data.
- The bits in the OIC memory have no effect if (a) the Micro Present byte is not active and the MEMOH signal is inactive or if (b) the processor is activated and the 'Insert OH' register bit is de-asserted.
- All bits from 700h to 77Fh can be accessed, only those defined below are used.
- Each bit controls the insertion of one of the overhead bytes from the transmit overhead memory (TX_OH) into the data stream. The bits are ordered exactly the same as the bytes are, from the most significant bit of the first address to the least significant bit of the last address. Thus, if address 700h bit 15 is '1', the transmitted STS-1 #1's A1 will be replaced with the A1#1 value stored in TX_OH. If Address 700h bit 14 is '1', the transmitted STS-1 #2's A1 will be replaced with the A1#2 value stored in TX_OH, etc.
- The 'undefined' locations may be read or written but their functions are not defined by the SONET/SDH standards.
- The 'x' placeholders represent locations that do not map to a valid SONET/SDH byte location.

3.7.10.2 TAC NOTES

- Mode: rw (read/write)
- Default value: After a power-up reset this memory will contain random data.
- The bits in the TAC memory have no effect if the Micro Present byte is not active.
- All bits from 780h to 7FFh can be accessed.
- Each bit controls whether the FPGA is prevented from writing to a byte within the transmit overhead memory (TX_OH). A '1' disables the FPGA write. The bits are ordered exactly the same as the bytes are -- from the most significant bit of the first address to the least significant bit of the last address. Thus, if address 780h bit 15 is '1', the FPGA is prevented from writing into the A1#1 byte in TX_OH. If Address 780h bit 14 is '1' the FPGA is prevented from writing into the A1#2 byte in TX_OH, etc.
- The 'undefined' locations may be read or written but their functions are not defined by the SONET/SDH standards.
- The 'x' placeholders represent locations that do not map to a valid SONET/SDH byte location.

3.7.10.3 Memory Maps for the 3 STS/STM Modes

Table 70 ADDR=0x700-0x750: OIC OR ADDR=0x780-0x7D0: TAC STS-48/STM-16 Memory

Address		Bit															
OIC	TAC	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
700	780	A1#1	A1#2	A1#3	A1#4	A1#5	A1#6	A1#7	A1#8	A1#9	A1#10	A1#11	A1#12	A1#13	A1#14	A1#15	A1#16
701	781	A1#17	A1#18	A1#19	A1#20	A1#21	A1#22	A1#23	A1#24	A1#25	A1#26	A1#27	A1#28	A1#29	A1#30	A1#31	A1#32
702	782	A1#33	A1#34	A1#35	A1#36	A1#37	A1#38	A1#39	A1#40	A1#41	A1#42	A1#43	A1#44	A1#45	A1#46	A1#47	A1#48
703	783	A2#1	A2#2	A2#3	A2#4	A2#5	A2#6	A2#7	A2#8	A2#9	A2#10	A2#11	A2#12	A2#13	A2#14	A2#15	A2#16
704	784	A2#17	A2#18	A2#19	A2#20	A2#21	A2#22	A2#23	A2#24	A2#25	A2#26	A2#27	A2#28	A2#29	A2#30	A2#31	A2#32
705	785	A2#33	A2#34	A2#35	A2#36	A2#37	A2#38	A2#39	A2#40	A2#41	A2#42	A2#43	A2#44	A2#45	A2#46	A2#47	A2#48
706	786	J0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0
707	787	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0
708	788	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0	Z0
709	789	B1	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
70a	78a	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
70b	78b	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
70c	78c	E1	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
70d	78d	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
70e	78e	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
70f	78f	F1	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
710	790	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
711	791	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
712	792	D1	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
713	793	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef

Address		Bit															
OIC	TAC	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
714	794	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
715	795	D2	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
716	796	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
717	797	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
718	798	D3	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
719	799	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
71a	79a	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
71b	79b	H1#1	H1#2	H1#3	H1#4	H1#5	H1#6	H1#7	H1#8	H1#9	H1#10	H1#11	H1#12	H1#13	H1#14	H1#15	H1#16
71c	79c	H1#17	H1#18	H1#19	H1#20	H1#21	H1#22	H1#23	H1#24	H1#25	H1#26	H1#27	H1#28	H1#29	H1#30	H1#31	H1#32
71d	79d	H1#33	H1#34	H1#35	H1#36	H1#37	H1#38	H1#39	H1#40	H1#41	H1#42	H1#43	H1#44	H1#45	H1#46	H1#47	H1#48
71e	79e	H2#1	H2#2	H2#3	H2#4	H2#5	H2#6	H2#7	H2#8	H2#9	H2#10	H2#11	H2#12	H2#13	H2#14	H2#15	H2#16
71f	79f	H2#17	H2#18	H2#19	H2#20	H2#21	H2#22	H2#23	H2#24	H2#25	H2#26	H2#27	H2#28	H2#29	H2#30	H2#31	H2#32
720	7a0	H2#33	H2#34	H2#35	H2#36	H2#37	H2#38	H2#39	H2#40	H2#41	H2#42	H2#43	H2#44	H2#45	H2#46	H2#47	H2#48
721	7a1	H3#1	H3#2	H3#3	H3#4	H3#5	H3#6	H3#7	H3#8	H3#9	H3#10	H3#11	H3#12	H3#13	H3#14	H3#15	H3#16
722	7a2	H3#17	H3#18	H3#19	H3#20	H3#21	H3#22	H3#23	H3#24	H3#25	H3#26	H3#27	H3#28	H3#29	H3#30	H3#31	H3#32
723	7a3	H3#33	H3#34	H3#35	H3#36	H3#37	H3#38	H3#39	H3#40	H3#41	H3#42	H3#43	H3#44	H3#45	H3#46	H3#47	H3#48
724	7a4	B2#1	B2#2	B2#3	B2#4	B2#5	B2#6	B2#7	B2#8	B2#9	B2#10	B2#11	B2#12	B2#13	B2#14	B2#15	B2#16
725	7a5	B2#17	B2#18	B2#19	B2#20	B2#21	B2#22	B2#23	B2#24	B2#25	B2#26	B2#27	B2#28	B2#29	B2#30	B2#31	B2#32
726	7a6	B2#33	B2#34	B2#35	B2#36	B2#37	B2#38	B2#39	B2#40	B2#41	B2#42	B2#43	B2#44	B2#45	B2#46	B2#47	B2#48
727	7a7	K1	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
728	7a8	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
729	7a9	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
72a	7aa	K2	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
72b	7ab	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
72c	7ac	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
72d	7ad	D4	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
72e	7ae	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
72f	7af	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
730	7b0	D5	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
731	7b1	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
732	7b2	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
733	7b3	D6	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
734	7b4	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
735	7b5	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
736	7b6	D7	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
737	7b7	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
738	7b8	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
739	7b9	D8	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
73a	7ba	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
73b	7bb	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
73c	7bc	D9	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
73d	7bd	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
73e	7be	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
73f	7bf	D10	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
740	7c0	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
741	7c1	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
742	7c2	D11	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
743	7c3	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
744	7c4	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
745	7c5	D12	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
746	7c6	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
747	7c7	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
748	7c8	S1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1
749	7c9	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1
74a	7ca	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1
74b	7cb	Z2	Z2	M1	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2
74c	7cc	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2
74d	7cd	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2
74e	7ce	E2	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
74f	7cf	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
750	7d0	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef

Table 71 ADDR=0x700-0x714: OIC OR ADDR=0x780-0x794: TAC STS-12/STM-4 Memory

Address		Bit															
OIC	**TAC**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
700	780	A1#1	A1#2	A1#3	A1#4	A1#5	A1#6	A1#7	A1#8	A1#9	A1#10	A1#11	A1#12	A2#1	A2#2	A2#3	A2#4
701	781	A2#5	A2#6	A2#7	A2#8	A2#9	A2#10	A2#11	A2#12	J0	Z0	Z0	Z0	Z0	Z0	Z0	Z0
702	782	Z0	Z0	Z0	Z0	B1	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
703	783	E1	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	F1	undef	undef	undef
704	784	undef	undef	undef	undef	undef	undef	undef	undef	D1	undef	undef	undef	undef	undef	undef	undef
705	785	undef	undef	undef	undef	D2	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
706	786	D3	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	H1#1	H1#2	H1#3	H1#4
707	787	H1#5	H1#6	H1#7	H1#8	H1#9	H1#10	H1#11	H1#12	H2#1	H2#2	H2#3	H2#4	H2#5	H2#6	H2#7	H2#8
708	788	H2#9	H2#10	H2#11	H2#12	H3#1	H3#2	H3#3	H3#4	H3#5	H3#6	H3#7	H3#8	H3#9	H3#10	H3#11	H3#12
709	789	B2#1	B2#2	B2#3	B2#4	B2#5	B2#6	B2#7	B2#8	B2#9	B2#10	B2#11	B2#12	K1	undef	undef	undef
70a	78a	undef	undef	undef	undef	undef	undef	undef	undef	K2	undef	undef	undef	undef	undef	undef	undef
70b	78b	undef	undef	undef	undef	D4	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
70c	78c	D5	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	D6	undef	undef	undef
70d	78d	undef	undef	undef	undef	undef	undef	undef	undef	D7	undef	undef	undef	undef	undef	undef	undef
70e	78e	undef	undef	undef	undef	D8	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
70f	78f	D9	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	D10	undef	undef	undef
710	790	undef	undef	undef	undef	undef	undef	undef	undef	D11	undef	undef	undef	undef	undef	undef	undef
711	791	undef	undef	undef	undef	D12	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef	undef
712	792	S1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z2	Z2	M1	Z2
713	793	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	E2	undef	undef	undef	undef	undef	undef	undef
714	794	undef	undef	undef	undef	x	x	x	x	x	x	x	x	x	x	x	x

Table 72 ADDR=0x700-0x706: OIC OR ADDR=0x780-0x786: TAC STS-3/STM-1 Memory

Address		Bit															
OIC	**TAC**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
700	780	A1#1	A1#2	A1#3	x	A2#1	A2#2	A2#3	x	J0	Z0	Z0	x	B1	undef	undef	x
701	781	E1	undef	undef	x	F1	undef	undef	x	D1	undef	undef	x	D2	undef	undef	x
702	782	D3	undef	undef	x	H1#1	H1#2	H1#3	x	H2#1	H2#2	H2#3	x	H3#1	H3#2	H3#3	x
703	783	B2#1	B2#2	B2#3	x	K1	undef	undef	x	K2	undef	undef	x	D4	undef	undef	x
704	784	D5	undef	undef	x	D6	undef	undef	x	D7	undef	undef	x	D8	undef	undef	x
705	785	D9	undef	undef	x	D10	undef	undef	x	D11	undef	undef	x	D12	undef	undef	x
706	786	S1	Z1	Z1	x	Z2	Z2	M1	x	E2	undef	undef	x	x	x	x	x

- The ‘undefined’ locations may be read or written but their functions are not defined by the SONET/SDH standards.
- The ‘x’ placeholders represent locations that do not map to a valid SONET/SDH byte location.

4 S3062 PIN DESCRIPTIONS

Note that all outputs default to a steady state on reset. Where an output has an active and an inactive mode defined, it will default to the inactive state.

Table 73 Receive Physical Media Interface

Name	Level	I/O	Ball #	Description	Shared Pin
CLKINP CLKINN	LVPECL, Differential	I	L26 M24	RX clock input. A High speed clock, to which DATAIN[15:0] is aligned. CLKINP/N is used to transfer the data on the DATAIN[15:0] inputs into a holding register. The rising edge of CLKINP/N samples DATAIN[15:0].	
DATAIN[15] DATAIN[14] DATAIN[13] DATAIN[12] DATAIN[11] DATAIN[10] DATAIN[9] DATAIN[8] DATAIN[7] DATAIN[6] DATAIN[5] DATAIN[4] DATAIN[3] DATAIN[2] DATAIN[1] DATAIN[0]	LVPECL, Single Ended	I	F24 E25 F25 E26 F26 H23 G26 H24 K23 J24 K24 J25 L23 K25 K26 L25	RX parallel input data. 16-bit wide word, aligned to the CLKINP/N parallel input clock. DATAIN[15] is the most significant bit (corresponding to bit 1 of each word, the first bit received serially). DATAIN[0] is the least significant bit (corresponding to bit 16 of each word, the last bit received serially). DATAIN is sampled on the rising edge of CLKINP/N.	
PECLREF	REF Voltage		D20	PECL reference input. Reference voltage for the LVPECL inputs from the AMCC DeMUX.	

Table 74 Transmit Physical Media Interface

Name	Level	I/O	Ball #	Description	Shared Pin
DATAOUT[15] DATAOUT[14] DATAOUT[13] DATAOUT[12] DATAOUT[11] DATAOUT[10] DATAOUT[9] DATAOUT[8] DATAOUT[7] DATOUT[6] DATAOUT[5] DATAOUT[4] DATAOUT[3] DATAOUT[2] DATAOUT[1] DATAOUT[0]	LVPECL, Single Ended	O	E3 E2 G4 G3 H2 K4 K3 L4 L3 M3 M1 N2 T1 P3 T3 T2	TX parallel output data. 16-bit wide word, aligned to the CLKOUTP/N parallel output clock. DATAOUT[15] is the most significant bit (corresponding to bit 1 of each word, the first bit transmitted serially). DATAOUT[0] is the least significant bit (corresponding to bit 16 of each word, the last bit transmitted serially). DATAOUT is transmitted on the rising edge of the CLKOUTP/N.	
CLKOUTP CLKOUTN	LVPECL, Differential	O	V1 T4	TX clock output. A high speed clock, to which DATAOUT[15:0] is aligned. Nominally 50% duty cycle. The rising clock edge of CLKOUTP/N transmits the DATAOUT[15:0].	
TXCLKP TXCLKN	LVPECL, Differential	I	M26 N23	TX clock input. A high speed clock, to which the S3062 FIFO read address is aligned. It is used to re-time the S3062's 32-bit internal data path to the transmit clock domain. This clock is sourced from the transmit MUX and should be generated from the receive clock to minimize drift between the S3062's CLKIN and TXCLK.	
FPOUTB	LVTTL	O	U4	Frame pulse output. Active low output. FPOUTB is updated on the rising edge of CLKOUTP When active this signal indicates SONET/SDH frame boundaries within the chip -- indicating that another frame of overhead can be read from or written to the RX_OH and TX_OH memories. The pulse is 154ns long in OC-12 and OC-48 modes and 102.5-205ns in OC-3 mode. It occurs 6 CLKOUTP ticks before the A1 bytes are output on DATAOUT. If FEC encode is ON, the A1 bytes will be delayed from FPOUTB by another 2 to 66 CLKOUTP ticks. FPOUTB will continue to pulse every 125µs even when LOS, OOF or LOF is received. It will shift to the new frame boundary when the framer moves from OOF to in-frame.	

Table 75 Control Pins

Name	Level	I/O	Ball #	Description	Shared Pin
PASSTHRU	LVTTL	I	W25	Pass-Through mode select. Active high input. When active, the DATAIN[15:0] and CLKINP/N inputs pass through the FIFO where they are re-timed to the transmitter clock domain (TXCLK) and output on the DATAOUT[15:0] pins. In Pass-Through mode, the SONET and GBE monitors are turned OFF. If the processor interface is activated by loading the Micro Present byte with a value of 59h, this input will have no effect and control will be transferred to the 'Pass Thru' register bit. This signal is static and must not be changed in normal operation.	
RATESEL[1] RATESEL[0]	LVTTL	I	AB25 AC26	Rate select input. These signals select the data rate. When any of the STS rates are selected, the STS monitors will be turned on and the Gigabit monitors will be powered OFF, in order to minimize device power dissipation. Conversely, when the Gigabit Ethernet rate is selected, the Gigabit monitors will be on and the STS monitors will be powered OFF. If the processor interface is activated by loading the Micro Present byte with a value of 59h, these inputs will have no effect and control will be transferred to the Rate Select register bits. RATESEL[1] RATESEL[0] S3062 RATE 0 0 STS-3/STM-1 0 1 STS-12/STM-4 1 0 STS-48/STM-16 1 1 Gigabit Ethernet These signals are static and must not be changed in normal operation. If the user wishes to change the S3062 rate on the fly through software, the RATESEL pins should be wired to the HIGHEST data rate that the chip will encounter. The reason for this is that if RATESEL is wired to a lower rate, you will have slower clocks propagating throughout the chip when/while the input clocks/data are set to a higher rate.	
PM_CLK	LVTTL	I	AB1	Performance Monitor clock input. This low frequency clock (typically one second) is used to accumulate section, and line performance monitoring statistics. The rising edge of the clock signals the end of one period, and the start of the next. Performance Monitoring counts are transferred to the PM count registers within 10 processor clocks of the rising edge. If the processor interface is activated by loading the Micro Present byte with a value of 59h, and the software tick function has been selected, this input will have no effect and control will be transferred to the PM Tick register bit.	
RESETB	LVTTL	I	AF8	Hardware reset input. Active low input. Asynchronous reset input for the device. If the processor interface is activated by loading the Micro Present byte with a value of 59h, the inverse of this input will be ORed with the Force Reset register bit.	

Table 76 SONET/SDH Control Pins

Name	Level	I/O	Ball #	Description	Shared Pin
FPGASEL	LVTTL	I	W24	FPGA mode select input. Active high input. When active, the 21 shared pins described in the shared pin sections below will be in FPGA mode providing all the overhead bytes on I/O pins for an FPGA to connect to the S3062. When inactive, the shared pins will be in Orderwire/DCC mode providing serial access to the orderwire bytes and the data communication channel bytes. This signal is static and must not be changed in normal operation.	
MEMOH	LVTTL	I	Y25	Inserts into overhead from OIC specified memory locations. Active high input. When active, the select bits in the Overhead Insert Control memory are used to determine which bytes from the memory will be inserted into the outgoing data stream. When inactive, no overhead bytes from the memory will be inserted. If the processor interface is activated by loading the Micro Present byte with a value of 59h, this input will have no effect and control will be transferred to the 'Insert OH' register bit.	
FIXSOH	LVTTL	I	W26	Fixes the transmit section overhead. Active high input. When active, the A1 and A2 bytes will be forced to F6h and 28h respectively, and the B1 byte will be recalculated. Insertion of any section, and line overhead bytes from the Transmit Overhead Memory will force B1 to be recalculated even if this input is inactive. Insertion of any of the bytes of overhead from the Transmit Overhead Memory takes precedence over the function of this signal. It is possible for the user to write incorrect values for the A1, A2, or B1 bytes into the memory, and have these incorrect values inserted into the transmit data. If the processor interface is activated by loading the Micro Present byte with a value of 59h this input will have no effect and control will be transferred to the 'Don't Fix SOH' register bit.	
SCRBEN	LVTTL	I/O	R26	Enable for the scrambler. Active high input (or output FEC signal when Micro Present byte is loaded with a value of 59h). This pin is configured as an input when the Micro Present byte is not active. When active, the frame synchronous scrambler is enabled. If the processor interface is activated by loading the Micro Present byte with a value of 59h, the user must use the 'Scrmbl OFF' register bit for scrambler control because this pin will become an output controlled by the FEC function (RX_FEC_DLCK).	RX_FEC_DLCK
DESCRBEN	LVTTL	I/O	P24	Enable for the descrambler. Active high input (or output FEC signal when Micro Present byte is loaded with a value of 59h). This pin is configured as an input when the Micro Present byte is not active. When active, the frame synchronous descrambler is enabled. If the processor interface is activated by loading the Micro Present byte with a value of 59h, the user must use the 'Descr OFF' register bit for descrambler control because this pin becomes an output controlled by the FEC function (RX_FEC_DL).	RX_FEC_DL

Name	Level	I/O	Ball #	Description	Shared Pin
FIXB2	LVTTL	I	V25	Fixes the transmitted B2 byte. Active high input. When active, normal operation occurs (B2 calculations and insertions are enabled). When in-active the B2 byte calculations and insertions are disabled. Inserting any bytes, other than section overhead, from the memory will force B2 to be recalculated even if this input is inactive. If the processor interface is activated by loading the Micro Present byte with a value of 59h, this input will have no effect and control will be transferred to the 'FIXB2' register bit.	
BLOCKBIP	LVTTL	I/O	W3	Calculate only Block BIP Errors. Active high input (or output FEC signal when the Micro Present byte is loaded with a value of 59h). This pin is configured as an input when the Micro Present byte is not active. When active, a BIP byte with an error in it is counted as 1 error regardless of how many bits were incorrect. When inactive, each bit, which is incorrect in a BIP byte, is counted as an error (up to 8 errors possible in a byte). This applies to both B1 and B2 bytes. If the processor interface is activated by loading the Micro Present byte with a value of 59h, the user must use the Block B1 and B2 enable register bits because this pin becomes an output controlled by the FEC function (TX_FEC_DLCK).	TX_FEC_DLCK
XORBIP	LVTTL	I	V3	XOR B1 and B2 with overhead insertion bytes. Active high input. This pin is only relevant if B1 and/or B2 bytes are enabled for insertion into the output data stream from the TX_OH memory. When active, the values that are stored in the B1 and B2 locations of the TX_OH are XORed with the re-generated B1 and B2 values. When inactive, the stored B1 and B2s are inserted directly into the B1 and B2 positions. If the processor interface is activated by loading the Micro Present byte with a value of 59h, the user must use the XOR B1 and B2 register bits because this pin becomes an input controlled by the FEC function (TX_FEC_DL).	TX_FEC_DL
AUTOAIS	LVTTL	I	AE9	Automatically inserts line AIS upon LOS or LOF. Active high input. When active, the SONET/SDH block will generate line AIS when LOS or LOF is received and will turn OFF line AIS when LOS or LOF end. (The AIS will be scrambled or not depending on SCRBEN.) If the processor interface is activated by loading the Micro Present byte with a value of 59h, this input will have no effect and control will be transferred to the 'Auto AIS' register bit. Note that an active DATAAIS or an active DATAOFF has priority over an active AUTOAIS.	
DATAAIS	LVTTL	I	AC11	Forces a line AIS regardless of data input. Active high input. When active, the SONET/SDH block is forced to output line AIS instead of the regular SONET/SDH data stream regardless of whether the input stream is in LOS or LOF or not. (The AIS will be scrambled or not depending on SCRBEN.) If the processor interface is activated by loading the Micro Present byte with a value of 59h, this input will have no effect and control will be transferred to the 'Force AIS' register bit. Note that an active DATAOFF has priority over an active DATAAIS.	

Name	Level	I/O	Ball #	Description	Shared Pin
DATAOFF	LVTTL	I	Y4	SONET/SDH block data OFF signal. Active high input. When active, the output of the SONET/SDH block will be forced to all zeros. If the processor interface is activated by loading the Micro Present byte with a value of 59h, this input will have no effect and control will be transferred to the Force LOS register bit. Note that this control signal affects the "output of the SONET/SDH block", not the output of the chip. The FEC and differential encode blocks are after the SONET/SDH block and will affect the data output if enabled. Also, Gigabit Ethernet and Pass-Through modes will be unaffected by the state of this pin or associated register bits.	

- These pins only have an effect if one of the SONET/SDH rates have been selected and if neither RESETB nor PASSTHRU are active.

Table 77 SONET/SDH Status Indicators

Name	Level	I/O	Ball #	Description	Shared Pin
LOS	LVTTL	O	Y3	Loss of Signal indicator. Active high output. When active, LOS indicates that a consecutive zero pattern for a minimum of 26.337us of all zeros is detected on the incoming scrambled STS-N/STM-M signal before descrambling. LOS is deactivated when two valid framing words are detected and no LOS is detected in between. LOS is updated on the rising edge of CLKOUTP. This signal is multiplexed with the Gigabit Ethernet SYNC_LOSS signal pin and is only available when a SONET/SDH mode is selected. See Section 3.3.1.3 for a detailed description of the Frame Check timing.	SYNC_ LOSS
OOF	LVTTL	O	AA2	Out-of-Frame indicator. Active high output. The Out-of-Frame (OOF) signal is active when the S3062 has detected an out-of-frame condition. The OOF is inactive when the S3062 is in-frame. An OOF declaration occurs when four consecutive erred framing patterns are received and clears when 2 consecutive valid frames are received. The OOF is updated on the rising edge of CLKOUTP. This signal is multiplexed with the Gigabit Ethernet INV_CODE signal pin and is only available when a SONET/SDH mode is selected. See Section 3.3.1.3 for a detailed description of the Frame Check timing.	INV_CODE
LOF	LVTTL	O	AC2	Loss of Frame indicator. Active high output. When active, this indicates that the out-of-frame (OOF) condition has persisted for a period of 3 ms. LOF is de-activated when an in-frame condition (as indicated by a low level on the OOF output) persists for a period of 3ms. LOF is updated on the rising edge of CLKOUTP. This signal is multiplexed with the Gigabit Ethernet DISP_ERR signal pin and is only available when a SONET/SDH mode is selected. See Section 3.3.1.3 for a detailed description of the Frame Check timing.	DISP_ERR
B1ERR	LVTTL	O	Y1	B1 parity error indicator. Active high output. Indicates that a B1 bit error has been detected when high for a minimum of 12ns. For each frame B1ERR will pulse a maximum of 8 times. In between pulses (bit errors) the B1ERR will be low for a minimum of 24ns. B1ERR is updated on the rising edge of CLKOUTP.	

Table 78 Gigabit Ethernet Status Indicators

Name	Level	I/O	Ball #	Description	Shared Pin
SYNC_LOSS	LVTTL	O	Y3	Loss of synchronization indicator. Active high output. Indicates that alignment of the incoming 10-bit GBE words have been lost. SYNC_LOSS is updated on the rising edge of CLKOUTP. This signal is multiplexed with the SONET/SDH LOS signal pin and is only available when Gigabit Ethernet is selected. The guaranteed minimum pulse width of this signal is 9ns for a 2.5GBE signal with 8-byte FEC encoding.	LOS
INV_CODE	LVTTL	O	AA2	Invalid 8B/10B code indicator. Active high output. Indicates that an 8B/10B code violation has been detected. INV_CODE is updated on the rising edge of CLKOUTP. This signal is multiplexed with the SONET/SDH OOF signal pin and is only available when Gigabit Ethernet is selected. The guaranteed minimum pulse width of this signal is 9ns for a 2.5GBE signal with 8-byte FEC encoding.	OOF
DISP_ERR	LVTTL	O	AC2	Disparity error indicator. Active high output. Indicates that a running disparity error has been detected. DISP_ERR is updated on the rising edge of CLKOUTP. This signal is multiplexed with the SONET/SDH LOF signal pin and is only available when Gigabit Ethernet is selected. The guaranteed minimum pulse width of this signal is 9ns for a 2.5GBE signal with 8-byte FEC encoding.	LOF

Table 79 Processor Interface (PIF) Signals

Name	Level	I/O	Ball #	Description	Shared Pin
PADD[10] PADD[9] PADD[8] PADD[7] PADD[6] PADD[5] PADD[4] PADD[3] PADD[2] PADD[1] PADD[0]	LVTTL	I	AF15 AE15 AD15 AE14 AD14 AC14 AF11 AD12 AE13 AE10 AD11	Processor address buss input, 11-bits wide. PADD[10] is the most significant bit. PADD[0] is the least significant bit.	
PDAT[15] PDAT[14] PDAT[13] PDAT[12] PDAT[11] PDAT[10] PDAT[9] PDAT[8] PDAT[7] PDAT[6] PDAT[5] PDAT[4] PDAT[3] PDAT[2] PDAT[1] PDAT[0]	LVTTL	I/O	AA24 AF24 AE23 AD22 AE22 AD21 AC20 AD20 AC19 AF21 AF20 AE19 AD18 AE18 AD17 AF18	Processor bi-directional data bus, 16-bits wide. These are normally input pins. They only change to become outputs during the output portion of a valid read cycle. PDAT[15] is the most significant bit. PDAT[0] is the least significant bit.	
PCLK	LVTTL	I	AC15	Processor system clock.	
PCS	LVTTL	I	AD16	Processor chip select. Active low input. When active, this signal indicates that the S3062 is being selected by the processor for a read/write access.	
PRW	LVTTL	I	AE16	Processor Read/Write. A low on this signal indicates that the processor is requesting write access of the S3062. A high indicates that the processor is requesting read access of the S3062.	
PTS	LVTTL	I	AF17	Processor transfer start. Active low input. When active, this signal indicates to the S3062 the	

Name	Level	I/O	Ball #	Description	Shared Pin
				beginning of a processor transaction (read or write of the S3062's memory or registers).	
PBURST	LVTTL	I	AD10	Processor burst transfer. Active low input. When active, this signal indicates to the S3062 that a burst transfer is in progress.	
PBDIP	LVTTL	I	AF9	Processor burst data in progress. Active low input. This signal is used in the processor burst protocol. When active and during a read, this signal indicates a processor request for burst data. When active and during a write, this signal indicates the validation of burst data.	
PTA	LVTTL Tri-State	O	AD7	Processor transfer acknowledge indicator. Active low output. When active, this signal indicates to the processor that data has been received (for a processor write), or transmitted (for a processor read). This signal needs a 10k Ohm external pull-up.	
PINT	LVTTL	O	AF16	Processor interrupt indicator. Active low output. When active, this signal notifies the processor to begin interrupt servicing.	

Table 80 Forward Error Correction (FEC) Signals

Name	Level	I/O	Ball #	Description	Shared Pin
FEC_ENC	LVTTL	I	H4	FEC encoder enable. Active high input. When active, this signal turns on forward error correction encoding with 8-byte error correction (unless the default error correction value has been changed). If the processor interface is activated by loading the Micro Present byte with a value of 59h, this pin will be ANDed with the inverted FEC Encode OFF register bit. The FEC_ENC signal has an internal weak pull-down on it to disable encoding if the input pin is not connected.	
FEC_DEC	LVTTL	I	C21	FEC decoder enable. Active high input. When active, this signal turns on forward error correction decoding with 8-byte error correction (unless the default error correction value has been changed). If the processor interface is activated by loading the Micro Present byte with a value of 59h, this pin is ANDed with the inverted FEC Decode OFF register bit. The FEC_DEC signal has an internal weak pull-down on it to disable encoding if the input pin is not connected.	
FEC_RDIV	LVTTL.	O	F23	FEC divided RX clock output. This output is the RX input clock divided down according to the values in Table 5 in the Forward Error Correction Algorithm section. (The processor can also program the divided down value)	
FEC_TDIV	LVTTL.	O	W2	FEC divided TX clock output. This output is the TX input clock divided down according to the values in Table 5 in the Forward Error Correction Algorithm section. (The processor can also program the divided down value)	
FEC_ERR	LVTTL	O	B22	FEC error output. Active high output. This output is active for two CLKOUTP pulses to indicate that one symbol error has been corrected. If there are more errors than the FEC decoder can correct, FEC_ERR will be active for the whole 255-byte block. FEC_ERR will also be active when the FEC decoder is out of frame. FEC_ERR is updated on the rising edge of CLKOUTP. The guaranteed minimum pulse width of this signal is 9ns for an OC-48 signal with 8-byte FEC encoding.	
RX_FEC_DLCK	LVTTL	O	R26	FEC RX data link clock output. This pin is multiplexed with the SCRBEN signal and is only available when a processor is connected and the Micro Present byte is loaded with a value of 59h. This signal is a gapped clock with a maximum frequency of 13.95MHz.	SCRBEN
RX_FEC_DL	LVTTL	O	P24	FEC RX data link output. This pin is multiplexed with the DESCRBEN signal and is only available when a processor is connected and the Micro Present byte is loaded with a value of 59h. This signal is updated on the falling edge of RX_FEC_DLCK.	DESCRBEN
TX_FEC_DLCK	LVTTL	O	W3	FEC TX data link clock output. This pin is multiplexed with the BLOCKBIP signal and is only available when a processor is connected and the Micro Present byte is loaded with a value of 59h. This signal is a gapped clock with maximum frequency of 13.95MHz.	BLOCKBIP

Name	Level	I/O	Ball #	Description	Shared Pin
TX_FEC_DL	LVTTL	I	V3	FEC TX data link input. This pin is multiplexed with the XORBIP signal and is only available when a processor is connected and the Micro Present byte is loaded with a value of 59h. This signal must be updated on the falling edge of TX_FEC_DLCK.	XORBIP

Table 81 FPGA Signals (FPGASEL = 1, Active High)

Name	Level	I/O	Ball #	Description	Shared Pin
RX_OH_DATA[7] RX_OH_DATA[6] RX_OH_DATA[5] RX_OH_DATA[4] RX_OH_DATA[3] RX_OH_DATA[2] RX_OH_DATA[1] RX_OH_DATA[0]	LVTTL	O	B10 D11 A9 A11 D12 B11 A12 D13	Receive overhead data output. STS-N/STM-M received overhead data from the received data stream. Data is to be latched out of the S3062 with the OH_CLK.	RX_SOW RX_LOW RX_OW_CLK RX_OW_FP RX_SDCC RX_SDCC_CLK RX_LDCC RX_LDCC_CLK
OH_CLK	LVTTL	O	D6	Overhead receive and transmit clock‡‡‡‡‡ of frequency of 19.44MHz (or 1.62MHz for STS-3/STM-1) used by an external FPGA. The S3062 latches out the received overhead RX_OH_DATA[7:0] data with this clock and also latches in the transmitted overhead TX_OH_DATA[7:0] data.	TX_OW_CLK
RX_OH_FP	LVTTL	O	A4	Overhead frame pulse. Active high output. A single OH_CLK period wide pulse, active during the first RX_OH_DATA A1 byte.	TX_OW_FP
TX_OH_FP	LVTTL	O	B12	Overhead frame pulse. Active high output. A single OH_CLK period wide pulse which is active eight clock ticks after the RX_OH_FP is active. This allows an external FPGA to easily READ/MODIFY/WRITE section and line overhead.	TX_SDCC_CLK

‡‡‡‡‡ The transmit and receive overhead data are inserted/extracted on the transmit side of the S3062 FIFO. Therefore, the OH_CLK frequency will increase by the bandwidth expansion factor listed in Table 4 when the FEC encoder is ON.

Name	Level	I/O	Ball #	Description	Shared Pin
TX_OH_DATA[7] TX_OH_DATA[6] TX_OH_DATA[5] TX_OH_DATA[4] TX_OH_DATA[3] TX_OH_DATA[2] TX_OH_DATA[1] TX_OH_DATA[0]	LVTTL	I	B18 A19 D17 C18 C19 B20 D19 A22	Transmit overhead data input. STS-N/STM-M transmitted overhead data for the transmit data stream. Data is to be latched into the S3062 with the OH_CLK.	TX_SOW TX_SOW_SEL TX_LOW TX_LOW_SEL TX_SDCC TX_SDCC_SEL TX_LDCC TX_LDCC_SEL
TX_OH_INS	LVTTL	I	A21	Transmit overhead insertion select. Active high input . When active, TX_OH_DATA will be inserted into the transmit data stream, unless overridden by the OIC memory.	

- The control signal FPGA Mode Select [FPGASEL] determines whether the pins are configured as a single read/write FPGA interface or as a number of section and line serial link interfaces.

Table 82 Overhead Serial Signals (FPGASEL = 0, NOT Active)

Name	Level	I/O	Ball #	Description	Shared Pin
RX_SOW	LVTTL	O	B10	Received section orderwire output. Updated on the falling edge of RX_OW_CLK. The MSB is delivered first, synchronous with RX_OW_FP. This function has no effect if FPGA Select has been activated.	RX_OH_DATA[7]
RX_LOW	LVTTL	O	D11	Received line orderwire output. Updated on the falling edge of RX_OW_CLK. MSB delivered first, synchronous with RX_OW_FP. This function has no affect if FPGA Select has been activated.	RX_OH_DATA[6]
RX_OW_CLK	LVTTL	O	A9	Received orderwire clock. Gapped 9.72MHz* clock, active for 8 cycles every frame, high otherwise. This function has no effect if FPGA Select has been activated.	RX_OH_DATA[5]
RX_OW_FP	LVTTL	O	A11	Received orderwire frame pulse. Active high output. Updated on the falling edge of RX_OW_CLK. One clock period wide. Active on MSB of RX_LOW and RX_SOW. This function has no effect if FPGA Select has been activated.	RX_OH_DATA[4]
RX_SDCC	LVTTL	O	D12	Received section data communication channel serial output. Updated on the falling edge of RX_SDCC_CLK. MSB of each DCC byte delivered first, in order D1-D3. This function has no effect if FPGA Select has been activated.	RX_OH_DATA[3]
RX_SDCC_CLK	LVTTL	O	B11	Received SDCC clock. Gapped 9.72MHz* clock, active for 24 cycles in every frame, high otherwise. This function has no effect if FPGA Select has been activated.	RX_OH_DATA[2]
RX_LDCC	LVTTL	O	A12	Received line data communication channel serial output. Updated on the falling edge of RX_LDCC_CLK. MSB of each DCC byte delivered first, in order D4-D12. This function has no effect if FPGA Select has been activated.	RX_OH_DATA[1]
RX_LDCC_CLK	LVTTL	O	D13	Received LDCC clock. Gapped 9.72MHz clock, active for 72 cycles in every frame, high otherwise. This function has no effect if FPGA Select has been activated.	RX_OH_DATA[0]
TX_OW_CLK	LVTTL	O	D6	Transmitted orderwire clock. Gapped 9.72MHz* clock, active for 8 cycles every frame, high otherwise. This function has no effect if FPGA Select has been activated.	OH_CLK
TX_OW_FP	LVTTL	O	A4	Transmitted orderwire frame pulse. Active high output. Updated on the falling edge of TX_OW_CLK. One clock period wide. This function has no effect if FPGA Select has been activated.	RX_OH_FP
TX_SDCC_CLK	LVTTL	O	B12	Transmitted SDCC clock. Gapped 9.72MHz* clock, active for 24 cycles in every frame, high otherwise. This function has no effect if FPGA Select has been activated.	TX_OH_FP
TX_LDCC_CLK	LVTTL	O	C14	Transmitted LDCC clock. Gapped 9.72MHz clock*, active for 72 cycles in every frame,	

* The frequency increases by the FEC encode bandwidth expansion when the FEC encoder is ON.

Name	Level	I/O	Ball #	Description	Shared Pin
				high otherwise.	
TX_SOW	LVTTL	I	B18	Transmitted section orderwire input. This is the section orderwire input data port (E1). It is sampled on the rising edge of TX_OW_CLK. The most significant bit is delivered first, synchronous with TX_OW_FP. This function has no effect if FPGA Select has been activated.	TX_OH_DATA[7]
TX_SOW_SEL	LVTTL	I	A19	Transmitted section orderwire select. Active high input. Synchronous with TX_SOW. When active, E1 overhead data is sourced from the TX_SOW pin and will be inserted into the outgoing overhead data stream. This function has no effect if FPGA Select has been activated.	TX_OH_DATA[6]
TX_LOW	LVTTL	I	D17	Transmitted line orderwire input. This is the line orderwire input data port (E2). It is sampled on the rising edge of TX_OW_CLK. The most significant bit is delivered first, synchronous with TX_OW_FP. This function has no effect if FPGA Select has been activated.	TX_OH_DATA[5]
TX_LOW_SEL	LVTTL	I	C18	Transmitted line orderwire select. Active high input. Synchronous with TX_LOW. When active, E2 overhead data sourced from the TX_LOW pin will be inserted into the outgoing overhead data stream. This function has no effect if FPGA Select has been activated.	TX_OH_DATA[4]
TX_SDCC	LVTTL	I	C19	Transmitted section DCC input. This is the section DCC input port. It is sampled on the rising edge of TX_SDCC_CLK. The most significant bit of each DCC byte is delivered first, in order D1-D3. This function has no effect if FPGA Select has been activated.	TX_OH_DATA[3]
TX_SDCC_SEL	LVTTL	I	B20	Transmitted section DCC select. Active high input. Synchronous with TX_SDCC. When active, SDCC overhead data sourced from the TX_SDCC pin will be inserted into the outgoing overhead data stream. This function has no effect if FPGA Select has been activated.	TX_OH_DATA[2]
TX_LDCC	LVTTL	I	D19	Transmitted line DCC input. This is the line DCC input port. It is sampled on the rising edge of TX_LDCC_CLK. The most significant bit of each DCC byte is delivered first, in order D4-D12. This function has no effect if FPGA Select has been activated.	TX_OH_DATA[1]
TX_LDCC_SEL	LVTTL	I	A22	Transmitted line DCC select. Active high input. Synchronous with TX_LDCC. When active, LDCC overhead data sourced from the TX_LDCC pin will be inserted into the outgoing overhead data stream. This function has no effect if FPGA Select has been activated.	TX_OH_DATA[0]

- The pins for these interfaces are shared. The control signal FPGA Mode Select [FPGASEL] determines whether the pins are configured as a single read/write FPGA interface or as a number of section and line serial link interfaces.

Table 83 JTAG, Scan and RAM BIST Signals

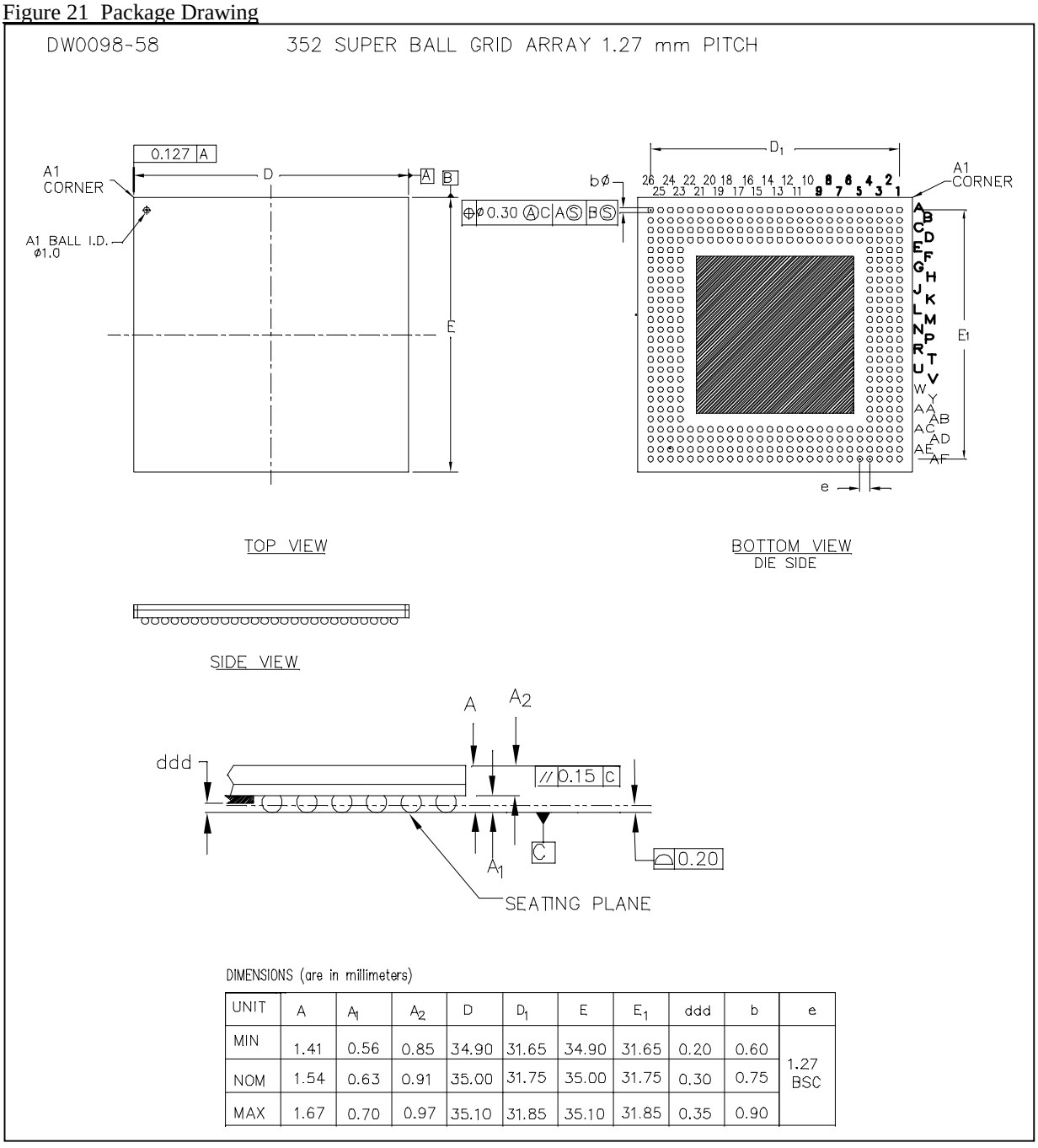
Name	Level	I/O	Ball #	Description	Shared Pin
TCK	LVTTL	I	V24	Test clock input. JTAG port test clock input.	
TMS	LVTTL	I	T26	Test mode select input. JTAG port test mode select. This input has an internal pull-up	
TDI	LVTTL	I	V26	Test data input. JTAG port test data input. This input has an internal pull-up	
TDO	LVTTL Tri-State	O	R23	Test data output. JTAG port test data output. This output driver is disabled when the JTAG port is in reset. Connect a weak external pull-up to prevent noise.	
TRSTB	LVTTL	I	N25	Test RESET input. Active low input. Asynchronous JTAG port reset. This input has an internal pull-up. When in normal device operation (mission mode), the JTAG port must be held in its reset state. One way to accomplish this is to drive this input low to ensure the test mode is OFF. The JTAG test features may only be accessed when the JTAG port is not in reset.	
TM	LVTTL	I	AE8	Global test mode input. Active high input. Configures internal clock generator to by-pass SONET clock generation and instead generate the scan and BIST clocks. Drive this input low for normal device operation.	
TST_SE	LVTTL	I	AF7	Global scan enable input. Active high input. Enables serial scan shifting that is required to support scan testing with ATPG vectors. Drive this input low for normal device operation.	
TST_IN_BIST_CLK TST_IN_SERIAL TST_IN_OH TST_IN_FPGA TST_IN_CLKIN TST_IN_DEC TST_IN_CLKOUT TST_IN_ENC TST_IN_TXCLK TST_IN_RXCLK TST_IN_CLKTX TST_IN_PIF TST_IN_CLKH TST_IN_PCLK TST_IN_GIG	LVTTL	I	C9 A7 B8 D8 W23 Y24 AA3 AA4 AB3 AB26 AC1 AC8 AD8 AE7 AF6	Inputs to internal scan chains used during scan testing with ATPG vectors. Tie these pins high or low for normal device operation.	
TST_OUT_FPGA TST_OUT_OH TST_OUT_SERIAL TST_OUT_BIST_CLK	LVTTL	O	B5 B6 C6 C7	Outputs from internal scan chain. 2-state output drivers. Outputs from the internal scan chains used during scan testing with ATPG vectors. These outputs may be left floating during normal device operation.	

Name	Level	I/O	Ball #	Description	Shared Pin
TST_OUT_RXCLK TST_OUT_DEC TST_OUT_CLKIN TST_OUT_ENC TST_OUT_PIF TST_OUT_CLKH TST_OUT_CLKOUT TST_OUT_CLKTX TST_OUT_TXCLK TST_OUT_PCLK TST_OUT_GIG			T23 T24 U26 AC5 AC6 AC7 AD1 AD4 AD5 AD6 AF4		
LV_TM BIST_EN	LVTTL	I	C16 D15	Memory BIST control inputs. Drive these controls low when running the chip normally. To run the test modes, LV_TM BIST_EN OPERATION 0 0 Normal operation 0 1 BIST mode 1 0 Scan mode	
BIST_CLK	LVTTL	I	A15	Memory BIST clock input. Drive this input low during normal device operation.	
  MBIST_ON MBIST_DONE MBIST_GO		 O O O	 D16 A16 B17	Memory BIST status output. 2-state output drivers. Outputs may be left floating during normal device operation. - MBIST test is RUNNING when output is active high. - MBIST test has been COMPLETED when output is active high. - MBIST test has PASSED when output is active high.	

Table 84 Power and Ground Signals

Name	Level	I/O	Ball #	Description
VDD0	3.3V		B2, B25, C3, C24, D4, D9, D14, D18, D23, J4, J23, N4, P23, V4, V23, AC4, AC9, AC13, AC18, AC23, AD3, AD24, AE2, AE25	3.3V power input. Supplies power to all PECL inputs, PECL pre drivers, TTL inputs and CORE logic.
VSS0	GND		A1, A2, A13, A14, A25, A26, B1, B3, B24, B26, C2, C25, N1, N26, P1, P26, AD2, AD25, AE1, AE3, AE24, AE26, AF1, AF2, AF13, AF14, AF25, AF26	Ground input. Supplies a ground connection to all PECL inputs, PECL pre drivers, TTL inputs and CORE logic.
VDD1	3.3V		B9, B13, D21, R25, AA1, AC16, AC17, AC21, AD23, AE4, AE6, AE20, AF22	3.3V power input. Supplies power to all TTL outputs.
VSS1	GND		B14, C10, C22, R24, Y2, AC22, AD19, AE17, AE21, AF3, AF5, AF19, AF23	Ground input. Supplies a ground connection to all TTL outputs.
VDD2	3.3V		D3, E1, F3, F4, G2, H1, J1, J3, K2, L2, M2, N3, P2, R1, R4, U1, U2, V2	3.3V power input. Supplies power to all PECL outputs.
VSS2	GND		E4, H3, M4, R2, W1	Ground input. Supplies a ground connection to all PECL outputs.
NO CONNECT (N/C)			All Unlisted Pins	Leave Floating during normal device operation.

Figure 21 Package Drawing

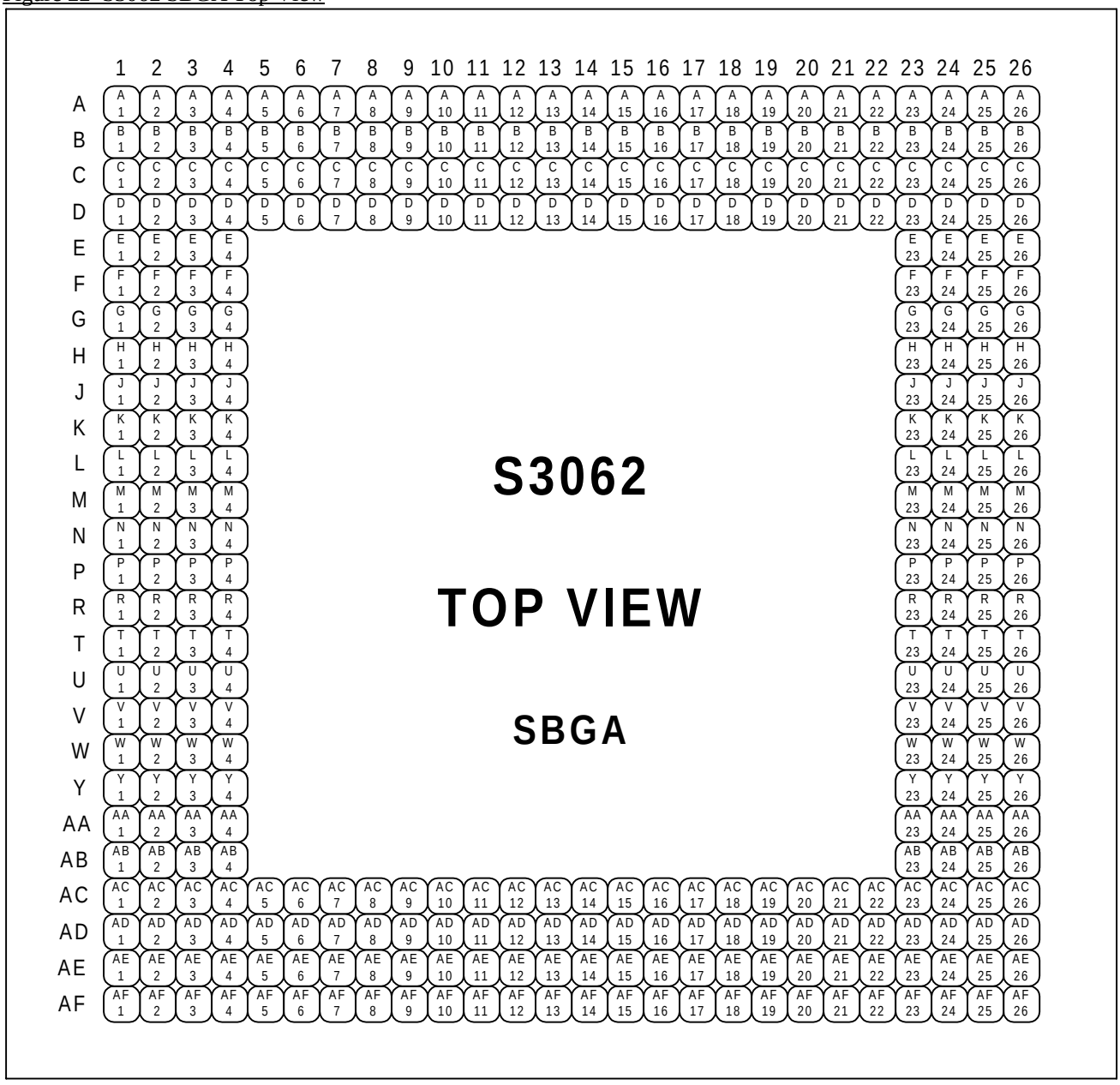


DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	ddd	b	e
MIN	1.41	0.56	0.85	34.90	31.65	34.90	31.65	0.20	0.60	1.27 BSC
NOM	1.54	0.63	0.91	35.00	31.75	35.00	31.75	0.30	0.75	
MAX	1.67	0.70	0.97	35.10	31.85	35.10	31.85	0.35	0.90	

Device	MAX Package Power	θ_{JC}	θ_{JA}
S3062	4.70W	0.72°C/W	11.7°C/W

Figure 22 S3062 SBGA Top View



NOTE: See Section 4, S3062 Pin Descriptions, for a detailed list of pin names, descriptions and ball numbers.

5 ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Table 85 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-40	125	°C
Voltage on V_{DD} with Respect to V_{SS}	-0.5	+3.8	V
Voltage on Any LVPECL Input Pin	0	V_{DD}	V
Voltage on Any LVTTL Input Pin	-0.5	V_{DD}+0.5	V
LVTTL Output sink current		8	mA
LVTTL Output source current		8	mA
ESD Sensitivity§§§§§	2000		V

5.2 Recommended Operating Conditions

Table 86 Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Ambient Temperature Under Bias	0		70	°C
Voltage On V_{DD} with Respect to V_{SS}	3.135	3.300	3.465	V
Voltage on Any LVPECL Input Pin	V_{DD} -2.0		V_{DD} -0.3	V
Voltage on Any LVTTL Input Pin	0		V_{DD}	V
Power Dissipation, STS-48 mode without FEC		1.560	2.240	W
Power Dissipation, STS-48 mode with FEC Decode & Encode		4.110	5.570	W
I_{DD}, MAX			1.610	A
I_{DD}, STS-3 mode without FEC		0.111	0.180	A
I_{DD}, STS-12 mode without FEC		0.142	0.270	A
I_{DD}, STS-48 mode without FEC		0.470	0.640	A
I_{DD}, STS-48 mode with FEC Encode Only		0.640	0.820	A
I_{DD}, STS-48 mode with FEC Decode Only		1.080	1.430	A
I_{DD}, STS-48 mode with FEC Decode & Encode		1.250	1.610	A
I_{DD}, Pass-Through mode (OC-48 data) without FEC		0.240	0.380	A
I_{DD}, Pass-Through mode (OC-48 data) with FEC Encode Only		0.400	0.560	A
I_{DD}, Pass-Through mode (OC-48 data) with FEC Decode Only		0.880	1.200	A
I_{DD}, Pass-Through mode (OC-48 data) with FEC Decode & Encode		1.050	1.380	A
I_{DD}, 1.25 Gigabit Ethernet mode without FEC		0.140	0.270	A

All power and current values for the FEC modes were calculated using the worst case RS(255,239) 8-byte correcting code.

§§§§§ Human Body model.

5.2.1 Heatsink/Airflow Requirements

- A heatsink with 50FPM airflow is required for:
  STS-48 mode with FEC Decode and Encode enabled.
- Airflow 200FPM (or a heatsink with no airflow) is required for:
  STS-48 mode with FEC Decode enabled.
  Pass-Through mode (OC-48 data) with FEC Decode and Encode enabled
- NO heatsink or airflow is required for all other configurations.

5.3 LVTTL Input/Output DC Characteristics

Table 87 LVTTL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
V_{OH}	Output HIGH Voltage (LVTTL) +3.3V Power Supply	2.4			V	V_{DD}=min, I_{OH}=-8mA Valid for all TTL outputs except: PTA, PINT, PDAT[15:0] V_{DD}=min, I_{OH}=-16mA Valid only for the TTL outputs: PTA, PINT, PDAT[15:0]
V_{OL}	Output LOW Voltage (LVTTL) +3.3V Power Supply			0.4	V	V_{DD}=min, I_{OL}=+8mA Valid for all TTL outputs except: PTA, PINT, PDAT[15:0] V_{DD}=min, I_{OL}=+16mA Valid only for the TTL outputs: PTA, PINT, PDAT[15:0]
V_{IH}	Input HIGH Voltage (LVTTL)	V_{DD} * 0.7			V	
V_{IL}	Input LOW Voltage (LVTTL)			V_{DD} * 0.3	V	
I_{IH}	Input HIGH Current (LVTTL)	-10		10	µA	$V_{IN}=V_{DD}$
I_{IH}	Input HIGH Current w/Pull-Up	-10		10	µA	$V_{IN}=V_{DD}$
I_{IH}	Input HIGH Current w/Pull-Down	4		100	µA	$V_{IN}=V_{DD}$
I_{IL}	Input LOW Current (LVTTL)	-10		10	µA	$V_{IN}=V_{SS}$
I_{IL}	Input LOW Current w/Pull-Up	-100		-4	µA	$V_{IN}=V_{SS}$
I_{IL}	Input LOW Current w/Pull-Down	-10		10	µA	$V_{IN}=V_{SS}$
I_{OZ}	3-State Output Leakage Current	-10		10	µA	$V_{OH} = V_{SS}$ OR V_{DD}

5.4 LVPECL Input/Output DC Characteristics

5.4.1 Differential LVPECL Input DC Characteristics

Table 88 Differential LVPECL Input DC Characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
V_{IL}	LVPECL Input Low	V_{DD}-2.00		V_{DD}-1.40	V	
V_{IH}	LVPECL Input High	V_{DD}-1.20		V_{DD}-0.30	V	
I_{IH}	LVPECL Input HIGH Current	-10		10	µA	
I_{IL}	LVPECL Input LOW Current	-10		10	µA	
ΔV_{INDIFF}	Differential Input Voltage Swing	400		2000	mV	See Figure 23
$\Delta V_{INSINGLE}$	Single-Ended Input Voltage Swing	200		1000	mV	See Figure 23

5.4.2 Differential LVPECL Output DC Characteristics

Table 89 Differential LVPECL Output DC Characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
V_{OL}	LVPECL Output Low	V_{DD}-1.90		V_{DD}-1.50	V	See Figure 24
V_{OH}	LVPECL Output High	V_{DD}-1.10		V_{DD}-0.60	V	See Figure 24
I_{OH}	LVPECL Output HIGH Current		16.0	22.6	mA	
I_{OL}	LVPECL Output LOW Current		0.0		mA	
$\Delta V_{OUTDIFF}$	Differential Output Voltage Swing ($V_{OUT\{+\)}$ - $V_{OUT(-)}$: see Figure 23)	1000		2000	mV	See Figure 23.
$\Delta V_{OUTSINGLE}$	Single-Ended Output Voltage Swing	500		1000	mV	See Figure 23.

5.4.3 Single-Ended LVPECL Input/Output DC Characteristics

Table 90 Single-Ended LVPECL Input/Output DC Characteristics

Parameters	Description	Min	Typ	Max	Unit	Conditions
V_{IL}	LVPECL Input LOW Voltage	V_{DD}-2.30		V_{DD} -1.44	V	
V_{IH}	LVPECL Input HIGH Voltage	V_{DD}-1.25		V_{DD}-0.57	V	
V_{OL}	LVPECL Output LOW Voltage	V_{DD}-1.75		V_{DD}-1.50	V	See Figure 24
V_{OH}	LVPECL Output HIGH Voltage	V_{DD}-1.10		V_{DD}-0.65	V	See Figure 24
I_{IH}	LVPECL Input HIGH Current	-10		10	µA	
I_{IL}	LVPECL Input LOW Current	-10		10	µA	
I_{OH}	LVPECL Output HIGH Current		16.0	21.6	mA	
I_{OL}	LVPECL Output LOW Current		0.0		mA	
PECLREF	Single-Ended PECL DC Bias Voltage	V_{DD}-1.80		V_{DD}-1.20	V	PECLREF = (VOH + VOL)/2 ± 120mV Where VOH and VOL are received from the AMCC DeMUX or Transceiver.
PECLREF	Input sink current			20	µA	

Figure 23 Voltage Measurement

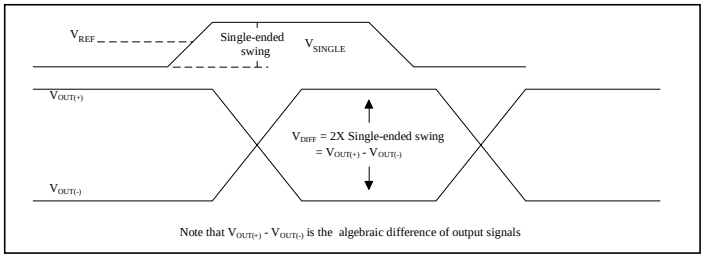
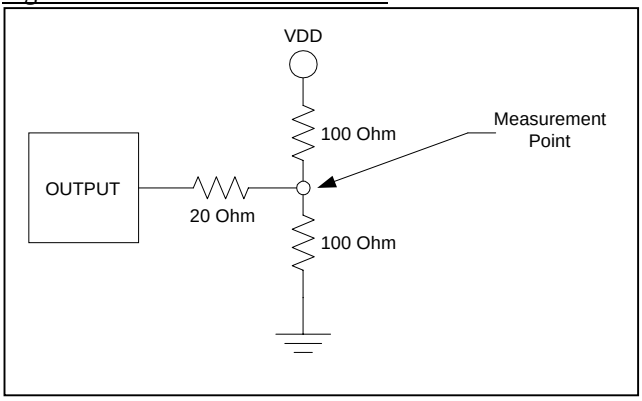


Figure 24 VOH/VOL Measurement



6 TIMING SPECIFICATIONS

6.1 Rise and Fall Times for TTL Outputs

Table 91 Rise and Fall Times for all LVTTL Outputs

Description	MAX t_{RISE}	MAX t_{FALL}	Units	Condition
LVTTL High Speed Outputs, (LOS, LOF, OOF, INV_CODE, SYNC_LOSS, DISP_ERR, B1ERR, FEC_TDIV, FEC_RDIV, FEC_ERR)	6.5	6.5	ns	0.8 – 2.0V
LVTTL Low Speed Outputs, (PDAT[15:0], PTA, PINT, FPOUTB, TDO, RX_OH_DATA[7:0], OH_CLK, RX_OH_FP, TX_OH_FP, TX_LDCC_CLK, RX_FEC_DLCK, TX_FEC_DLCK, RX_FEC_DL)	6.5	6.5	ns	0.8 – 2.0V

1. All measurements of outgoing signals are assumed to have an output load of 25pF.

6.2 Data Output AC Timing Characteristics

Table 92 Data Output AC Timing: Propagation Delay and Pulse Width (all STS/STM/GBE Modes)

Symbol	Description	Min	Max	Units
tPD_{DATO}	Propagation Delay: Data Output referenced to CLKOUTP rising	0.6	4	ns
tPD_{STATO}	Propagation Delay: Status Output referennced to CLKOUTP rising	0.8	6.2	ns
tPW_{STATO}	Pulse Width: Status Output, ALL Modes	9.0		ns

1. All measurements of outgoing signals are assumed to have an output load of 25pF.
2. DATA outputs are the data bus signals DATAOUT[15:0].
2. Status outputs include the signals LOS, OOF, LOF, FPOUTB, B1ERR, FEC_ERR, INV_CODE, DISP_ERR, SYNC_LOSS.
3. Status output pulse width is measured from the 50% point of the status output signal.
4. All skews are measured from the 50% cross over point of the clock output to the 50% point of the data outputs.
5. The minimum pulse width value for FPOUTB is not the typical value. See Table 93 for FPOUTB Pulse Width values.

Figure 25 Data Output AC Timing Diagram

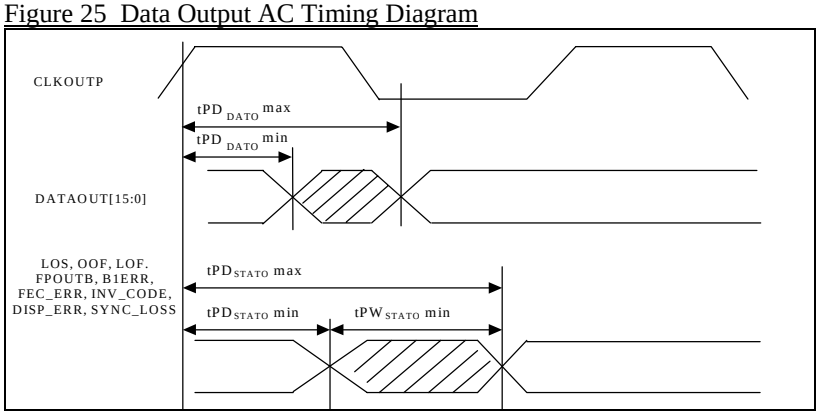
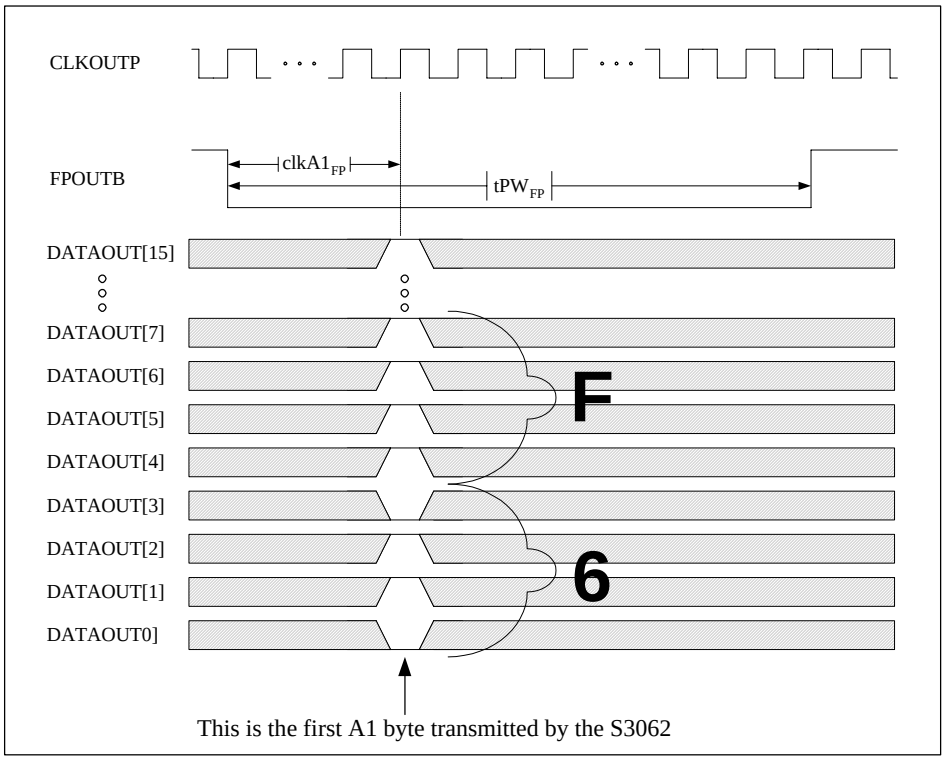


Table 93 FPOUTB Output AC Timing: Propagation Delay and Pulse Width (SONET/SDH Modes Only)

Symbol	Description	Min	Typ	Max	Units
$clkA1_{FP}$	Number of CLKOUTP cycles, from the start of the FPOUTB pulse, until the A1 (F6h) DATA Output Byte is Received. With Out the FEC Encoder enabled.		6		CLKOUTP Cycles
$clkA1_{FP}$	Number of CLKOUTP cycles, from the start of the FPOUTB pulse, until the A1 (F6h) DATA Output Byte is Received. With the FEC Encoder enabled.	8		72	CLKOUTP Cycles
tPW_{FP}	Pulse Width: FPOUTB, STS-48/STM-16 and STS-12/STM-3 modes		154		ns
tPW_{FP}	Pulse Width: FPOUTB, STS-3/STM-1 mode	102.5		208	ns

1. All measurements of outgoing signals are assumed to have an output load of 25pF.
2. Status output pulse width is measured from the 50% point of the status output signal.

Figure 26 FPOUTB Timing Diagram******



****** The FPOUTB for different revisions of the silicon may contain transitions during its active time. Please consult Errata 7.1 FPOUTB in the back of the data sheet for details.

6.3 Clock AC Timing Characteristics (all STS/STM/GBE Modes)

Table 94 Clock AC Timing: Propagation Delay and Duty Cycle (all STS/STM/GBE Modes)

Symbol	Description	Min	Max	Units
	Duty Cycle: TXCLKP/N	42	58	%
	Duty Cycle: CLKOUTP/N	40	60	%
t_{CHG}	Propagation Delay: TXCLKP to CLKOUTP, Steady-state Change	-5	5	ns

1. All measurements of outgoing signals are assumed to have an output load of 25pF.
2. After RESET or Power up of the S3062, the TXCLKP/N input to CLKOUTP/N output propagation delay must be valid and stable on the third rising edge of CLKOUTP/N clock.
3. Once the TXCLKP/N input to CLKOUTP/N output propagation delay is set (on the third CLKOUTP/N clock, after reset, or power up) the drift of the propagation delay must not exceed more than ± 5ns.
4. If t_{CHG} does alter more than ± 5ns, either reset the DeMUX or pulse its PHINIT pin to force it to re-check the propagation delay.

Figure 27 Clock Input (TXCLKP) to Output Clock (CLKOUTP) Propagation Delay

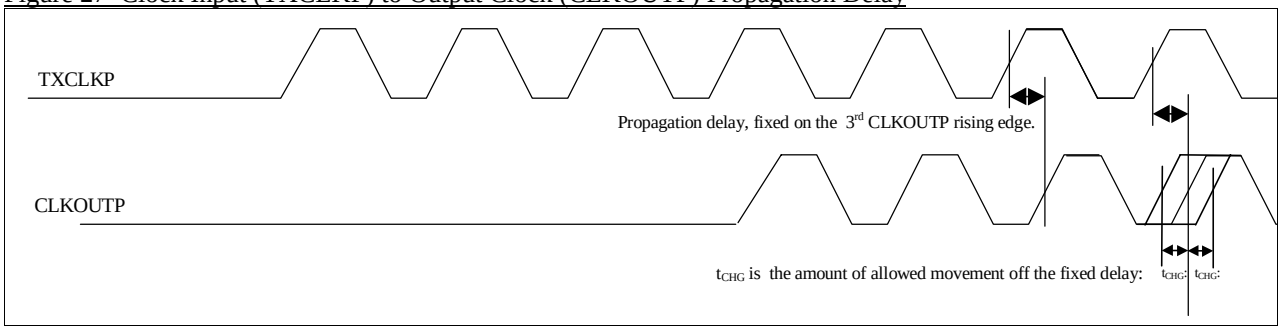
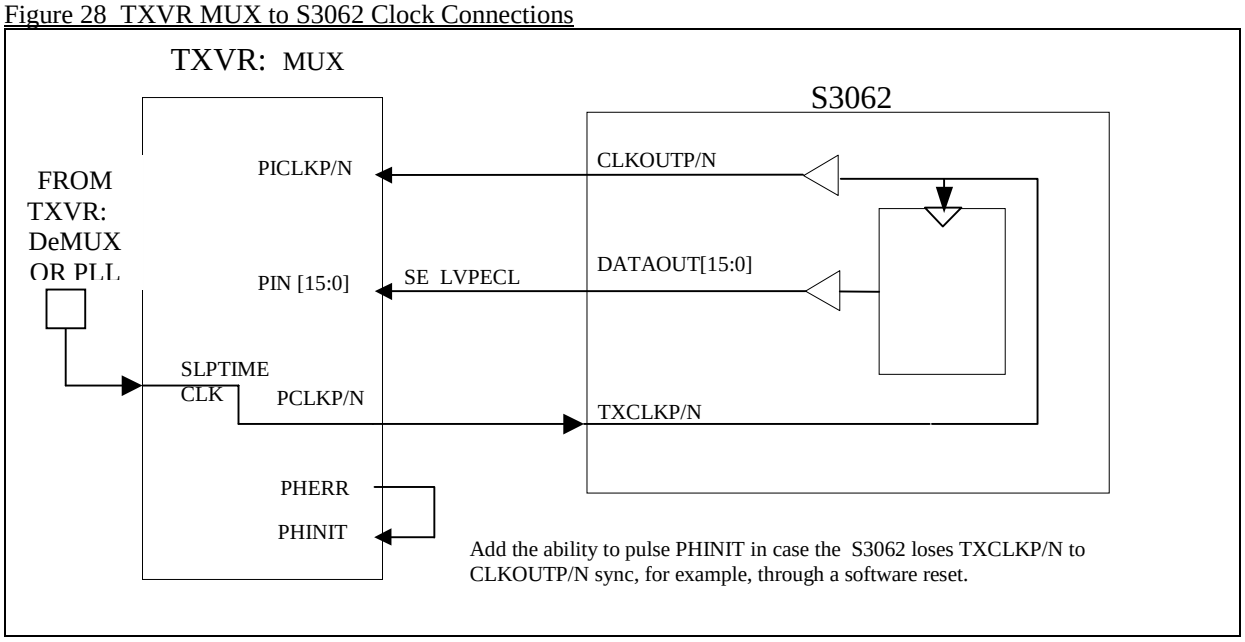


Figure 28 TXVR MUX to S3062 Clock Connections

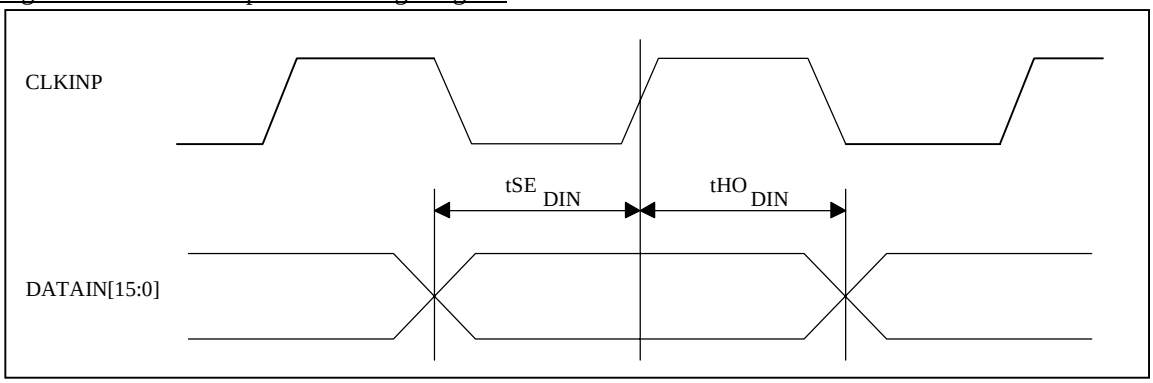


6.4 DATAIN Input AC Timing Characteristics

Table 95 DATAIN Input AC Timing: Set-Up, Hold and Duty Cycle

Symbol	Description	Min	Max	Units
	Duty Cycle: CLKINP/N	40	60	%
tSE_{DIN}	Set-up Time: DATAIN[15:0] w.r.t. CLKINP rising	1.5		ns
tHO_{DIN}	Hold Time: DATAIN[15:0] w.r.t. CLKINP rising	0.9		ns

Figure 29 DATAIN Input AC Timing Diagram



1. The set-up time is specified for LVPECL signals from the 50% point of the input to the 50% cross over point of the clock.
2. The hold time is specified for LVPECL signals from the 50% cross over point of the clock to the 50% point of the input.
3. The input signals: PASSTHRU, RATESEL, FPGASEL, MEMOH, FIXSOH, SCRBEN, DESCRBEN, FIXB2, BLOCKBIP, XORBIP, DATAAIS, AUTOAIS and DATAOFF are meant to be static control signals and no timings are provided for these signals, although they are latched by a clock divided down from the TXCLKP/N clock.

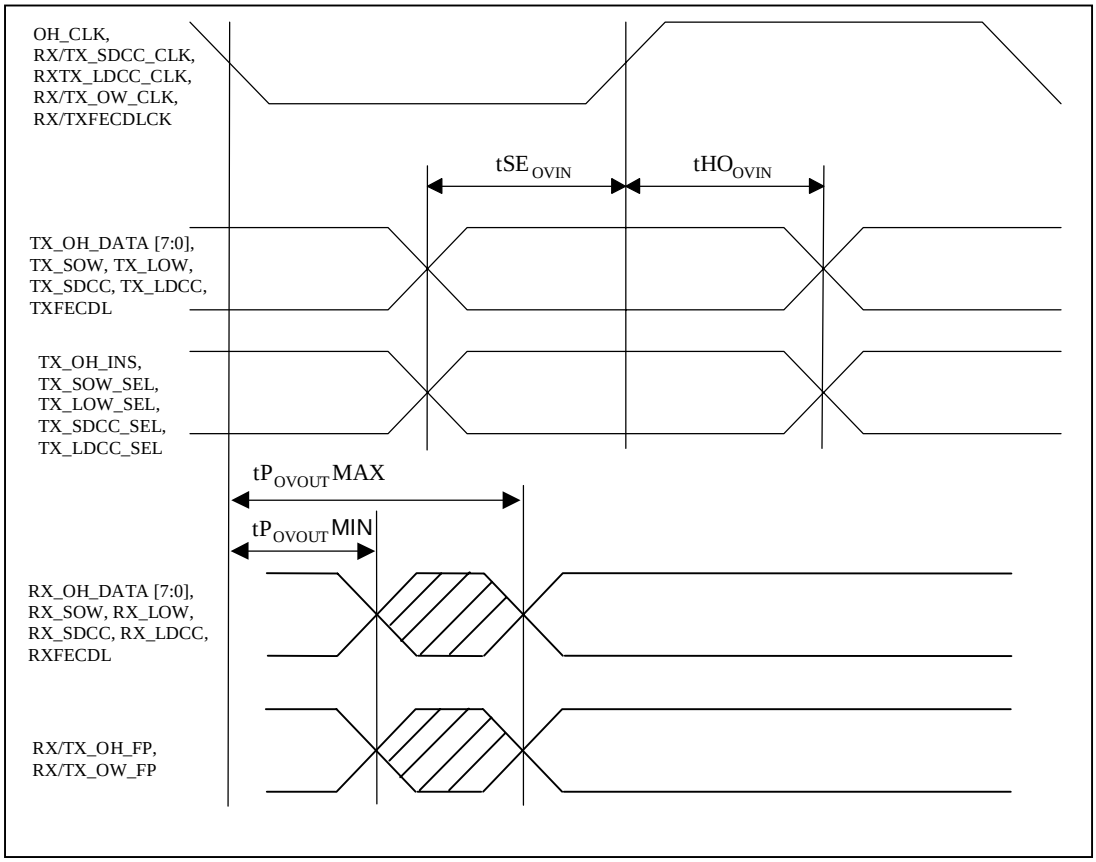
6.5 FPGA and Serial Links Port AC Timing Characteristics (all STS/STM modes)

Table 96 FPGA and Serial Links Port AC Timing: Set-Up, Hold, Propagation Delay and Duty Cycle

Symbol	Description	Min	Max	Units
	Duty Cycle: Clocks listed in Figure 30 .	40	60	%
tSE_{OVIN}	Set-up Time: Data and Select lines w.r.t CLK rising	3.9		ns
tHO_{OVIN}	Hold Time: Data and Select lines w.r.t CLK rising	4.6		ns
tP_{OVOUT}	Propagation Delay: Outputs listed in Figure 30 referenced to CLK falling edge	-2.0	4.5	ns

1. All measurements of outgoing signals are assumed to have an output load of 25pF.

Figure 30 FPGA and Serial Links Port Input AC Timing Diagram



1. When the set-up time is specified on LVTTL signals between an input and a clock, the set-up time is specified from the 50% point of the input to the 50% cross over point of the clock.
2. When a hold time is specified on LVTTL signals between an input and a clock, the hold time is the time is specified from the 50% cross over point of the clock to the 50% point of the input.

Figure 31 FPGA Port Functional Timings STS-3/STM-1 Mode

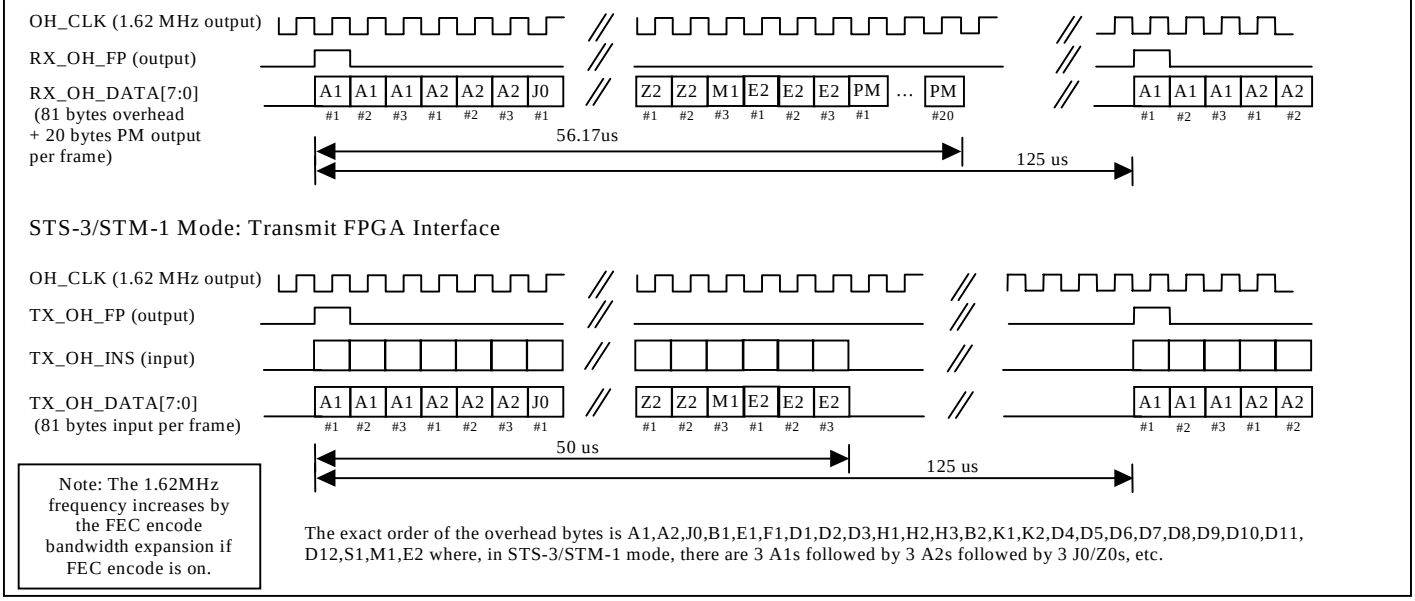


Figure 32 FPGA Port Functional Timings STS-12/STM-4 Mode

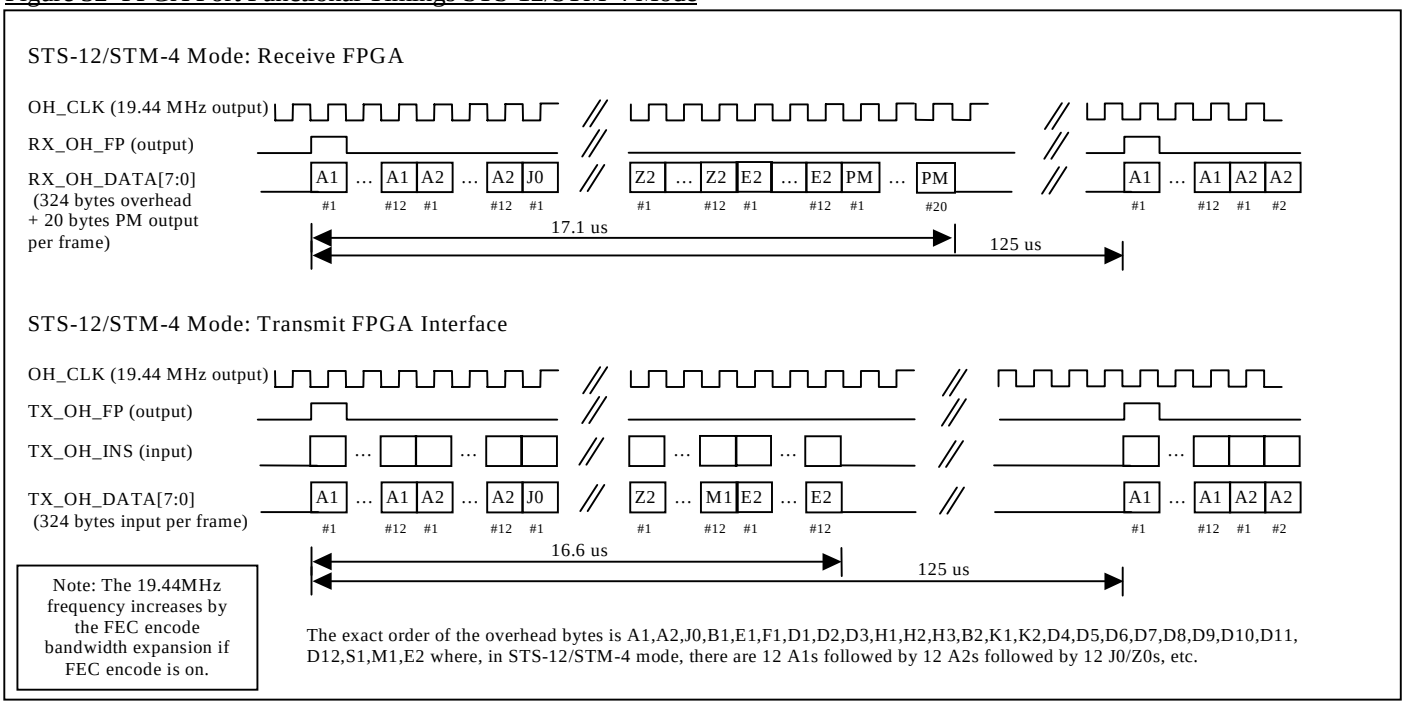


Table 97 FPGA and Serial Links: Gapped Clock Cycle Count

Symbol	Description	Min	Typ	Max	Units
clkACTIVE	Number of Active Cycles for the RX and TX OH_CLK		8		OH_CLK Cycles
clkACTIVE	Number of Active Cycles for the RX and TX_SDCC_CLK		24		SDCC_CLK Cycles
clkACTIVE	Number of Active Cycles for the RX and TX_LDCC_CLK		72		LDCC_CLK Cycles

1. All measurements of outgoing signals are assumed to have an output load of 25pF.
2. All of the FPGA overhead clocks are gapped with a cycle frequency of 9.72MHz. If FEC Encoding is enabled, the clock frequency will increase by the FEC Encoder bandwidth expansion rates listed in Table 4 .

Figure 33 FPGA and Serial Links: Gapped Clock Cycle Count

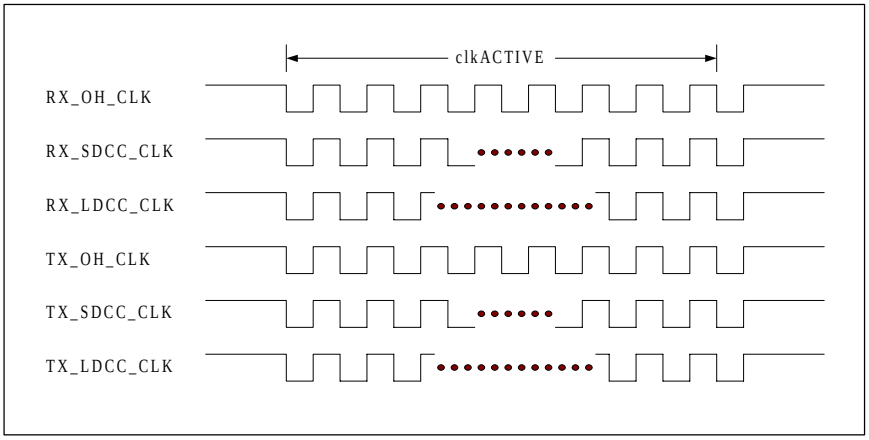


Figure 34 FPGA Port Functional Timings STS-48/STM-16 Mode

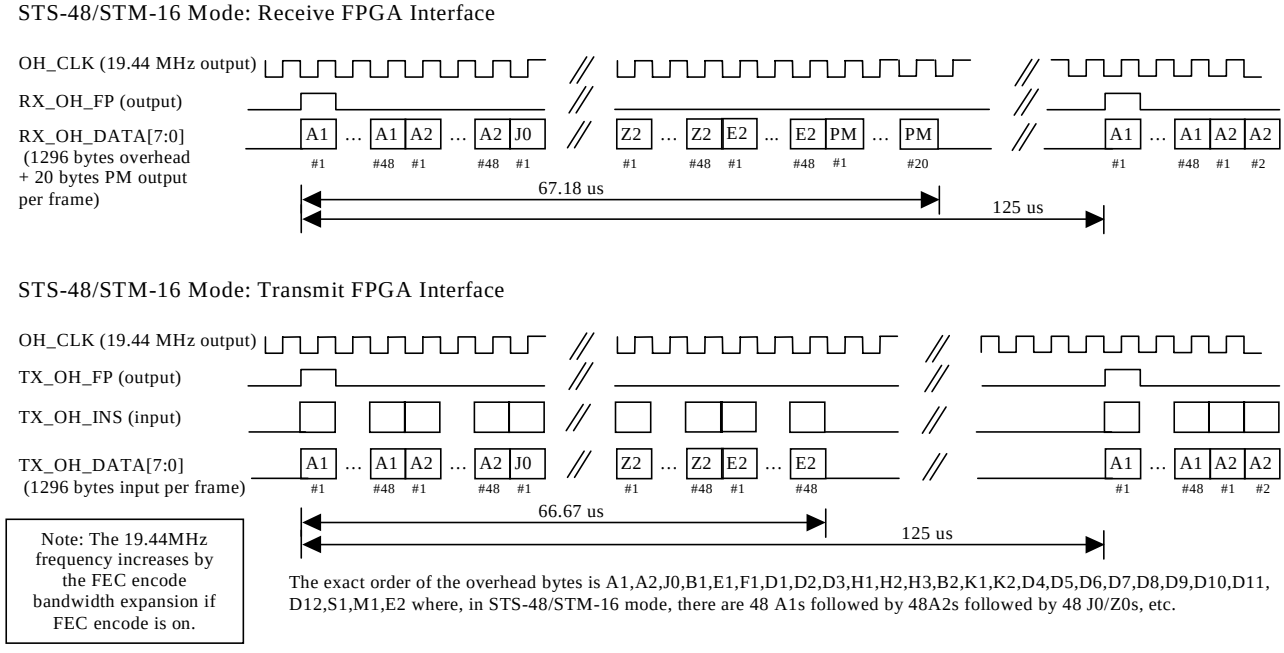


Figure 35 Serial Link Functional Timings

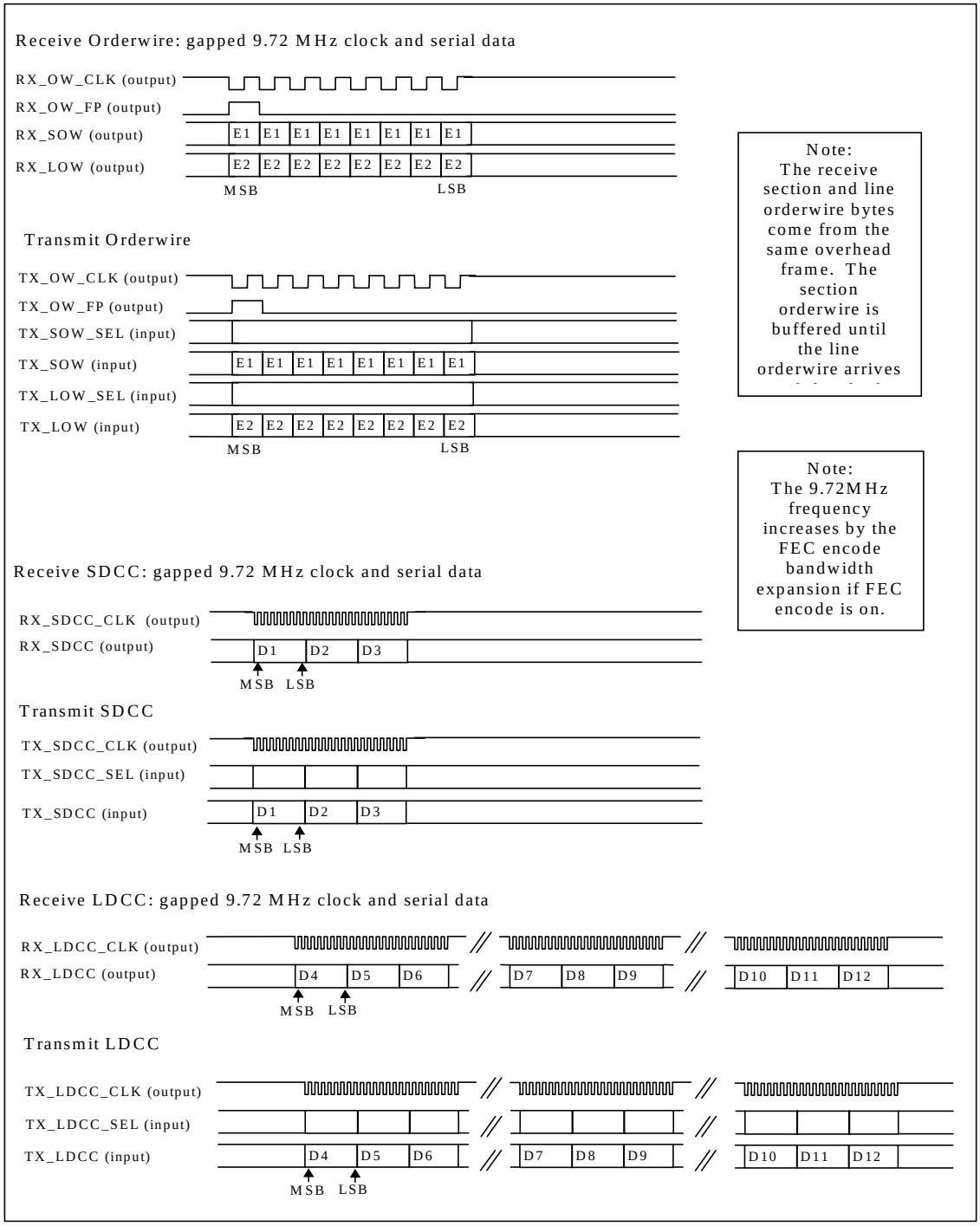
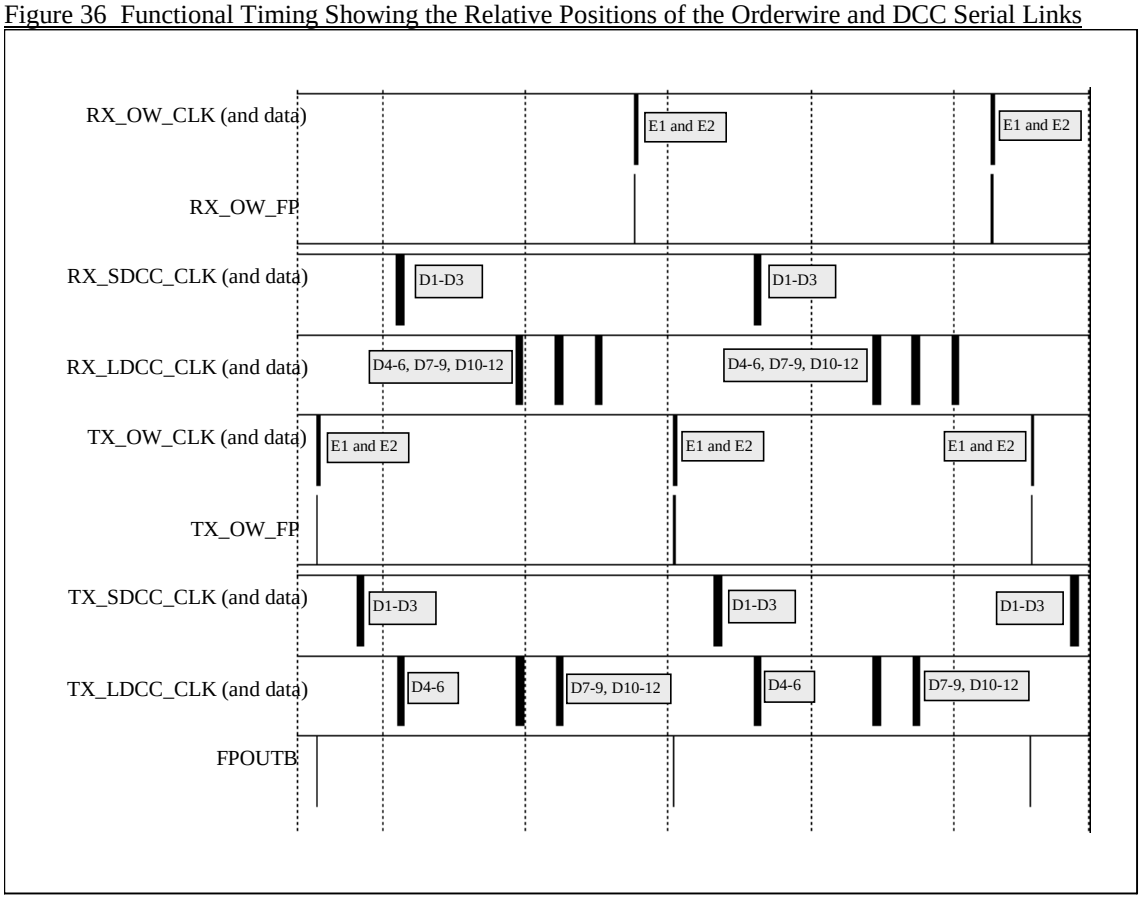


Figure 36 Functional Timing Showing the Relative Positions of the Orderwire and DCC Serial Links



Note: The relative positions of these signals remain the same even when FEC is ON.

6.6 Internal Page Swap Timing with respect to External Timing Signals

Note that in all the pictures in this section, the time between page swap and FPOUTB may increase by a maximum of (2T+1)*2 CLKOUT for STS-12 and STS-48 and by a maximum of ((2T+1)*2)+2 CLKOUT for STS-3 if FEC is on. "T" is defined in Section 3.1.8.

Figure 37 STS-3/STM-1 RX_OH and TX_OH Page Swaps w.r.t Frame Pulses and Clocks

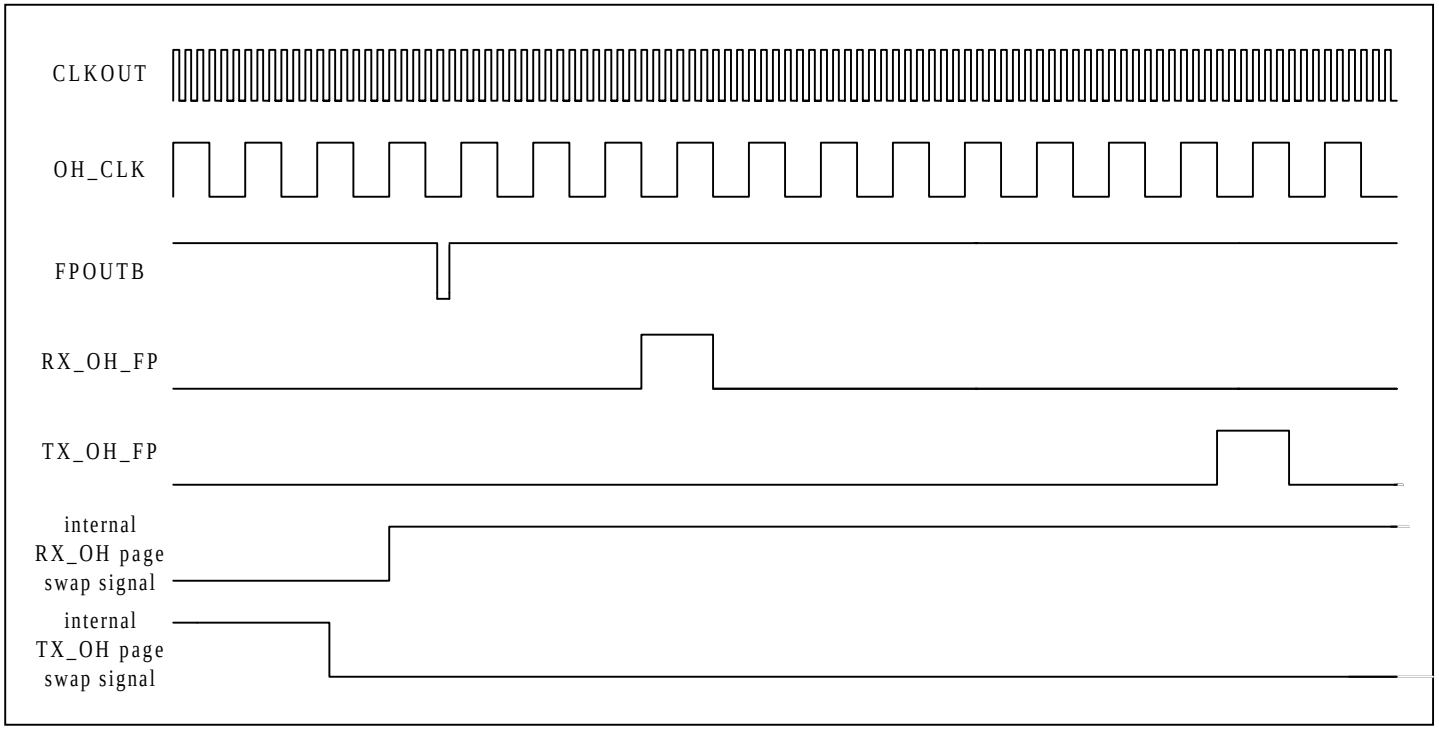


Figure 38 STS-12/STM-3 RX_OH and TX_OH Page Swaps w.r.t Frame Pulses and Clocks

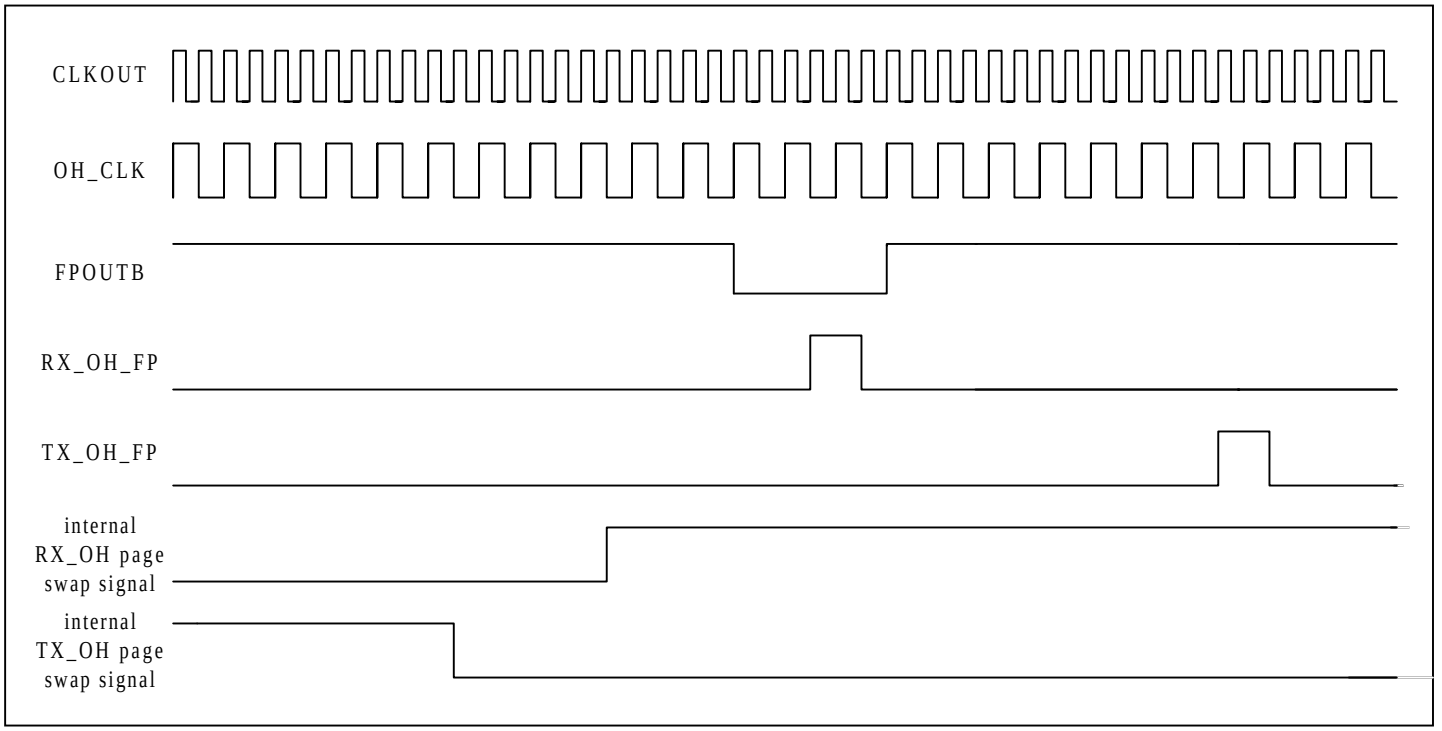
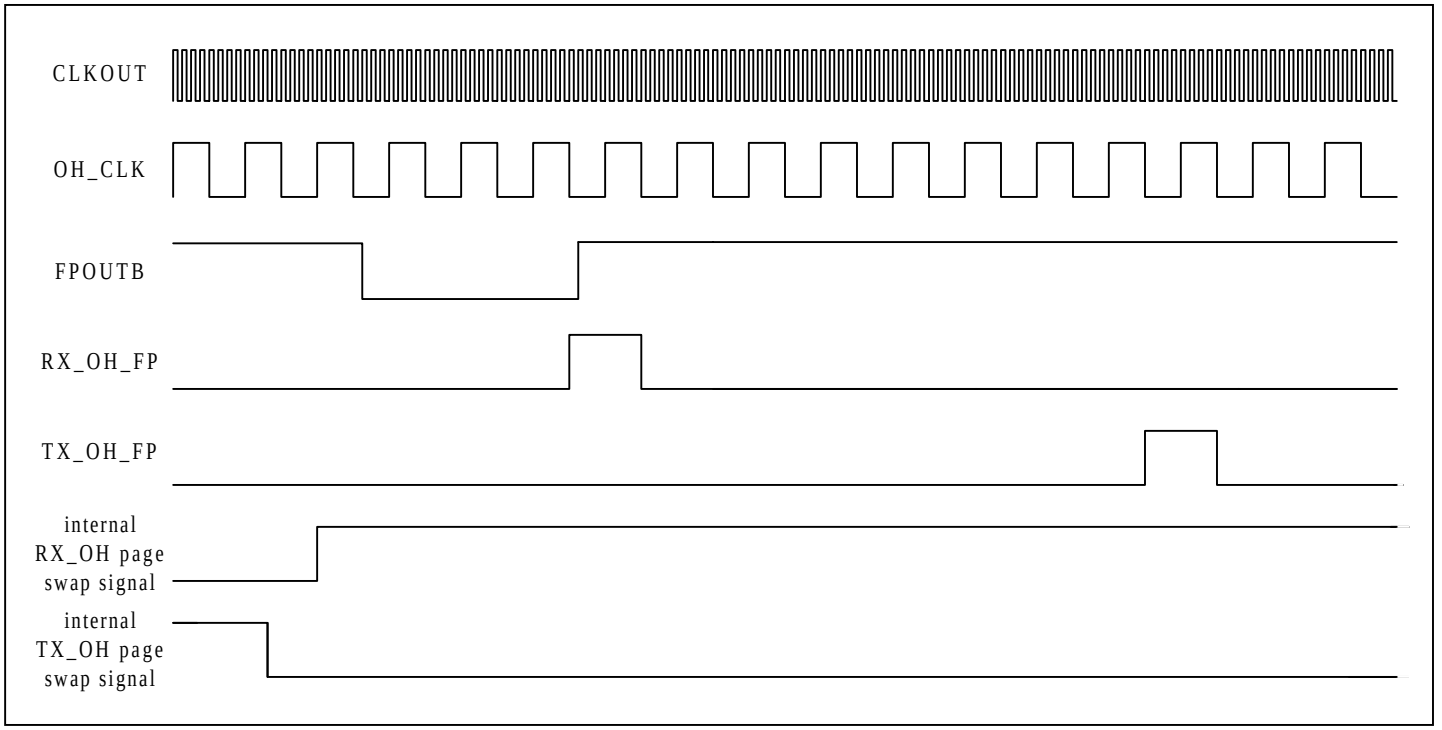


Figure 39 STS-48/STM-16 RX_OH and TX_OH Page Swaps with Respect to Frame Pulses and Clocks



6.7 MPC860 Port AC Timing Characteristics

Table 98 MPC860 Port AC Timing: Set-Up, Hold, Propagation Delay and Cycle Time

Symbol	Description	Min	Max	Units
tCK_{PROC}	Cycle Time: PCLK	20	40	ns
tSE_{PROC}	Set-up Time: Processor Interface Input w.r.t PCK rising	2.5		ns
tHO_{PROC}	Hold Time: Processor Interface Input w.r.t PCK rising	1.0		ns
tP_{PROC}	{Propagation Delay: PCLK rising to Processor Interface Output			
	- PDAT	1.53	8.19	
	- PTA	1.51	6.96	ns
	- PINT	1.46	7.00	

1. All measurements of outgoing signals are assumed to have an output load of 25pF.
2. The required timings for the processor interface signals with respect to PCLK is shown in Figure 40 below.
3. The required timings for the processor interface signals with respect to a processor cycle is shown in the following figures.

Figure 40 MPC860 Port AC Timing Diagram

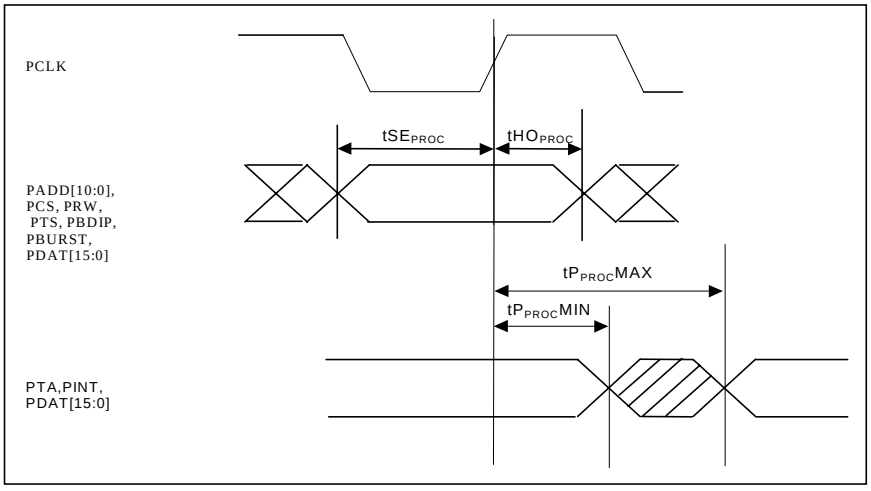


Figure 41 Processor Interface Single Beat Read Timing

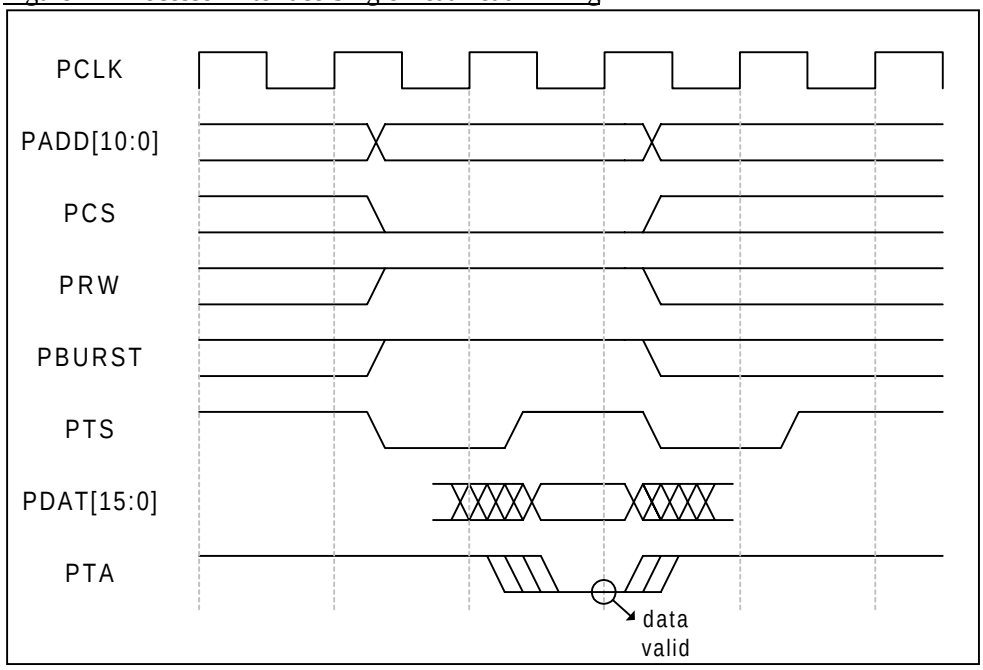


Figure 42 Processor Interface Single Beat Write Timing

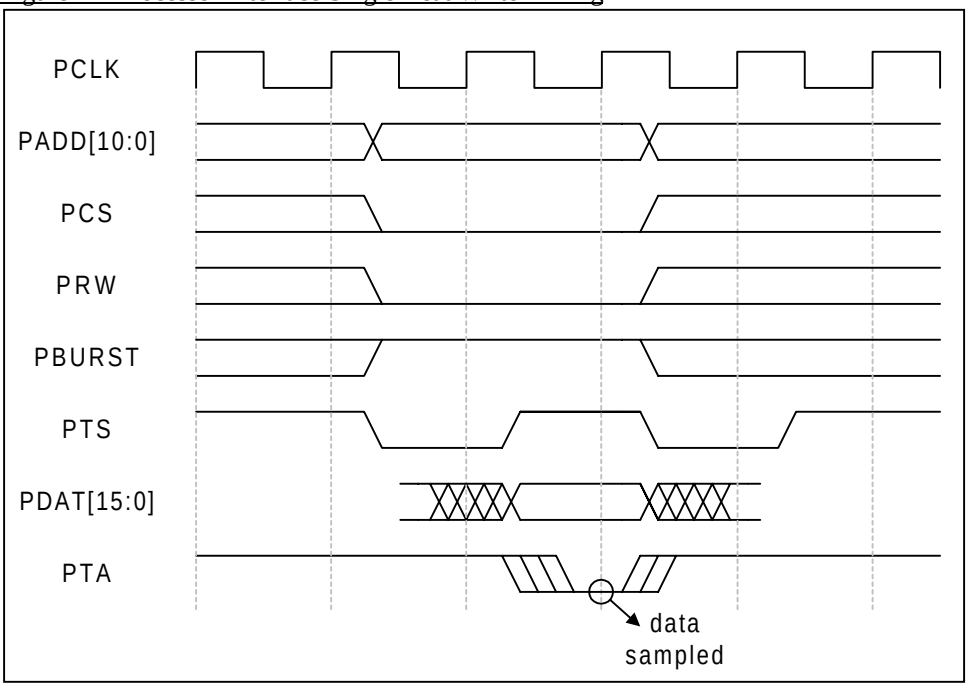


Figure 43 Processor Interface Burst Read Timing

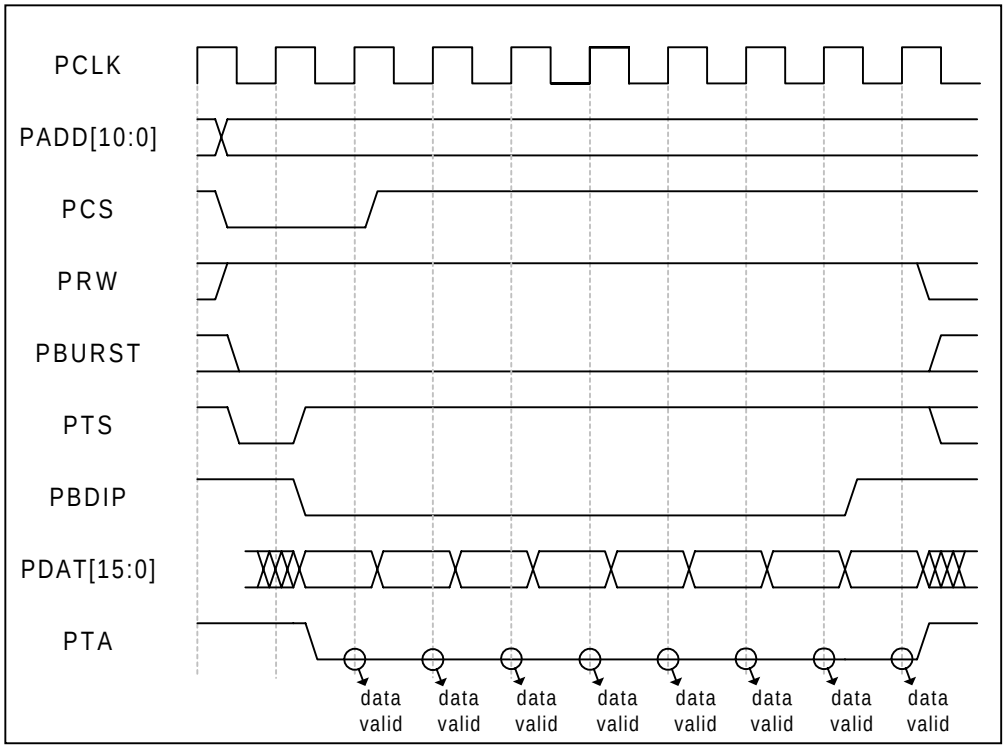
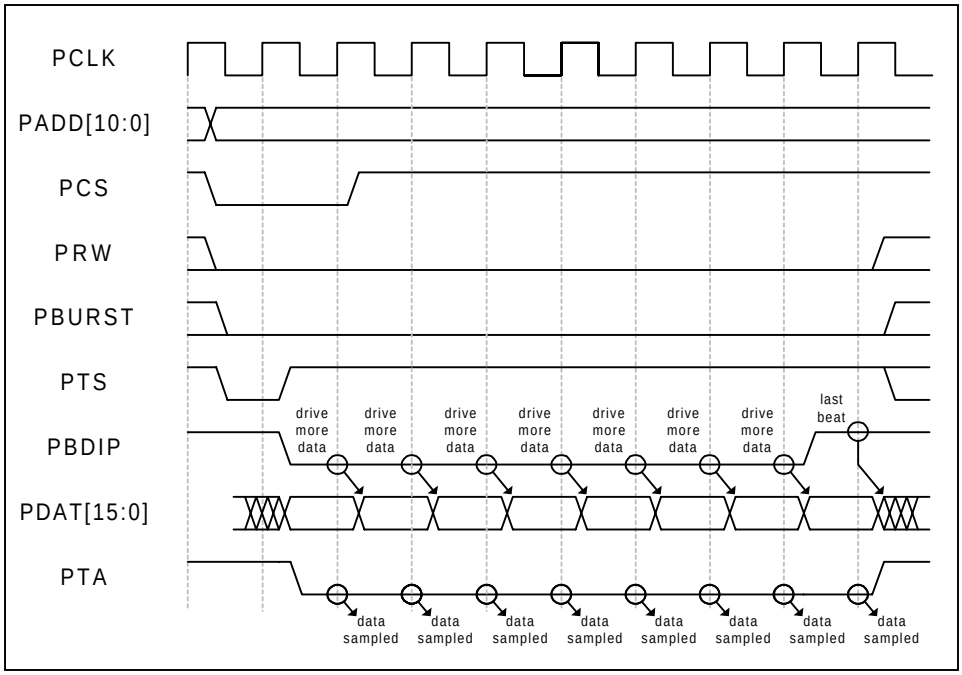


Figure 44 Processor Interface Burst Write Timing



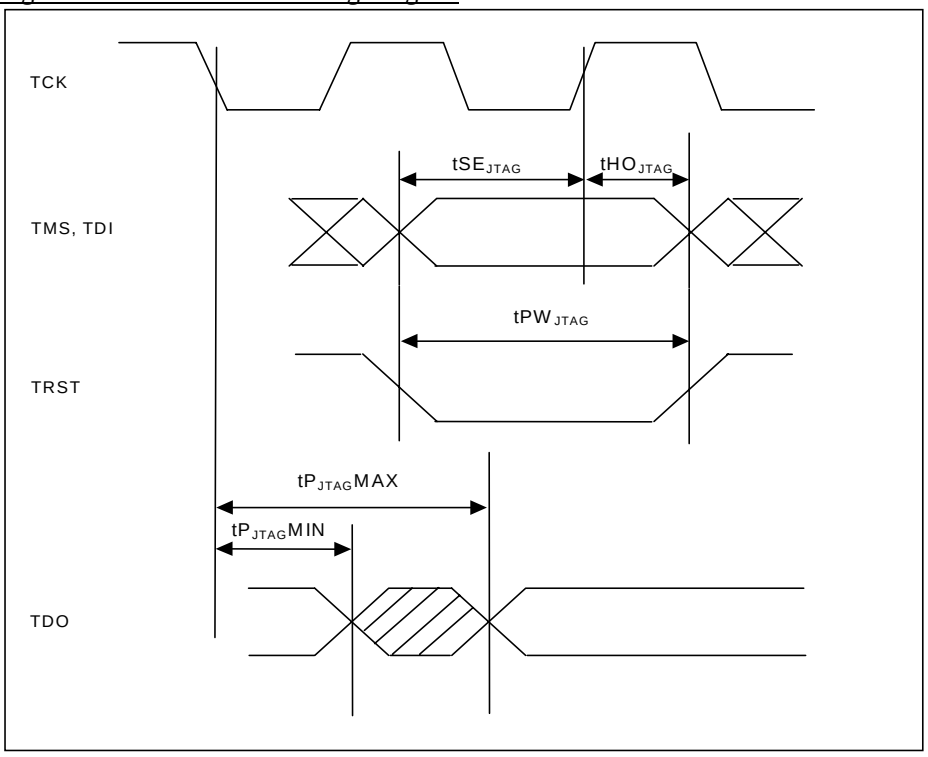
6.8 JTAG Port AC Timing Characteristics

Table 99 JTAG Port AC Timing: Set-Up, Hold, Propagation Delay, Pulse Width and Cycle Time

Symbol	Description	Min	Max	Units
tCK_{cycle}	Cycle Time: TCK	100		ns
tSE_{JTAG}	Set-up Time: TMS, TDI w.r.t TCK rising	20		ns
tHO_{JTAG}	Hold Time: TMS, TDI w.r.t TCK rising	20		ns
tPW_{JTAG}	Pulse Width: TRST	100		ns
tP_{JTAG}	Propagation Delay: TCK falling to TDO	1.0	7.4	ns

1. All measurements of outgoing signals are assumed to have an output load of 25pF.

Figure 45 JTAG Port AC Timing Diagram



6.9 Data Latency through the S3062

Table 100 Data Latency through the S3062 with Various FEC Modes Enabled

	Mode	Latency in terms of number of CLKINP/N ticks
A	Decode FEC only	1259 to 1299 ticks
B	Decode FEC and Encode FEC	1261 to 1301
C	Decode FEC and SONET monitoring	10 ticks more than A: 1269 to 1309 ticks
D	Decode FEC, SONET monitoring and Encode FEC	10 ticks more than B: 1271 to 1311 ticks
E	Encode FEC only	247 to 287 ticks
F	SONET monitoring and Encode FEC	10 ticks more than E: 257 to 297 ticks

7 ERRATA LIST

NOTE: Multiple revisions of silicon are available for the S3062. Each listed errata contains a record of the affected part numbers for that errata item. Please consult this list to determine the part number revision that will suit your application.

7.1 FPOUTB

DESCRIPTION OF PROBLEM
During the active time of the FPOUTB signal, the FPOUTB signal toggles if the FEC Encoder is enabled. These transitions ONLY occur in the active region of the FPOUTB signal.

CONSEQUENCE OF PROBLEM
Edge triggered logic using the FPOUTB pulse will NOT be able to trigger only on the first rising edge since more than one rising edge will occur during the active region after the frame pulse has gone active.

AFFECTED AMCC PART NUMBER
S3062TB

AFFECTED S3062 DATA SHEET REQUIREMENT
Figure 26 FPOUTB Timing Diagram
LOCATION: S3062 DATA SHEET, REV D (November 29, 2000), Section 6.2, Page 118 of 136

7.2 OOF/LOF

DESCRIPTION OF PROBLEM
The previous version of the OOF/LOF state machine created several conditions that make the S3062 OOF/LOF state machine non-SONET/SDH compliant.

CONSEQUENCE OF PROBLEM
This is a non-compliance with the SONET/SDH standards, however, the specific cases may never occur in a network.

AFFECTED AMCC PART NUMBER
S3062TB

AFFECTED S3062 DATA SHEET REQUIREMENT
"Bellcore, ITU-T and IEEE compliant"
LOCATION: S3062 DATA SHEET, REV D, (November 29, 2000), Section 1.2 Features, Page 8 of 136
Figure 17 LOF and OOF (SEF) State Machine Diagram
LOCATION: S3062 DATA SHEET, REV D (November 29, 2000), Figure 17, Page 34 of 136

7.3 Differential Encode Enable

DESCRIPTION OF PROBLEM
The Micro Present byte in ADDR=0x001: Global Control register, must be loaded with a value of 59h for the Differential Encode enable bit to take affect.

CONSEQUENCE OF PROBLEM
The user must be aware of the state of the Micro Present byte when setting this bit.

AFFECTED AMCC PART NUMBER
S3062TB

AFFECTED S3062 DATA SHEET REQUIREMENT
Table 54 ADDR=0x02B: Encoding and Decoding General Controls
LOCATION: S3062 DATA SHEET, REV D (November 29, 2000), Section 3.7.5, Page 77 of 136

7.4 AUTOAIS

DESCRIPTION OF PROBLEM
If AUTOAIS is active, the current silicon does not send out a valid SONET frame (valid A1A2, B1) when the AIS_L is inserted.

CONSEQUENCE OF PROBLEM
When a LOS or LOF is detected, the user must enable FIXSOH to allow the downstream devices to recover the AIS_L indication. A string of unscrambled zeros will be contained in the J0/Z0 registers if a LOS was the cause of the AIS_L alarm. FIXSOH must NOT be enabled when exiting a hardware reset while in OC-48 mode or OOF/LOF alarms will appear downstream.

AFFECTED AMCC PART NUMBER
S3062TB

AFFECTED S3062 DATA SHEET REQUIREMENT
"If a LOS or LOF has been detected and automatic AIS insertion has been selected, the section overhead bytes A1, A2 and B1 will be recalculated and the entire line overhead and payload will be replaced with 1s."
LOCATION: S3062 DATA SHEET, REV D (November 29, 2000), Section 3.3.1.9:Paragraph 1, Page 38 of 136

7.5 FIFO Recentering

DESCRIPTION OF PROBLEM
If the input clocks to the S3062 are unstable for an extended period of time, a condition may occur that will leave the internal S3062 FIFO without the ability to recenter. Constant address collisions will occur, creating bit errors for downstream equipment.

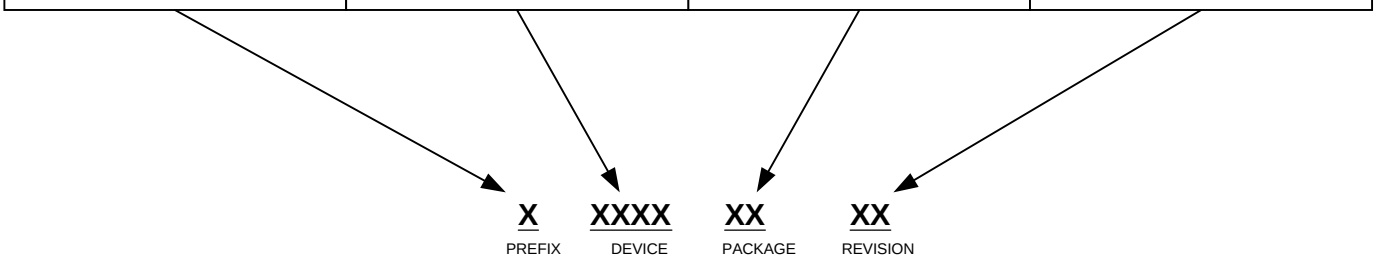
CONSEQUENCE OF PROBLEM
A hardware reset will have to implemented to recenter the FIFO. This will push the FIFO addresses 180 apart, clearing the errored condition.

AFFECTED AMCC PART NUMBER
S3062TB, S3062TB20

AFFECTED S3062 DATA SHEET REQUIREMENT
"However, if the addresses do come within 2 to 6 addresses of each other, the S3062 will force them back apart …"
LOCATION: S3062 DATA SHEET, REV D (November 29, 2000), Section 3.1.4:Paragraph 6, Page 19 of 136

8 ORDERING INFORMATION

PREFIX	DEVICE	PACKAGE	REVISION
S - Integrated Circuit	3062	TB - 352 SBGA	Blank - Consult Errata 7.1 - 7.5 20 - Consult Errata 7.5 21 - No Errata



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