



3.3V CMOS 1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH16832 ADVANCE INFORMATION

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{sk(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.50mm pitch TSSOP package
- Extended commercial range of -40°C to +85°C
- $V_{cc} = 3.3V \pm 0.3V$, Normal Range
- $V_{cc} = 2.7V$ to 3.6V, Extended Range
- $V_{cc} = 2.5V \pm 0.2V$
- CMOS power levels (0.4μW typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH16832:

- High Output Drivers: ±24mA
- Suitable for heavy loads

APPLICATIONS:

- Memory subsystems
- PC motherboards and servers
- Workstations
- Telecommunication applications

DESCRIPTION:

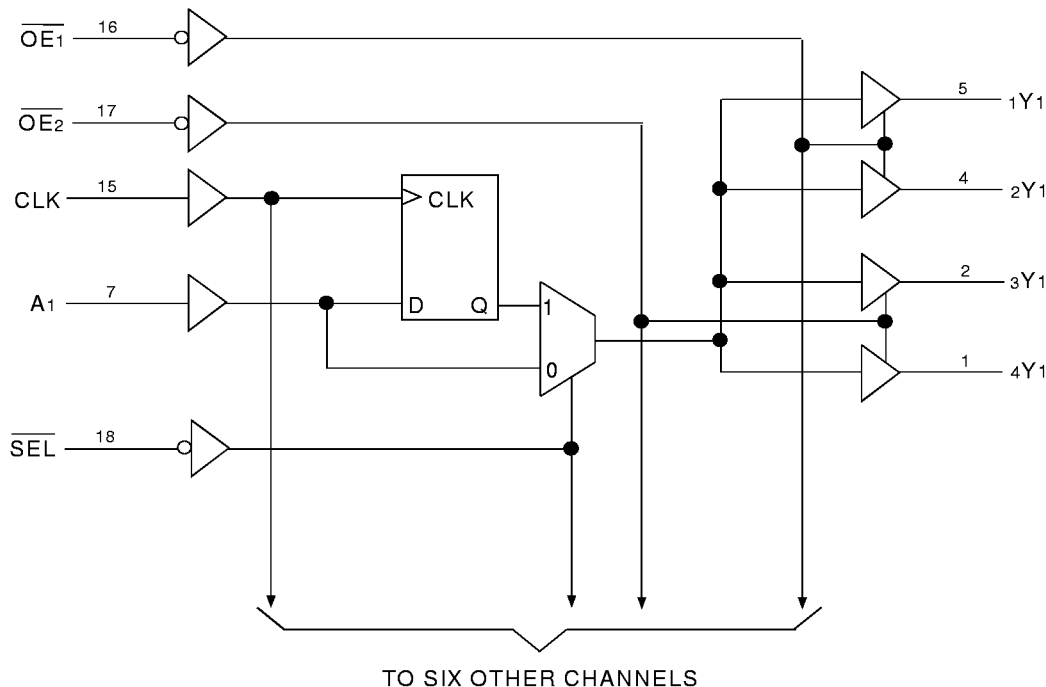
This 1-bit to 4-bit address register/driver is built using advanced dual metal CMOS technology. This device is ideal for use in applications in which a single address bus is driving four separate memory locations. The ALVCH16832 can be used as a buffer or a register, depending on the logic level of the select (\overline{SEL}) input.

When \overline{SEL} is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output-enable (\overline{OE}) controls. Each \overline{OE} controls two groups of seven outputs. When \overline{SEL} is logic low, the device is in the register mode. The register is an edge-triggered D-type flip-flop. On the positive transition of the clock (CLK) input, data at the A inputs is stored in the internal registers. \overline{OE} controls operate the same as in buffer mode.

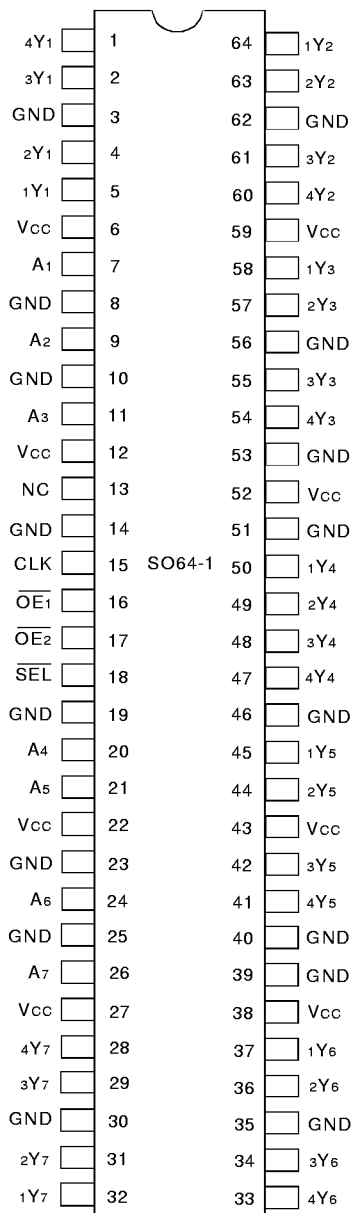
The ALVCH16832 has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

The ALVCH16832 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

Functional Block Diagram



PIN CONFIGURATION



TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}x$	3-State Output Enable Inputs (Active LOW)
CLK	Register Input Clock
\overline{SEL}	Select Input (Active LOW)
Ax	Data Inputs ⁽¹⁾
xYx	3-State Outputs
NC	No Internal Connection

NOTE:

1. These pins have "Bus-hold". All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	- 0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	- 65 to + 150	°C
I _{OUT}	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I _{OK}	Continuous Clamp Current, $V_O < 0$	- 50	mA
I _{CC} I _{SS}	Continuous Current through each Vcc or GND	±100	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. All terminals except Vcc.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$	5	7	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0V$	7	9	pF
C _{I/O}	I/O Port Capacitance	$V_{IN} = 0V$	7	9	pF

NOTE:

1. As applicable to the device type.

FUNCTION TABLE (1)

Inputs				Outputs
$\overline{OE}x$	\overline{SEL}	CLK	Ax	xYx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

NOTE:

1. H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH transition

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = -40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V _{IH}	Input HIGH Voltage Level	V _{CC} = 2.3V to 2.7V		1.7	—	—	V
		V _{CC} = 2.7V to 3.6V		2	—	—	
V _{IL}	Input LOW Voltage Level	V _{CC} = 2.3V to 2.7V		—	—	0.7	V
		V _{CC} = 2.7V to 3.6V		—	—	0.8	
I _{IH}	Input HIGH Current	V _{CC} = 3.6V	V _I = V _{CC}	—	—	± 5	μA
I _{IL}	Input LOW Current	V _{CC} = 3.6V	V _I = GND	—	—	± 5	
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = 3.6V	V _O = V _{CC}	—	—	± 10	μA
I _{OZL}			V _O = GND	—	—	± 10	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = 2.3V, I _{IN} = -18mA		—	-0.7	-1.2	V
V _H	Input Hysteresis	V _{CC} = 3.3V		—	100	—	mV
I _{CCL}	Quiescent Power Supply Current	V _{CC} = 3.6V		—	0.1	40	μA
I _{CCH}		V _{IN} = GND or V _{CC}		—			
I _{CCZ}				—			
ΔI _{CC}	Quiescent Power Supply Current Variation	One input at V _{CC} - 0.6V, other inputs at V _{CC} or GND		—	—	750	μA

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NOTE:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
I _{BHH}	Bus-Hold Input Sustain Current	V _{CC} = 3.0V	V _I = 2.0V	-75	—	—	μA
			V _I = 0.8V	75	—	—	
I _{BHL}	Bus-Hold Input Sustain Current	V _{CC} = 2.3V	V _I = 1.7V	-45	—	—	μA
			V _I = 0.7V	45	—	—	
I _{BHNO}	Bus-Hold Input Overdrive Current	V _{CC} = 3.6V	V _I = 0 to 3.6V	—	—	± 500	μA
I _{BHLO}							

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NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
VOH	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = -0.1mA	V _{CC} - 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = -6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = -12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = -24mA	2	—	
VOL	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = -40°C to +85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	V _{CC} = 2.5V ± 0.2V	V _{CC} = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance per register/driver Outputs enabled	C _L = 0pF, f = 10MHz	119	132	pF
CPD	Power Dissipation Capacitance per register/driver Outputs disabled		22	25	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	V _{CC} = 2.5V ± 0.2V		V _{CC} = 2.7V		V _{CC} = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f _{MAX}		150	—	150	—	150	—	MHz
t _{PLH} t _{PHL}	Propagation Delay A _x to xY _x	1.2	4	—	4.1	1.6	3.6	ns
t _{PLH} t _{PHL}	Propagation Delay CLK to xY _x	1.1	4.5	—	4.4	1.5	3.9	ns
t _{PLH} t _{PHL}	Propagation Delay $\overline{\text{SEL}}$ to xY _x	1.3	5.2	—	5.2	1.7	4.4	ns
t _{PZH} t _{PZL}	Output Enable Time $\overline{\text{OEx}}$ to xY _x	1.1	5.1	—	5	1.2	4.3	ns
t _{PHZ} t _{PLZ}	Output Disable Time $\overline{\text{OEx}}$ to xY _x	1.4	5.5	—	4.7	1.6	4.5	ns
t _w	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
t _{SU}	Setup Time, A _x data before CLK↑	2	—	2	—	1.6	—	ns
t _H	Hold Time, A _x data after CLK↑	0.7	—	0.5	—	1.1	—	ns
t _{SK(o)}	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

- See test circuits and waveforms. T_A = -40°C to +85°C.
- Skew between any two outputs of the same package and switching in the same direction.

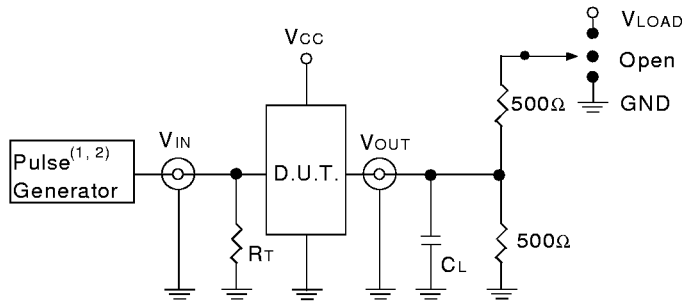
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{cc} (1)= 3.3V±0.3V	V _{cc} (1)= 2.7V	V _{cc} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{cc}	V
V _{IH}	2.7	2.7	V _{cc}	V
V _T	1.5	1.5	V _{cc} /2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

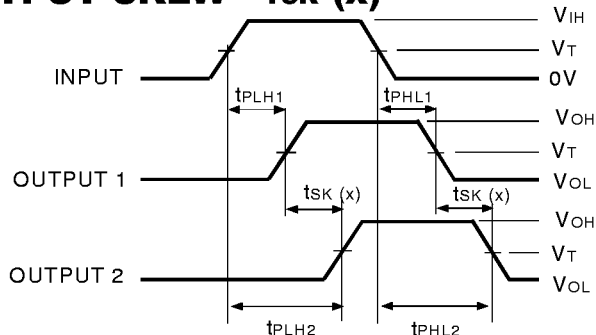
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)



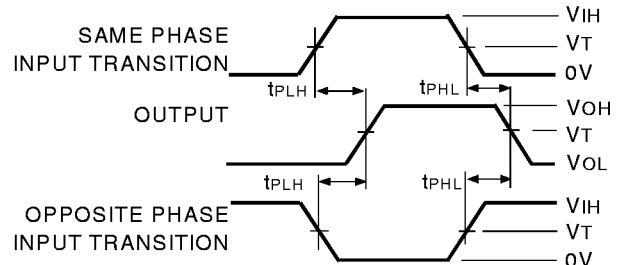
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

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NOTES:

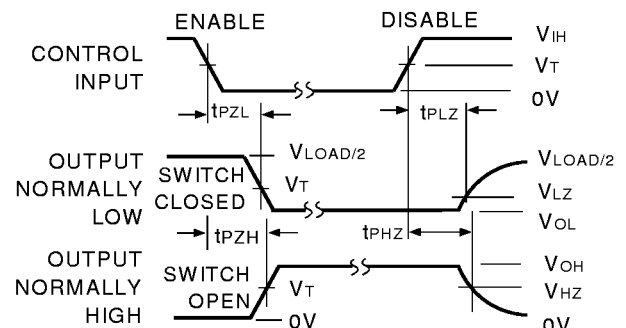
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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ENABLE AND DISABLE TIMES

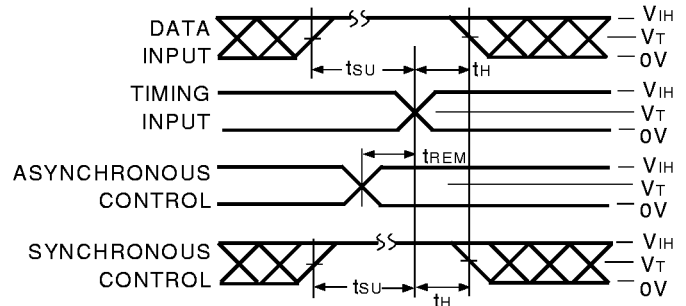


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NOTE:

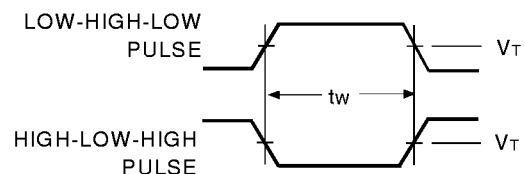
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



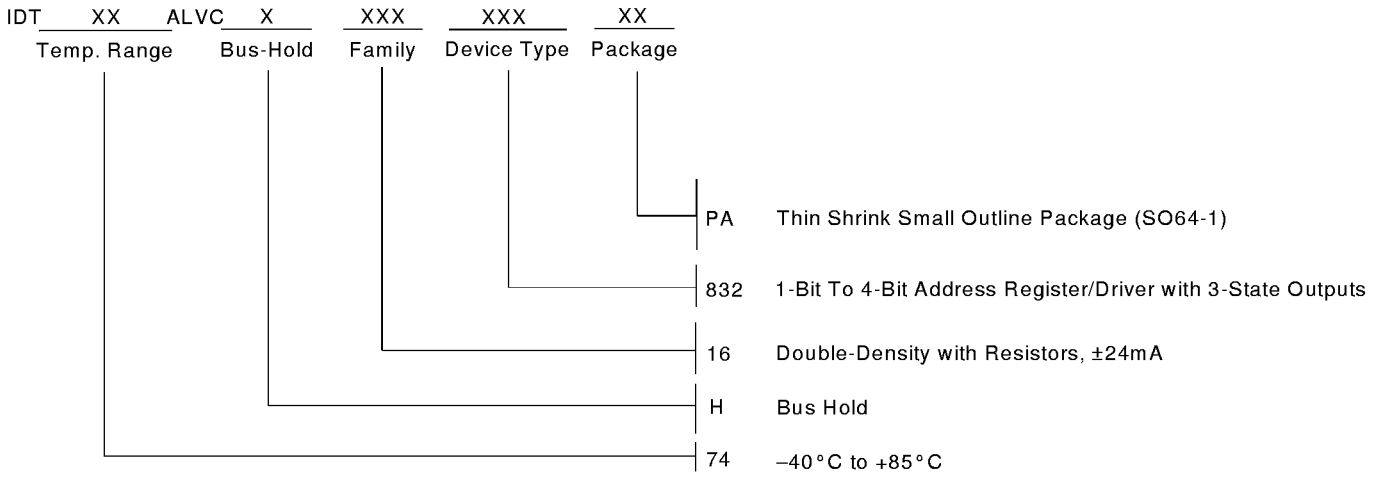
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PULSE WIDTH



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ORDERING INFORMATION



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