

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	29F(U.L.) HIGH/LOW
AC ₀ -AC ₈	Column Address	0.5/0.375
AR ₀ -AR ₈	Row Address	0.5/0.375
Q ₀ -Q ₈	Address Output	25/12.5
MC ₀ ,MC ₁	Memory Cycle	0.5/0.375
\overline{CS}	Chip Select Input	0.5/0.375
MSEL	Memory Select Input	0.5/0.375
LE	Latch Enable Input	0.5/0.375
SEL ₀ ,SEL ₁	Select Inputs	0.5/0.375
RASI	Row Address Strobe In	0.5/0.375
CASI	Column Address Strobe In	0.5/0.375
\overline{RAS}_0 - \overline{RAS}_3	Row Address Strobe Output	25/12.5
\overline{CAS}_0 - \overline{CAS}_3	Column Address Strobe Output	25/12.5
\overline{OE}	Output Enable	0.5/0.375

Functional Description

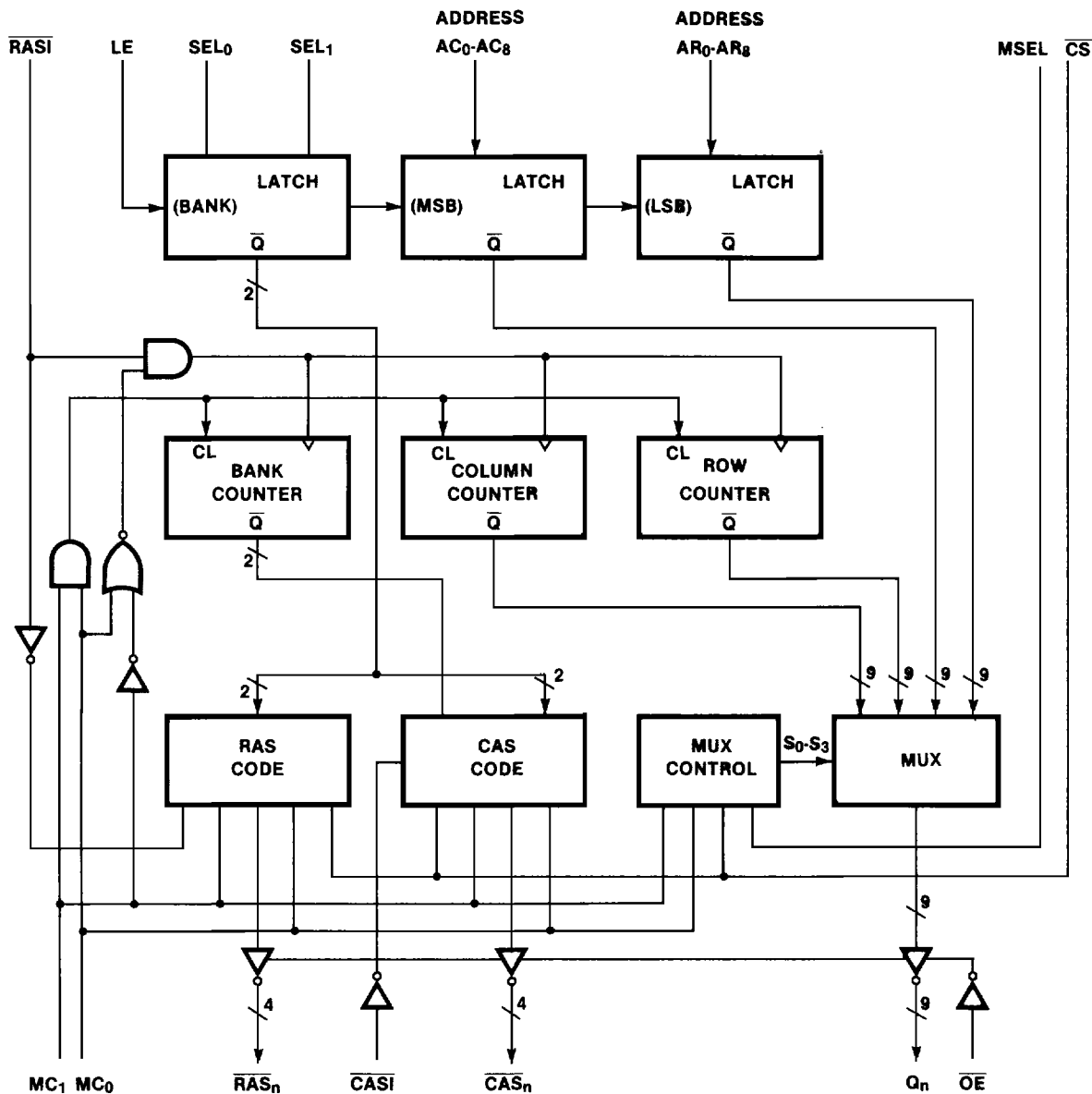
The 29F68 is designed to be used with 16K, 64K or 256K dynamic RAMs. The two 9-bit address latches are used to store row and column addresses provided by the I/O processor while the 2-bit latch is used to select one each of the four RAS and CAS outputs.

In the refresh mode, two counters cycle through the refresh address. Only the row address is used for normal 'RAS-only' refreshing or refresh without scrubbing, generating up to 512 addresses to refresh 512-cycle-refresh dynamic RAM. The column counter is used only for refresh with scrubbing. In this mode all RAS outputs are generated with only one CAS output.

Mode Control Function Table

MC ₁	MC ₀	Operating Mode
0	0	Refresh without Scrubbing —Refresh cycles are performed with only the Row Counter being used to generate addresses. In this mode, all four \overline{RAS}_i outputs are active while the four \overline{CAS}_i signals are kept HIGH.
0	1	Refresh with Scrubbing/Initialize —During this mode, refresh cycles are done with both the Row and Column counters generating the addresses. MSEL is used to select between the Row and Column counter. All four \overline{RAS}_i go active in response to RASI, while only one \overline{CAS}_i output goes LOW in response to CASI. The Bank Counter keeps track of which \overline{CAS}_i output will go active. This mode is also used on system power-up so that the memory can be written with a known data pattern.
1	0	Read/Write —This mode is used to perform Read/Write cycles. Both the Row and Column addresses are latched and multiplexed to the address output lines using MSEL; SEL ₀ and SEL ₁ are decoded to determine which \overline{RAS}_i and \overline{CAS}_i will be active.
1	1	Clear Refresh Counter —This mode will clear the three refresh counters (Row, Column, and Bank) on the HIGH-to-LOW transition of RASI, putting them at the start of the refresh sequence. In this mode, all four \overline{RAS}_i are driven LOW upon receipt of RASI so that DRAM wake-up cycles may be performed.

Block Diagram



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Address Output Function Table

\overline{CS}	MC_1	MC_0	MSEL	Mode	MUX Output
0	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	1	Read/Write	Column Address Latch
			0		Row Address Latch
1	1	X	Clear Refresh Counter	Zero	
1	0	0	X	Refresh without Scrubbing	Row Counter Address
	0	1	1	Refresh with Scrubbing	Column Counter Address
			0		Row Counter Address
	1	0	X	Read/Write	Zero
	1	1	X	Clear Refresh Counter	Zero

RAS Output Function Table

RASI	\overline{CS}	MC_1	MC_0	SEL_1	SEL_0	Mode	\overline{RAS}_0	\overline{RAS}_1	\overline{RAS}_2		
0	X	X	X	X	X		X	1	1	1	
1	0	0	0	X	X	Refresh without Scrubbing	0	0	0	0	
						Refresh with Scrubbing	0	0	0	0	
		1	0	0	0	0	1	Read/Write	0	1	1
									1	0	1
									1	0	0
		1	1	1	X	X	X	Clear Refresh Counter	0	0	0
									0	0	0
	1	1	0	0	X	X	Refresh without Scrubbing	0	0	0	
							Refresh with Scrubbing	0	0	0	
							Read/Write	1	1	1	
Clear Refresh Counter							0	0	0		

CAS[̄] Output Function Table

CAS [̄]	CS [̄]	MC ₁	MC ₀	CNTR ₁	CNTR ₀	SEL ₁	SEL ₀	CAS ₀ [̄]	CAS ₁ [̄]	CAS ₂ [̄]	CAS ₃ [̄]		
1	0	0	0	X	X	X	X	1	1	1	1		
				0	0			0	1	1	1		
		0	1	1	1	0	1	X	X	1	0	1	1
						1	0			1	1	0	1
						1	1			1	1	1	0
						0	0			0	1	1	1
		1	0	0	X	X	0	0	0	1	1	1	
							0	1	1	0	1	1	
							1	0	1	1	0	1	
							1	1	1	1	1	0	
	1	1	1	X	X	X	X	1	1	1	1		
						X	X	1	1	1	1		
		0	0	1	1	0	0	X	X	0	1	1	1
						0	1			1	0	1	1
						1	0			1	1	0	1
						1	1			1	1	1	0
		1	0	0	X	X	X	X	1	1	1	1	
							1	1	1	1	1	1	
0	X	X	X	X	X	X	1	1	1	1			

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DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	29F			Units	Conditions
		Min	Typ	Max		
I _{CC}	Power Supply Current				mA	V _{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	29F			Military 29F		Commercial 29F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} =$ Mil $C_L = 50\text{ pF}$		$T_A, V_{CC} =$ Com $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	11.0 11.0							ns
t_{PLH} t_{PHL}	Propagation Delay RAS_i to \overline{RAS}_i	9.0 9.0							ns
t_{PLH} t_{PHL}	Propagation Delay CAS_i to \overline{CAS}_i	9.0 9.0							ns
t_{PLH} t_{PHL}	Propagation Delay MSEL to Q	9.0 9.0							ns
t_{PLH} t_{PHL}	Propagation Delay MC_i to Q	12.0 12.0							ns
t_{PLH} t_{PHL}	Propagation Delay LE to \overline{RAS}_i	12.0 12.0							ns
t_{PLH} t_{PHL}	Propagation Delay LE to \overline{CAS}_i	12.0 12.0							ns
t_{PLH} t_{PHL}	Propagation Delay MC_i to \overline{RAS}_i	9.0 9.0							ns
t_{PLH} t_{PHL}	Propagation Delay MC_i to \overline{CAS}_i	9.0 9.0							ns
t_{PLH} t_{PHL}	Propagation Delay LE to Q_n	11.0 11.0							ns
t_{PHZ} t_{PLZ}	Output Enable Time \overline{OE} to Q_n, \overline{RAS}_i or \overline{CAS}_i	5.0 5.0							ns
t_{PZH} t_{PZL}	Output Disable Time \overline{OE} to Q_n, \overline{RAS}_i or \overline{CAS}_i	10.0 10.0							ns
$t_w(H)$ $t_w(L)$	\overline{RAS}_i or \overline{CAS}_i Pulse Width HIGH or LOW								ns

AC Characteristics (Cont'd)

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 50\text{ pF}$	$T_A, V_{CC} =$ Mil $C_L = 50\text{ pF}$	$T_A, V_{CC} =$ Com $C_L = 50\text{ pF}$	
		Min Typ Max	Min Max	Min Max	
t_{DHL} t_{DLH}	Skew Q_n to \overline{RAS}_i MC = 10				ns
t_{DHL} t_{DLH}	Skew Q_n to \overline{RAS}_i MC = 00, 01				ns
t_{DHL} t_{DLH}	Skew Q_n to \overline{RAS}_i				ns
t_{DHL} t_{DLH}	Skew Q_n to \overline{CAS}_i				ns

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AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 500\text{ pF}$	$T_A, V_{CC} =$ Mil $C_L = 500\text{ pF}$	$T_A, V_{CC} =$ Com $C_L = 500\text{ pF}$	
		Min Typ Max	Min Max	Min Max	
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	14.0 14.0			ns
t_{PLH} t_{PHL}	Propagation Delay RAS_i to \overline{RAS}_i	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay CAS_i to \overline{CAS}_i	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay MSEL to Q	12.0 12.0			ns
t_{PLH} t_{PHL}	Propagation Delay MC_i to Q	15.0 15.0			ns
t_{PLH} t_{PHL}	Propagation Delay LE to \overline{RAS}_i	15.0 15.0			ns
t_{PLH} t_{PHL}	Propagation Delay LE to \overline{CAS}_i	15.0 15.0			ns

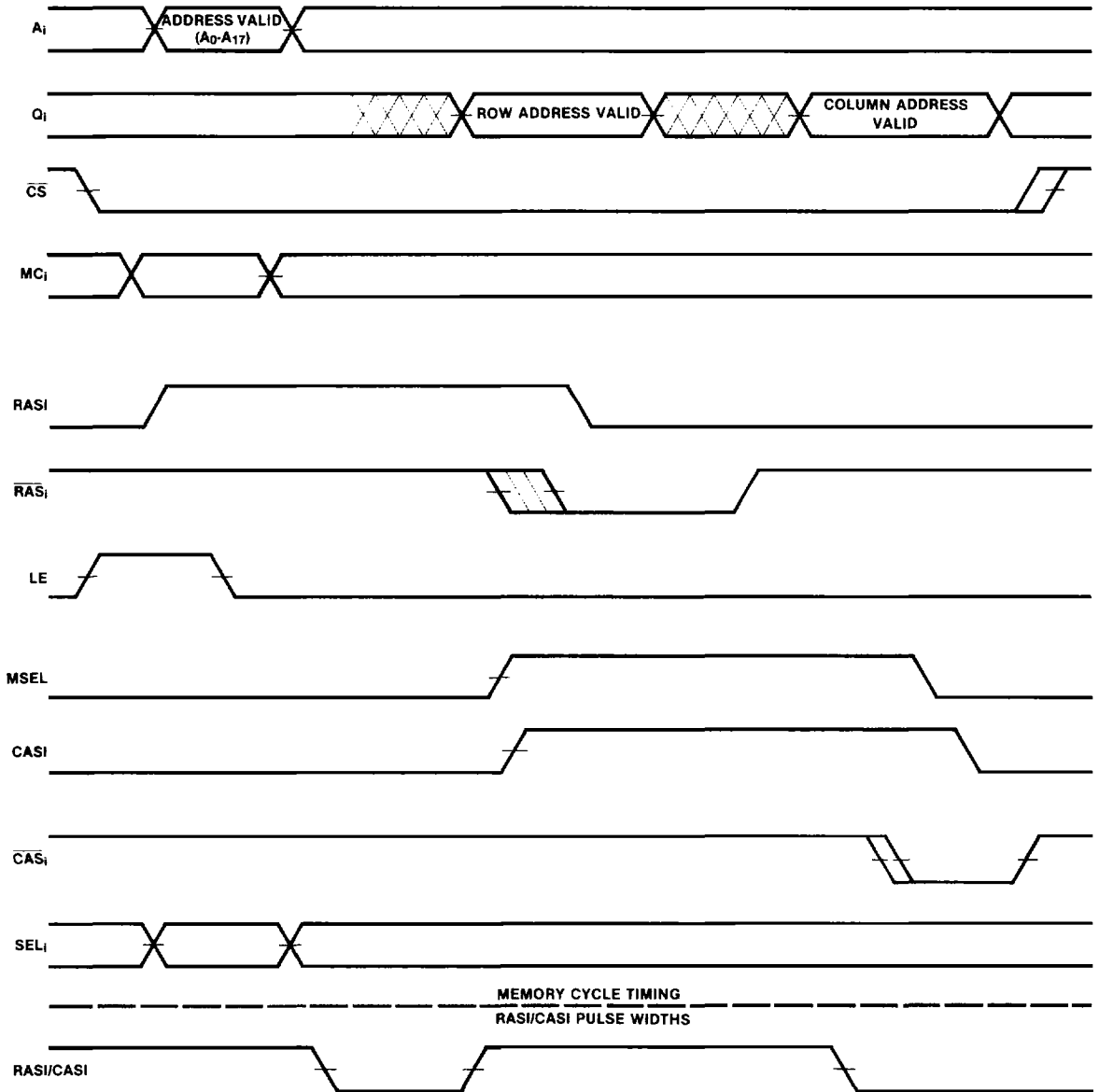
AC Characteristics (Cont'd)

Symbol	Parameter	29F	Military 29F	Commercial 29F	Units	
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$ $C_L = 500\text{ pF}$		$T_A, V_{CC} =$ Mil $C_L = 500\text{ pF}$		$T_A, V_{CC} =$ Com $C_L = 500\text{ pF}$
		Min	Typ	Max		Min
t_{PLH} t_{PHL}	Propagation Delay MC_i to \overline{RAS}_i	12.0			ns	
t_{PLH} t_{PHL}	Propagation Delay MC_i to CAS_i	12.0			ns	
t_{PLH} t_{PHL}	Propagation Delay LE to Q_n	14.0			ns	
t_{PHZ} t_{PLZ}	Output Disable Time \overline{OE} to Q_n, \overline{RAS}_i or CAS_i				ns	
t_{PZH} t_{PZL}	Output Enable Time \overline{OE} to Q_n, \overline{RAS}_i or CAS_i	13.0			ns	
$t_w(H)$ $t_w(L)$	\overline{RAS}_i or CAS_i Pulse Width HIGH or LOW				ns	
t_{DHL} t_{DLH}	Skew Q_n to \overline{RAS}_i MC = 10				ns	
t_{DHL} t_{DLH}	Skew Q_n to \overline{RAS}_i MC = 00, 01				ns	
t_{DHL} t_{DLH}	Skew Q_n to \overline{RAS}_i				ns	
t_{DHL} t_{DLH}	Skew Q_n to \overline{CAS}_i				ns	

AC Operating Requirements: See Section 3 for waveforms

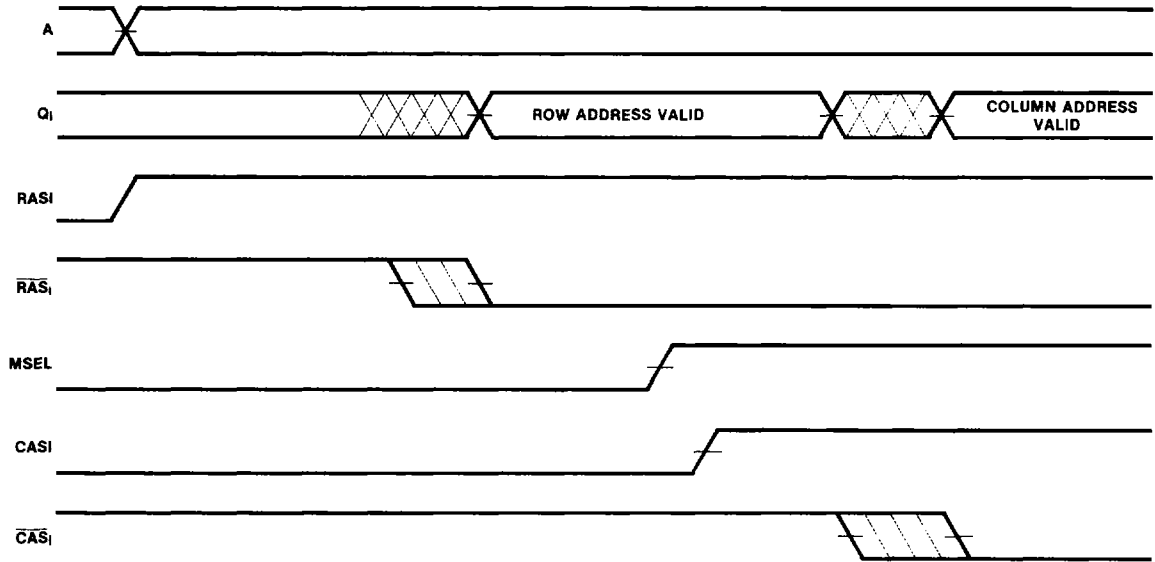
Symbol	Parameter	29F	Military 29F	Commercial 29F	Units	
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{ V}$		$T_A, V_{CC} =$ Mil		$T_A, V_{CC} =$ Com
		Min	Typ	Max		Min
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n to LE	5.0			ns	
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n to LE	5.0			ns	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW \overline{MC}_i to \overline{RAS}_i	10.0			ns	
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW \overline{MC}_i to \overline{RAS}_i	10.0			ns	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SEL to LE	5.0			ns	
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SEL to LE	5.0			ns	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CS to \overline{MC}_i				ns	
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW \overline{CS} to \overline{CAS}_i				ns	

Fig. 68-a Dynamic Memory Controller Timing



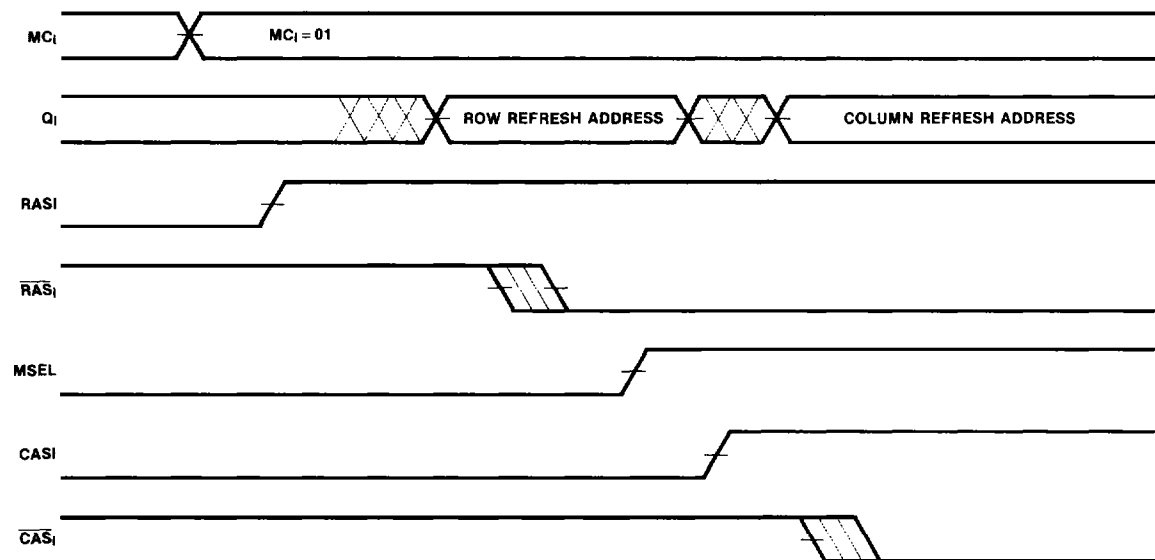
Memory Cycle Timing

Fig. 68-b Specifications Applicable to Memory Cycle Timing



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Fig. 68-c Desired System Timing



Refresh Cycle Timing

Fig. 68-d Specifications Applicable to Refresh Cycle Timing

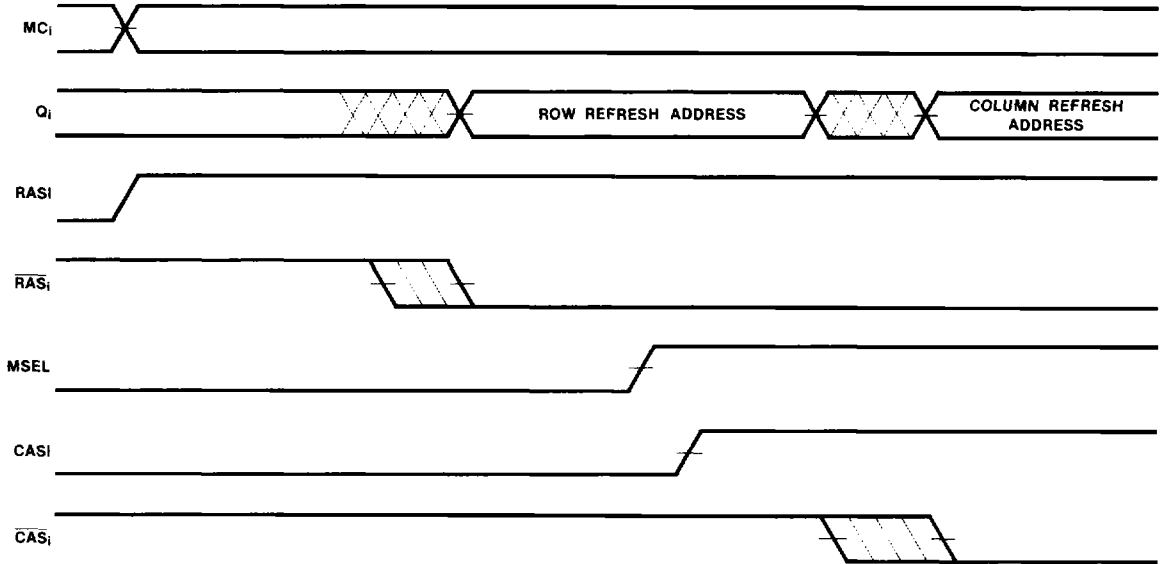


Fig. 68-e Desired Timing: Refresh w/Scrubbing

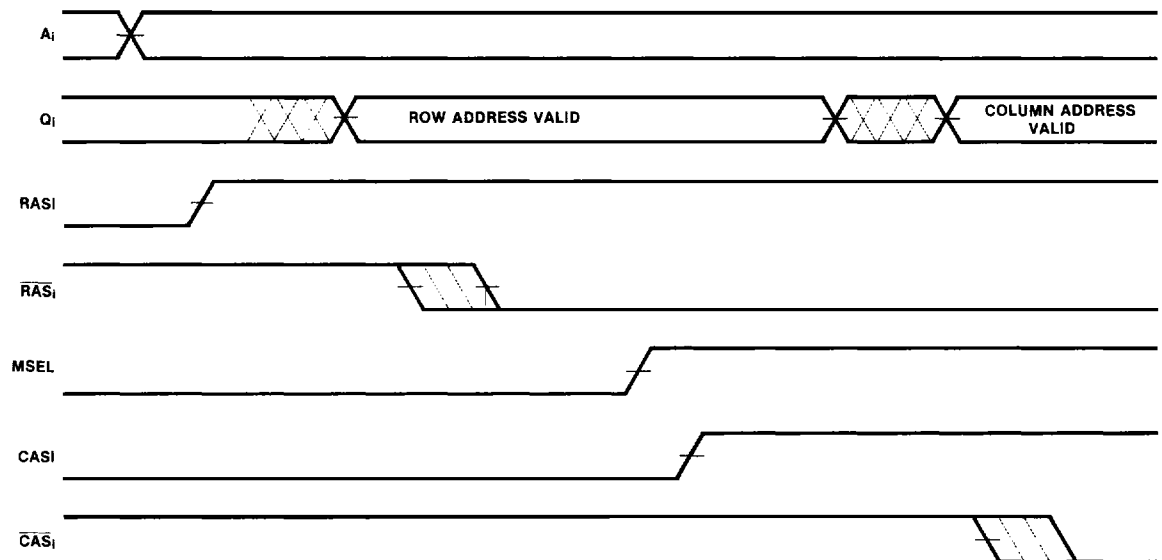


Fig. 68-f Desired Timing: Refresh w/Scrubbing

