# 8/16-bit Data Bus One-Time PROM Card

Connector Type

## Two-piece 68-pin

**MF4257-G1EATXX**
**MF4257-G5EATXX**

**MF4513-G1EATXX**
**MF4513-G5EATXX**

**MF41M1-G1EATXX**
**MF41M1-G5EATXX**

**MF42M1-G1EATXX**
**MF42M1-G5EATXX**

**MF44M1-G1EATXX**
**MF44M1-G5EATXX**

### DESCRIPTION

Mitsubishi's One-Time PROM cards provide large memory capacities on a device approximately the size of a credit card (85.6mm × 54mm × 3.3mm). The cards use a 8/16-bit data bus. Available in 256 KB, 512KB, 1 MB, 2 MB, and 4 MB capacities, Mitsubishi's One-Time PROM cards are available with a 68 pin, two-piece connector.

### FEATURES

- Uses TSOP (Thin Small Outline Package) to achieve very high memory density coupled with high reliability, without enlarging card size
- Electrostatic discharge protection to 15kV
- Buffered interface
- 68-pin connector
- 8/16bit controllable data bus width

### APPLICATIONS

- Office automation
- Computers
- Telecommunications
- Data Communications
- Industrial
- Consumer

### PRODUCT LIST

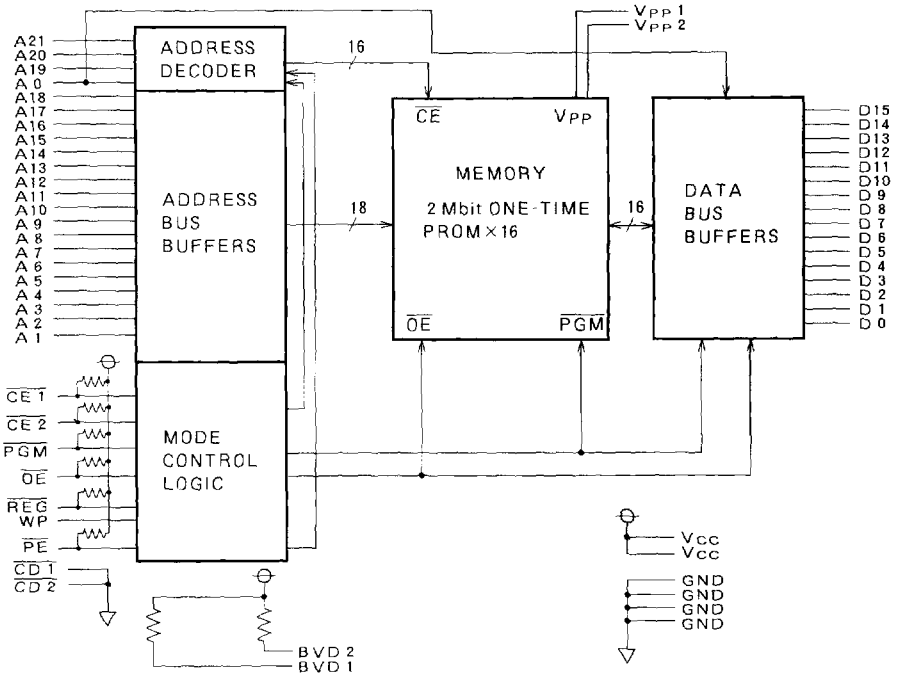
| Item / Type name | Memory capacity | Data bus width (bits) | Access time (ns) | Connector type | Number of pins | Outline drawing |
|---|---|---|---|---|---|---|
| MF4257-G1EATXX | 256KB | 8/16 | 250 | Two-piece | 68 | 68P-001 |
| MF4257-G5EATXX | | | | | | |
| MF4513-G1EATXX | 512KB | | | | | |
| MF4513-G5EATXX | | | | | | |
| MF41M1-G1EATXX | 1 MB | | | | | |
| MF41M1-G5EATXX | | | | | | |
| MF42M1-G1EATXX | 2 MB | | | | | |
| MF42M1-G5EATXX | | | | | | |
| MF44M1-G1EATXX | 4 MB | | | | | |
| MF44M1-G5EATXX | | | | | | |

## PIN ASSIGNMENT

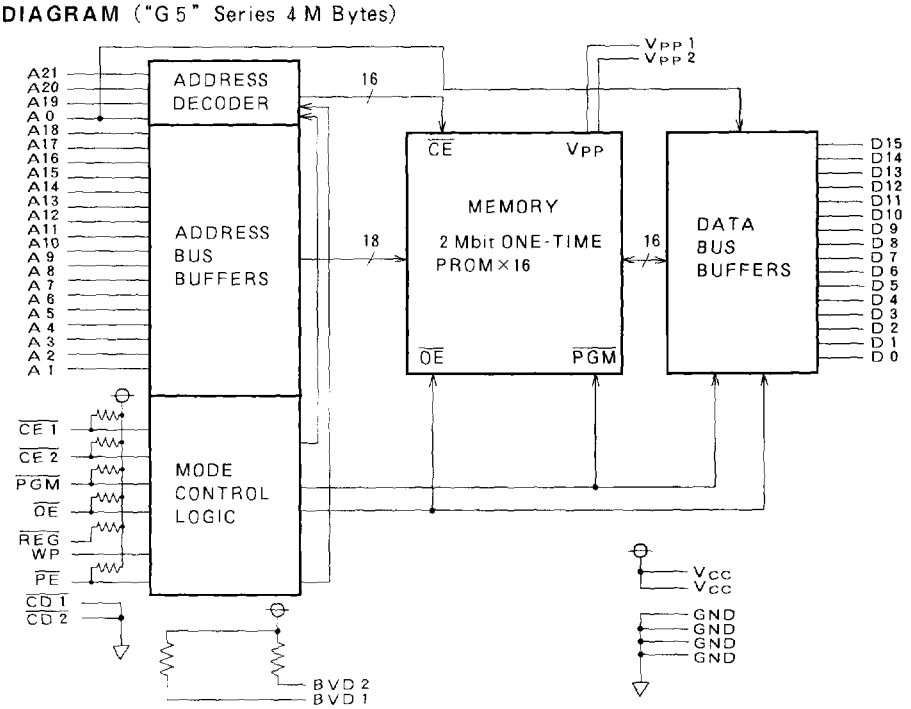
**Two-Piece Type** (68-pin)

| Pin No. | Symbol | Function | Pin No. | Symbol | Function |
|---|---|---|---|---|---|
| 1 | GND | Ground | 35 | GND | Ground |
| 2 | D3 | | 36 | CD1 | Card detect 1 |
| 3 | D4 | | 37 | D11 | |
| 4 | D5 | Data | 38 | D12 | |
| 5 | D6 | | 39 | D13 | Data I/O |
| 6 | D7 | | 40 | D14 | |
| 7 | $\overline{CE1}$ | Card enable 1 | 41 | D15 | |
| 8 | A10 | Address input | 42 | $\overline{CE2}$ | Card enable 2 |
| 9 | $\overline{OE}$ | Output enable | 43 | NC | No connection |
| 10 | A11 | | 44 | $\overline{PE}$ | Program enable |
| 11 | A9 | | 45 | NC | No connection |
| 12 | A8 | Address input | 46 | A17 | A17 (NC for ≤ 128KB types |
| 13 | A13 | | 47 | A18 | A18 (NC for ≤ 256KB types |
| 14 | A14 | | 48 | A19 | A19 (NC for ≤ 512KB types Address input |
| 15 | $\overline{PGM}$ | Program control | 49 | A20 | A20 (NC for ≤ 1 MB types |
| 16 | NC | No connection | 50 | A21 | A21 (NC for ≤ 2 MB types |
| 17 | $V_{CC}$ | Power supply voltage | 51 | $V_{CC}$ | Power supply voltage |
| 18 | $V_{PP}$ 1 | Power supply voltage | 52 | $V_{PP}$ 2 | Power supply voltage |
| 19 | A16 | A16 (NC for 64KB type) | 53 | NC | |
| 20 | A15 | | 54 | NC | |
| 21 | A12 | | 55 | NC | |
| 22 | A7 | | 56 | NC | No connection |
| 23 | A6 | | 57 | NC | |
| 24 | A5 | Address input | 58 | NC | |
| 25 | A4 | | 59 | NC | |
| 26 | A3 | | 60 | NC | |
| 27 | A2 | | 61 | $\overline{REG}$ | REG function |
| 28 | A1 | | 62 | BVD2 | Battery voltage detect 2 |
| 29 | A0 | | 63 | BVD1 | Battery voltage detect 1 |
| 30 | D0 | | 64 | D8 | |
| 31 | D1 | Data I/O | 65 | D9 | Data I/O |
| 32 | D2 | | 66 | D10 | |
| 33 | WP | Write protect | 67 | $\overline{CD2}$ | Card detect 2 |
| 34 | GND | Ground | 68 | GND | Ground |

## BLOCK DIAGRAM ("G1" Series 4 M Bytes)




## BLOCK DIAGRAM ("G5" Series 4 M Bytes)



## FUNCTION TABLE

| Mode | | $\overline{REG}$ | $\overline{CE1}$ | $\overline{CE2}$ | $\overline{OE}$ | $\overline{PGM}$ | $\overline{PE}$ | A0 | Vpp 2 | Vpp 1 | I/O (D15~D8) | I/O (D7~D0) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Standby | | X | H | H | X | X | X | X | $V_{CC}$ | $V_{CC}$ | High-impedance | High-impedance |
| Read A (16bit) common | | H | L | L | L | H | H | X | $V_{CC}$ | $V_{CC}$ | Odd Byte Data out | Even Byte Data out |
| Read B (8 bit) common | | H | L | H | L | H | H | L | $V_{CC}$ | $V_{CC}$ | High-impedance | Even Byte Data out |
| | | | | | | | | H | | | | Odd Byte Data out |
| Program (8 bit) common | | H | L | H | H | L | L | L | $V_{CC}$ | $V_{PP}$ | High-impedance | High-impedance |
| | | | | | | | | H | $V_{PP}$ | $V_{CC}$ | | |
| Verify (8 bit) common | | H | L | H | L | H | H | L | $V_{CC}$ | $V_{PP}$ | High-impedance | Even Byte Data out |
| | | | | | | | | H | $V_{PP}$ | $V_{CC}$ | | Odd Byte Data out |
| Latch (8 bit) common | | H | L | H | L | H | L | L | $V_{CC}$ | $V_{PP}$ | High-impedance | Even Byte Data in |
| | | | | | | | | H | $V_{PP}$ | $V_{CC}$ | | Odd Byte Data in |
| Read C (8 bit) common | | H | H | L | L | H | H | X | $V_{CC}$ | $V_{CC}$ | Odd Byte Data out | High-impedance |
| Output disable | | X | X | X | H | H | H | X | $V_{CC}$ | $V_{CC}$ | High-impedance | High-impedance |
| Read A (16bit) attribute | Available only G1 series | L | L | L | L | H | H | X | $V_{CC}$ | $V_{CC}$ | Data out (unknown) | Data out (FFh) |
| Read B (8 bit) attribute | | L | L | H | L | H | H | L | $V_{CC}$ | $V_{CC}$ | High-impedance | Data out (FFh) |
| | | | | | | | | H | | | | Data out (unknown) |
| Read C (8 bit) attribute | | L | H | L | L | H | H | X | $V_{CC}$ | $V_{CC}$ | Data out (unknown) | High-impedance |

Note 1 : H = $V_{IH}$, L = $V_{IL}$, X = $V_{IH}$ or $V_{IL}$.
$\overline{REG}$ is available only in "G1" series.

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | −0.3~6.25 | V |
| $V_{PP}$ | Supply voltage | | −0.3~14.0 | V |
| $V_I$ | Input voltage | | −0.3~$V_{CC}$+0.3 (Max. 6.25V) | V |
| $V_O$ | Output voltage | | 0~$V_{CC}$ | V |
| $T_{opr}$ | Operating temperature | | 0~70 | ℃ |
| $T_{stg}$ | Storage temperature | | −30~80 | ℃ |

## READ OPERATION

### RECOMMENDED OPERATING CONDITIONS ($T_a$ = 0~55℃, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $V_{CC}$ | $V_{CC}$ supply voltage | 4.75 | 5.0 | 5.25 | V |
| $V_{PP}$ | Vpp supply voltage | | $V_{CC}$ | | V |
| $V_{IH}$ | High input voltage | 2.4 | | $V_{CC}$ | V |
| $V_{IL}$ | Low input voltage | 0 | | 0.8 | V |

## ELECTRICAL CHARACTERISTICS ($T_a$ = 0 ~ 55°C, $V_{CC}$ = $V_{PP}$ = 4.75 ~ 5.25V, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High output voltage | $I_{OH}$ = −1.0mA (except BVD 1, BVD 2) | | 2.4 | | | V |
| $V_{OL}$ | Low output voltage | $I_{OL}$ = 2 mA | | | | 0.4 | V |
| $I_{IH}$ | High input current | $V_I$ = $V_{CC}$ V | | | | 10 | μA |
| $I_{IL}$ | Low input current | $V_I$ = 0 V | $\overline{CE1}$ $\overline{CE2}$ $\overline{REG}$ $\overline{OE}$ $\overline{PE}$ $\overline{PGM}$ | | | −70 | μA |
| | | | Other inputs | | | −10 | |
| $I_{OZH}$ | High output current in off state | $\overline{CE1}$ = $\overline{CE2}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$, $V_o$ = $V_{CC}$ V | | | | 10 | μA |
| $I_{OZL}$ | Low output current in off state | $\overline{CE1}$ = $\overline{CE2}$ = $V_{IH}$ or $\overline{OE}$ = $V_{IH}$, $V_o$ = 0 V | | | | −10 | μA |
| $I_{CC1 \cdot 1}$ | Standby $V_{CC}$ supply current 1 | $\overline{CE1}$ = $\overline{CE2}$ = $V_{IH}$, Outputs = open, Other inputs = $V_{IH}$ or $V_{IL}$ | 256KB | | | 10 | mA |
| | | | 512KB | | | | |
| | | | 1 MB | | | | |
| | | | 2 MB | | | | |
| | | | 4 MB | | | | |
| $I_{CC1 \cdot 2}$ | Standby $V_{CC}$ supply current 2 | $\overline{CE1}$ = $\overline{CE2}$ ≧ $V_{CC}$ − 0.2V, Outputs = open, Other inputs ≦ 0.2V or ≧ $V_{CC}$ − 0.2V | 256KB | | | 0.5 | mA |
| | | | 512KB | | | | |
| | | | 1 MB | | | 0.8 | |
| | | | 2 MB | | | 1.2 | |
| | | | 4 MB | | | 2 | |
| $I_{CC2 \cdot 1}$ | Active $V_{CC}$ supply current 1 | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, $\overline{PGM}$ = $\overline{PE}$ = $V_{IH}$, Outputs = open, Other inputs = $V_{IH}$ or $V_{IL}$ | 256KB | | | 200 | mA |
| | | | 512KB | | | | |
| | | | 1 MB | | | | |
| | | | 2 MB | | | | |
| | | | 4 MB | | | 220 | |
| $I_{CC2 \cdot 2}$ | Active $V_{CC}$ supply current 2 | $\overline{CE}$ = $\overline{OE}$ ≦ 0.2V, $\overline{PGM}$ = $\overline{PE}$ ≧ $V_{CC}$ − 0.2V, Outputs = open, Other inputs ≦ 0.2V or ≧ $V_{CC}$ − 0.2V | 256KB | | | 130 | mA |
| | | | 512KB | | | | |
| | | | 1 MB | | | | |
| | | | 2 MB | | | | |
| | | | 4 MB | | | 150 | |
| $I_{PP1}$ | $V_{pp}$ supply current of each $V_{PP}$ pin ($V_{PP1}$ or $V_{pp2}$) | | 256K | | | 0.1 | mA |
| | | | 512K | | | | |
| | | | 1 MB | | | 0.2 | |
| | | | 2 MB | | | 0.4 | |
| | | | 4 MB | | | 0.8 | |

Note 2 : Direction for current flowing into IC is indicated as positive (no mark).

3 : $\overline{CE}$ indicates as follows

READ A : $\overline{CE}$ = $\overline{CE1}$ = $\overline{CE2}$

READ B : $\overline{CE}$ = $\overline{CE1}$, $\overline{CE2}$ = "H" level

READ C : $\overline{CE}$ = $\overline{CE2}$, $\overline{CE1}$ = "H" level

## SWITCHING CHARACTERISTICS (COMMON MEMORY)

**Read Cycle** ($T_a$ = 0 ~ 55°C, $V_{CC}$ = $V_{PP}$ = 4.75 ~ 5.25V, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{CR}$ | Read cycle time | 250 | | | ns |
| $t_{a(A)}$ | Address access time | | | 250 | ns |
| $t_{a(CE)}$ | Card enable access time | | | 250 | ns |
| $t_{a(OE)}$ | Output enable access time | | | 125 | ns |
| $t_{dis(CE)}$ | Output disable time (from $\overline{CE}$) | | | 100 | ns |
| $t_{dis(OE)}$ | Output disable time (from $\overline{OE}$) | | | 100 | ns |
| $t_{en(CE)}$ | Output enable time (from $\overline{CE}$) | 5 | | | ns |
| $t_{en(OE)}$ | Output enable time (from $\overline{OE}$) | 5 | | | ns |
| $t_{v(A)}$ | Data valid time after address change | 0 | | | ns |

Note 4 : $V_{CC}$ must be applied and removed simultaneously with $V_{PP}$.

## SWITCHING CHARACTERISTICS (ATTRIBUTE MEMORY)

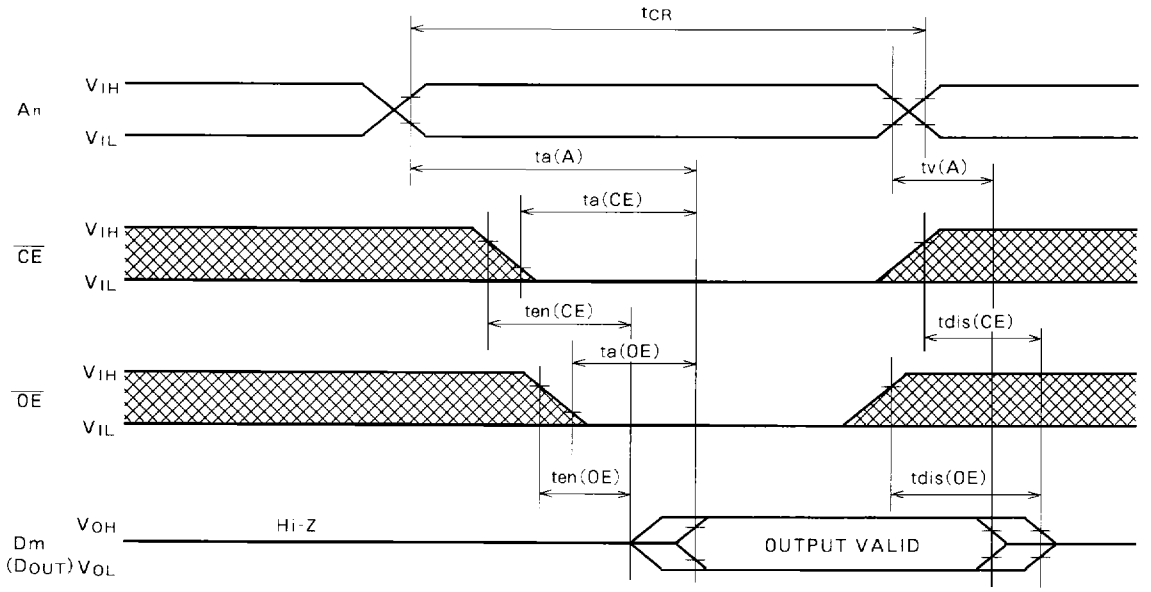
**Read Cycle** ($T_a$ = 0 ~ 55°C, $V_{CC}$ = $V_{PP}$ = 4.75 ~ 5.25V, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{CR}R$ | Read cycle time | 300 | | | ns |
| $t_{a(A)}R$ | Address access time | | | 300 | ns |
| $t_{a(CE)}R$ | Card enable access time | | | 300 | ns |
| $t_{a(OE)}R$ | Output enable access time | | | 150 | ns |
| $t_{dis(CE)}R$ | Output disable time (from $\overline{CE}$) | | | 100 | ns |
| $t_{dis(OE)}R$ | Output disable time (from $\overline{OE}$) | | | 100 | ns |
| $t_{en(CE)}R$ | Output enable time (from $\overline{CE}$) | 5 | | | ns |
| $t_{en(OE)}R$ | Output enable time (from $\overline{OE}$) | 5 | | | ns |
| $t_{v(A)}R$ | Data valid time after address change | 0 | | | ns |

Note 5 : $V_{CC}$ must be applied and removed simultaneously with $V_{PP}$.

## TIMING DIAGRAM

### Read Cycle (COMMON MEMORY)

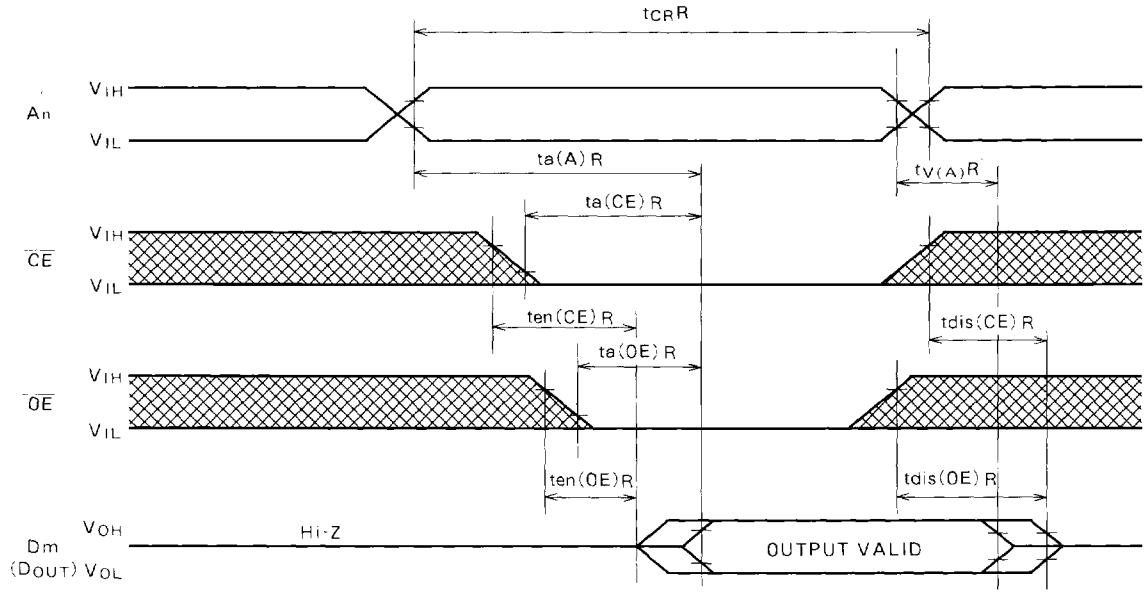



$\overline{PGM}$ = "H" level
$\overline{PE}$ = "H" level
$\overline{REG}$ = "H" level

Note 6 : Indicates the don't care input.

## TIMING DIAGRAM

### Read Cycle (ATTRIBUTE MEMORY)




$\overline{PGM}$ = "H" level
$\overline{PE}$ = "H" level
$\overline{REG}$ = "L" level

Note 7 : Test conditions for A. C. characteristics.
Input pulse levels : $V_{IL}$ = 0.45V, $V_{IH}$ = 2.8V
Input pulse rise, fall time : tr = tf = 10ns
Reference voltage Input : $V_{IL}$ = 0.8V, $V_{IH}$ = 2.4V
Output : $V_{OL}$ = 0.8V, $V_{OH}$ = 2.0V ($t_{en}$, $t_{dis}$ are measured when output voltage is ±500mV from steady state.)
Output load : 100pF + 1TTL gate
: 5pF + 1TTL gate (When $t_{en}$, $t_{dis}$ are measured)

8 : $\overline{CE}$ indicates as follows
READ A : $\overline{CE} = \overline{CE1} = \overline{CE2}$
READ B : $\overline{CE} = \overline{CE1}$, $\overline{CE2}$ = "H" level
READ C : $\overline{CE} = \overline{CE2}$, $\overline{CE1}$ = "H" level

## PROGRAM OPERATION

### RECOMMENDED OPERATING CONDITIONS ($T_a$=20~30℃, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $V_{CC}$ | $V_{CC}$ supply voltage | 5.75 | 6.0 | 6.25 | V |
| $V_{PP}$ | Vpp supply voltage | 12.2 | 12.5 | 12.8 | V |
| $V_{IH}$ | High input voltage | 3.0 | | $V_{CC}$ | V |
| $V_{IL}$ | Low input voltage | 0 | | 0.8 | V |

### ELECTRICAL CHARACTERISTICS ($T_a$=20~30℃, $V_{CC}$=5.75~6.25V, $V_{PP}$=12.2~12.8V, unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | High output voltage | $I_{OH}$=−1.0mA (except BVD1, BVD2) | | 2.4 | | | V |
| $V_{OL}$ | Low output voltage | $I_{OL}$=2mA | | | | 0.4 | V |
| $I_{IH}$ | High input current | $V_I$=$V_{CC}$ V | | | | 20 | μA |
| $I_{IL}$ | Low input current | $V_I$=0V | $\overline{CE1}$ $\overline{CE2}$ $\overline{REG}$ $\overline{OE}$ $\overline{PE}$ $\overline{PGM}$ | | | −80 | μA |
| | | | Other inputs | | | −20 | |
| $I_{CC3}$・1 | Active $V_{CC}$ supply current 1 | Outputs=open (During Data out), Inputs=$V_{IH}$ or $V_{IL}$ | 256KB | | | | mA |
| | | | 512KB | | | 250 | |
| | | | 1MB | | | | |
| | | | 2MB | | | 400 | |
| | | | 4MB | | | 650 | |
| $I_{CC3}$・2 | Active $V_{CC}$ supply current 2 | Outputs=open (During Data out) Inputs≦0.2V or ≧$V_{CC}$−0.2 | 256KB | | | | mA |
| | | | 512KB | | | 200 | |
| | | | 1MB | | | | |
| | | | 2MB | | | 350 | |
| | | | 4MB | | | 600 | |
| $I_{PP2}$・2 | $V_{PP}$ supply current of each $V_{PP}$ pin ($V_{PP}$1 or $V_{PP}$2) | $\overline{PGM}$=$V_{IL}$ | 256KB | | | | mA |
| | | | 512KB | | | 120 | |
| | | | 1MB | | | | |
| | | | 2MB | | | | |
| | | | 4MB | | | 130 | |

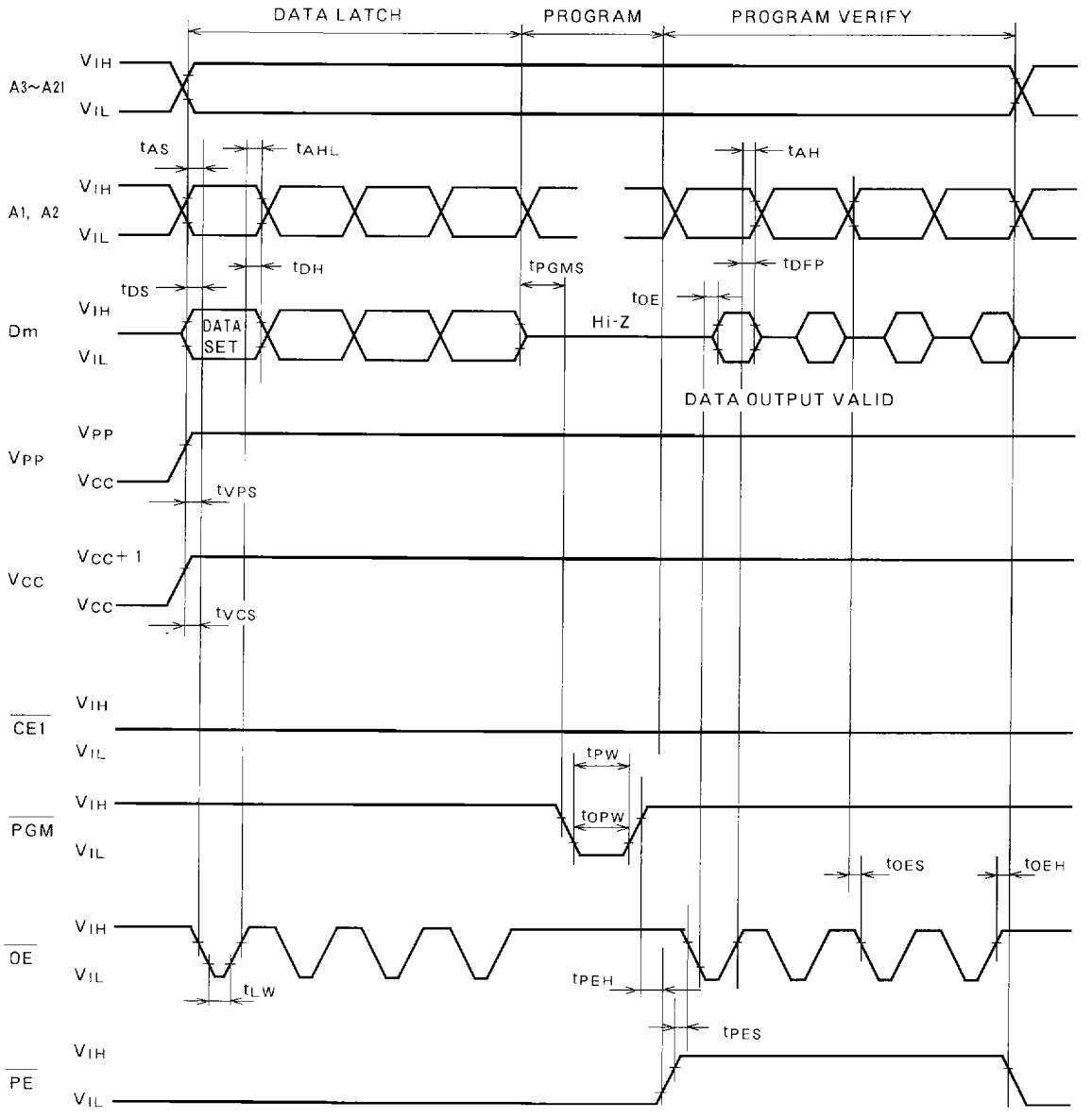
Note 9 : Direction for current flowing into IC is indicated as positive (no mark).

**SWITCHING CHARACTERISTICS** ($T_a$=20~30℃, $V_{CC}$=5.75~6.25V, $V_{PP}$=12.2~12.8V, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | |
| $t_{AS}$ | Address setup time | 2 | | | μs |
| $t_{OES}$ | $\overline{OE}$ setup time | 2 | | | μs |
| $t_{DS}$ | Data setup time | 2 | | | μs |
| $t_{AH}$ | Address hold time | 0 | | | μs |
| $t_{AHL}$ | | 2 | | | μs |
| $t_{DH}$ | Data hold time | 2 | | | μs |
| $t_{DFP}$ | Output disable time (from $\overline{OE}$) | 0 | | 190 | ns |
| $t_{VCS}$ | $V_{CC}$ setup time | 2 | | | μs |
| $t_{VPS}$ | $V_{PP}$ setup time | 2 | | | μs |
| $t_{PW}$ | $\overline{PGM}$ initial program pulse width | 0.19 | 0.20 | 0.21 | ms |
| $t_{OPW}$ | $\overline{PGM}$ over program pulse width | 0.19 | | 5.25 | ms |
| $t_{PES}$ | $\overline{PE}$ setup time | 2 | | | μs |
| $t_{OE}$ | Data valid from $\overline{OE}$ | 0 | | 210 | ns |
| $t_{LW}$ | Data latch time | 1 | | | μs |
| $t_{PGMS}$ | $\overline{PGM}$ setup time | 2 | | | μs |
| $t_{PEH}$ | $\overline{PE}$ hold time | 2 | | | μs |
| $t_{OEH}$ | $\overline{OE}$ hold time | 2 | | | μs |

Note 10 : $V_{CC}$ must be applied and removed simultaneously with $V_{PP}$.

## PROGRAM TIMING DIAGRAM (4 M Bytes)



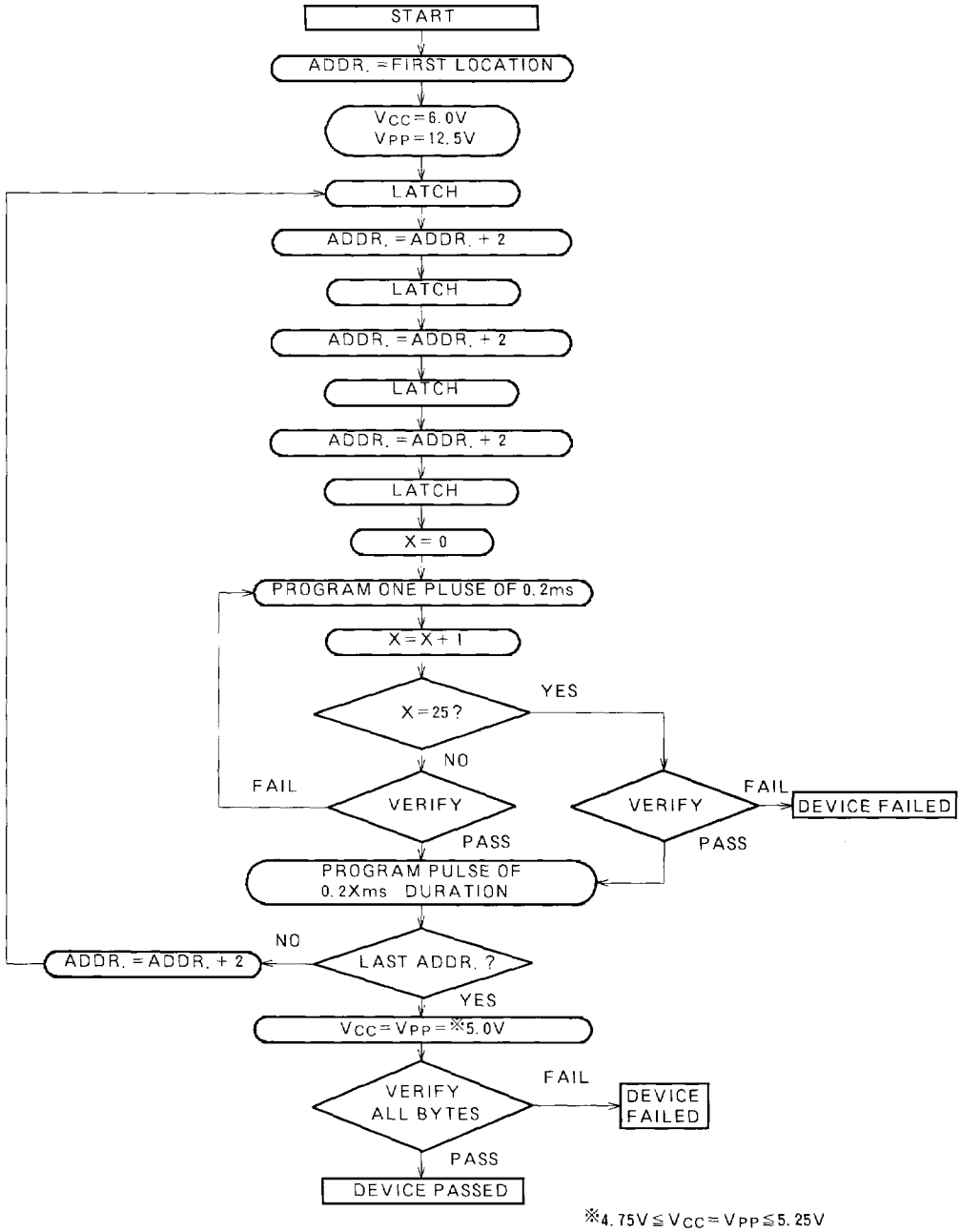

CE2 = "H" level

Note 11 : Test conditions

| | | | |
|---|---|---|---|
| Input pulse level | | : $V_{IL}$ = 0.45V, $V_{IH}$ = 3.4V | |
| Input pulse rise, fall time | | : $t_r = t_f$ = 10ns | |
| Reference voltage | input | : $V_{IL}$ = 0.8V, $V_{IH}$ = 3.0V | (tDFP is measured when |
| | output | : $V_{OL}$ = 0.8V, $V_{OH}$ = 2.0V | output voltage is ±500mV from steady state.) |

12 : Odd byte is accessed when A0 = "H" level, and even byte is accessed when A0 = "L" level

## PROGRAMMING ALGORITHM FLOW CHART




※4.75V≦VCC=VPP≦5.25V

## CAPACITANCE

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $C_I$ | Input capacitance | $V_I$=GND, $V_I$=25mVrms, f=1MHz, $T_a$=25℃ | | | 45 | pF |
| $C_O$ | Output capacitance | $V_I$=GND, $V_I$=25mVrms, f=1MHz, $T_a$=25℃ | | | 45 | pF |

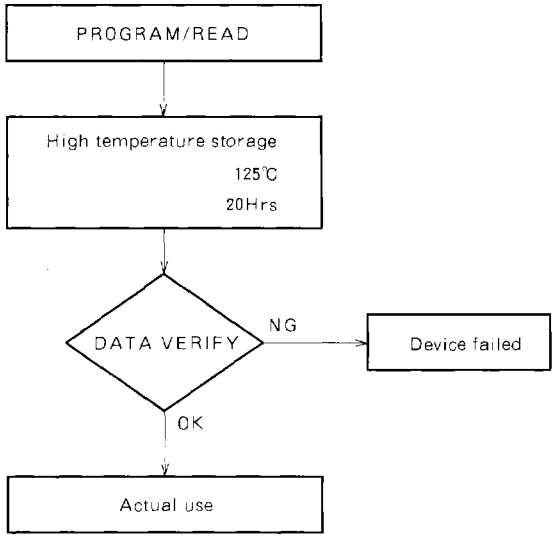
Note 13 : These items are not 100% tested.

## DEVICE IDENTIFIER MODE

This card does not support a device identifier mode. Do not apply voltages exceeding 6.25V to the A9 pin.

## RECOMMENDED SCREENING CONDITIONS

The following screening test is recommended before using a card for evaluation which you have programmed. If you use cards for another purpose, it is recommended that the manufacturer programs them.




Note 14 : The color of panels might be affected at this high-temperature storage.
It is recommended that you attach labels of your own design to the surface of the card after the data verify test.

## IC MEMORY CARD GUIDELINES VER. 4

(defined by Japan Electronic Industry Development Association Personal Computer Operation Committee)

Specifications of this card are partly different from the IC memory card guidenes ver. 4 defined by Japan Electronic Industry Development Association (JEIDA) Personal Computer Operation Committee. The differences are as follows.

1. Mode of programing operation is original.
2. $\overline{PE}$ : program enable signal (44 pin) is added to this card.