HEWLETT PACKARD

Decision Circuit (Comparator/D-FF)

Technical Data

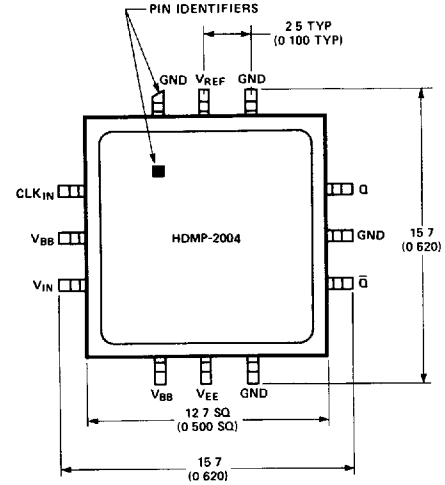
HDMP-2003
HDMP-2004

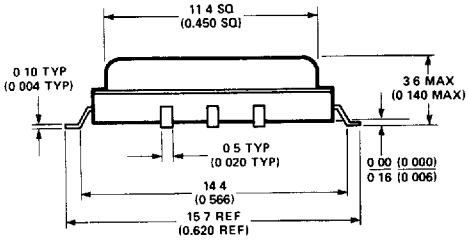
Features

- **Silicon Bipolar Technology**
- **ECL Levels**
- **Operational to 1.5 GBit Input Rates**
- **Single -5.2 V Power Supply**
- **Operational over Full Temperature Range -55°C to +125°C**
- **Highly Reliable HBIC Hermetic Surface Mount Package**
- **Low Power Dissipation ≤0.5 W**

Description/Applications

The HDMP-2003, and -2004 Decision Circuits are high speed/ high sensitivity digital waveform regeneration modules consisting of a comparator, an edge-triggered D-flip-flop, and a 50 ohm output driver. They sample GBit data in both time and amplitude, and decide whether a "1" or a "0" exists relative to an internal V_{BB} or external DC reference voltage, thus regenerating a retimed, less noisy digital waveform. They are recommended for use as the data regeneration circuits in high speed fiber optics communication receivers. Other applications include Digital Radio communications systems, High Speed Computer Interconnect Systems, Instrumentation, and other Data Recovery Systems.





NOTE BOTTOM OF PACKAGE IS PRIMARY GROUND CONTACT
ALL DIMENSIONS IN MILLIMETERS (INCHES)

OUTLINE HBIC-0512
WEIGHT (TYPICAL): 1.15 GRAMS
(HDMP-2003, HDMP-2004)

FIBER OPTICS

Absolute Maximum Ratings

Symbols	Parameters	Units	Ratings
V_{EE}	Supply Voltage	V	-6.0
T_{STG}	Storage Temperature	°C	-60 to +150
T_C	Operating Case Temperature	°C	-55 to +125
V_{IN}	Input Voltage	V	+2 pk-pk

Operation in excess of these conditions may result in permanent damage to the device.

Operating Specifications

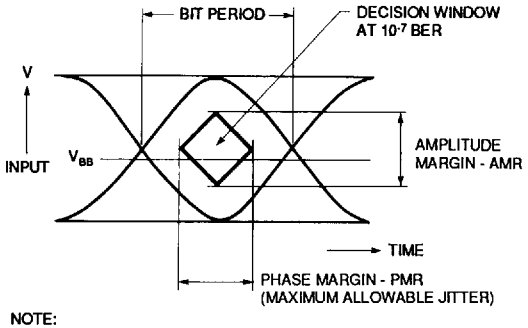
Symbols	Parameters	Units	HDMP-2003		HDMP-2004	
			Min.	Typ.	Min.	Typ.
DR	Input Data Rate	GBits/sec	2.0	2.4	2.8	
AMR[1]	Amplitude Margin	mV	100	120	70	130
PMR[1]	Phase Margin	psec	250	300	170	240
VTM	Threshold Margin	mV		40		40
t_r[2]	Rise Time	psec		110		120
t_f[2]	Fall Time	psec		110		90
V_O	pk-pk Output Voltage	Volts		0.6		0.6
I_{EE}	Supply Current	mA		70		60

Test Conditions:
V_{EE} = -5.2 V
CLK: HDMP-2003 = 2.0 GHz, 400 mV pk-pk
HDMP-2004 = 2.8 GHz, 400 mV pk-pk

V_{IN}: HDMP-2003 = 2.0 GHz, 200 mV pk-pk
HDMP-2004 = 2.8 GHz, 200 mV pk-pk

2^{15}-1 Pseudo Random Bit Sequence (PRBS)
CLK, V_{IN}, and Output are at 50 Ohms AC coupled
T_A = 25°C

Notes:
1. See Figure 1A.
2. 10% to 90% (see Figure B).



NOTE:
VTM = THE MINIMUM DIFFERENCE BETWEEN THE INTERNAL REFERENCE VOLTAGE AND THE NEAREST EDGE OF THE AMPLITUDE MARGIN WINDOW.

Figure 1a. Decision Window Definition.

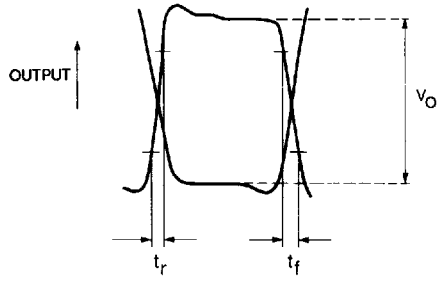


Figure 1b. Output Waveform Definition.

TYPICAL RETURN LOSS AT T = 25°C FOR HDMP-2003

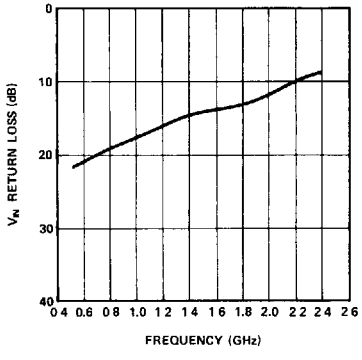


Figure 2a.

TYPICAL CASE TEMPERATURE PERFORMANCE FOR HDMP-2003

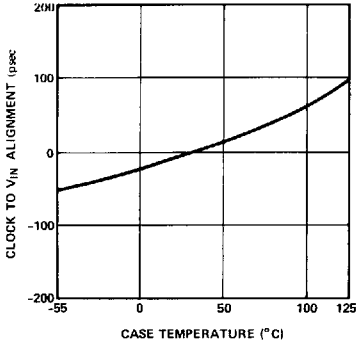


Figure 2b.

TYPICAL RETURN LOSS AT T = 25°C
FOR HDMP-2003

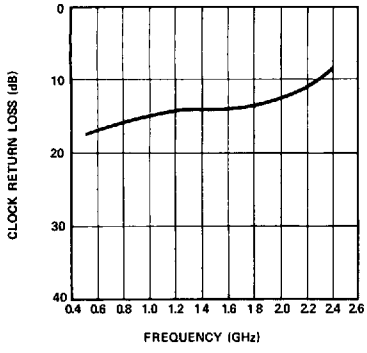


Figure 2c.

TYPICAL CASE TEMPERATURE PERFORMANCE
FOR HDMP-2003

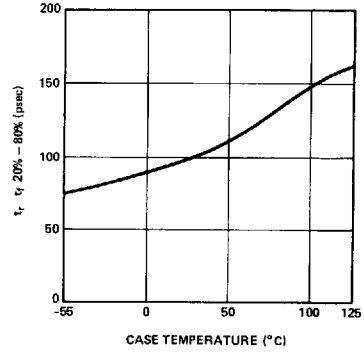


Figure 2d.

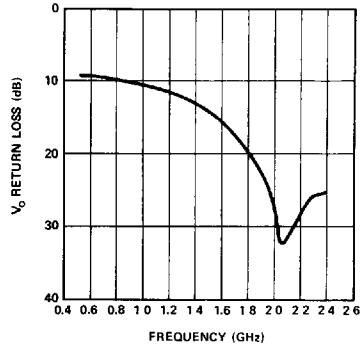


Figure 2e.

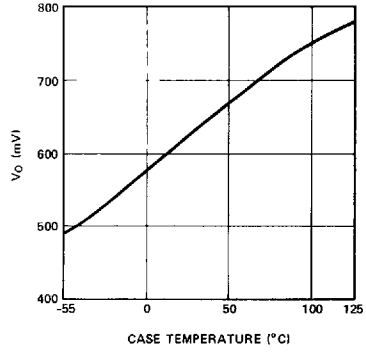


Figure 2f.

TYPICAL RETURN LOSS AT T = 25°C
FOR HDMP-2004

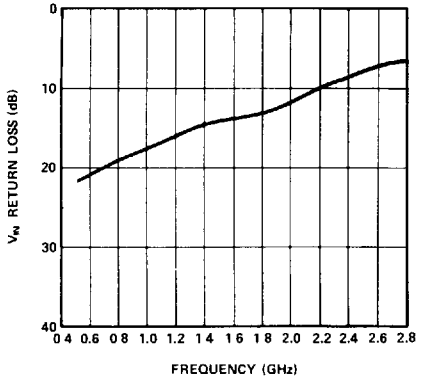


Figure 3a.

TYPICAL CASE TEMPERATURE PERFORMANCE
FOR HDMP-2004

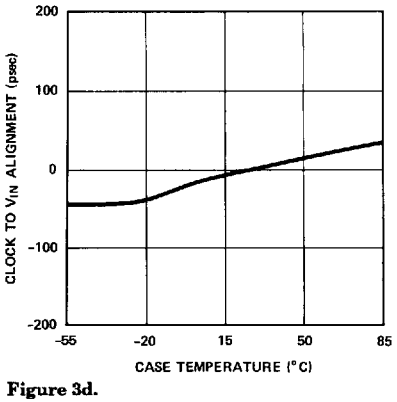


Figure 3d.

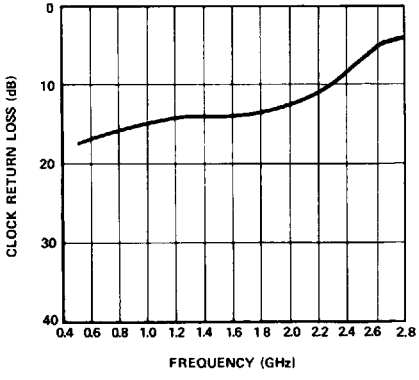


Figure 3b.

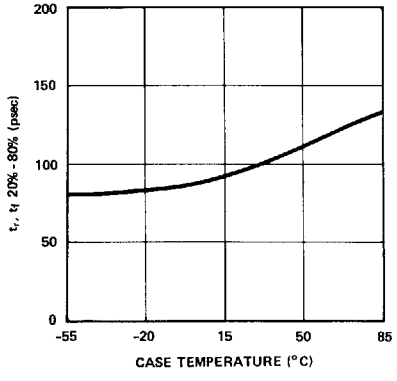


Figure 3e.

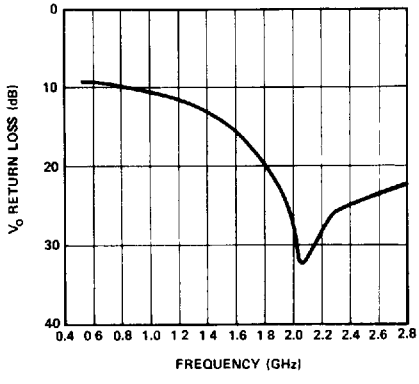


Figure 3c.

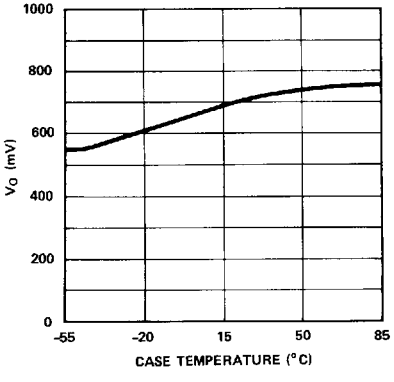


Figure 3f.

FIBER OPTICS

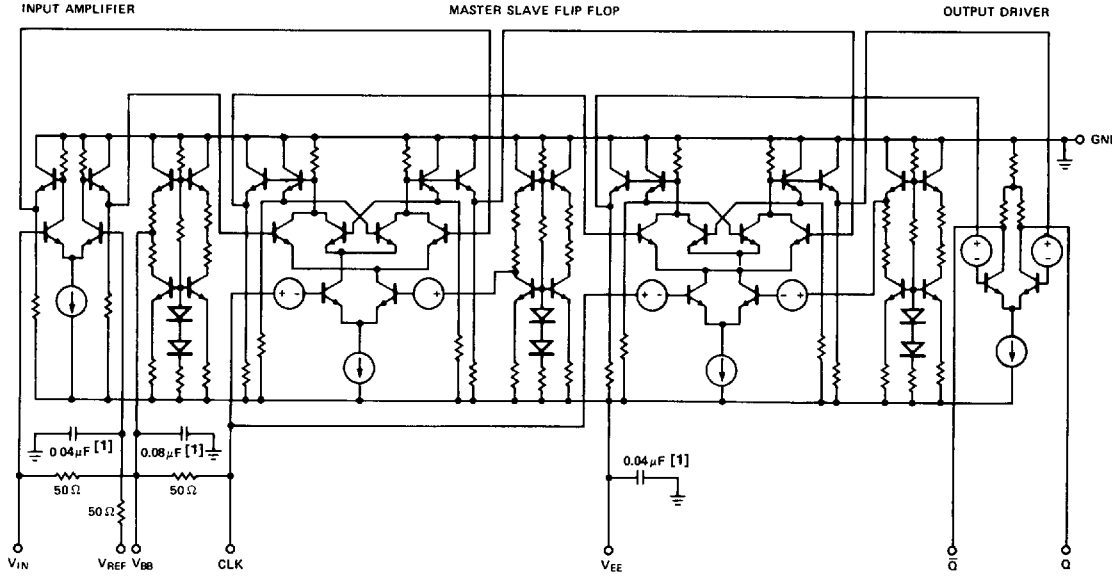
Theory of Operation

The HDMP-2003 and -2004 consist of three major sections – an input comparator amplifier, a master-slave flip-flop, and an output driver (see Figure 4). During operations, a distorted waveform enters the comparator via V_{IN}, and is compared to a reference DC voltage supplied at V_{REF}. The output of the D-flip-flop is next fed into the D-flip-flop section where a clock input triggers the master/slave action that synchronizes the signal with the rising edge of the clock. The amplified and retimed signal then exits the module through the driver section.

Under normal operating conditions, V_{REF} is connected to V_{BB}, and V_{IN} and CLK are externally capacitively coupled (see Figure 4). The internal termination resistors also form a biasing network which eliminate the need for additional external biasing. The integrity of the input amplifier is determined by the Amplitude Margin (AMR), which is defined by the range of V_{REF} at which the Bit Error Rate (BER) is less than 10^{-7}. For values inside this range, the BER falls sharply to produce virtually error free operation (see Figures 6 and 8).

The performance of the retiming flip-flop is determined by the Phase Margin (PMR) which is defined by the range of deviation of clock alignment relative to the input signal at a BER less than 10^{-7}. Again, the BER falls sharply inside this range (see Figure 7 and 9). Once the clock to data alignment is set, the internal compensation circuitry will track this alignment over temperature (see Figures 2d and 3d).

The output driver section is characterized by the peak-to-peak output voltage and the 10% to 90% rise and fall times relative to the levels at the center of the output bit. This driver also has the advantage of driving directly into 50 ohms with or without a coupling capacitor, or directly into ECL (see Figure 10). The excellent line matching also dampens pulse reflections typical for many high frequency circuit interconnections.



[1]HDMP-2004 only.

Figure 4. Circuit Schematic, HDMP-2003 and HDMP-2004.

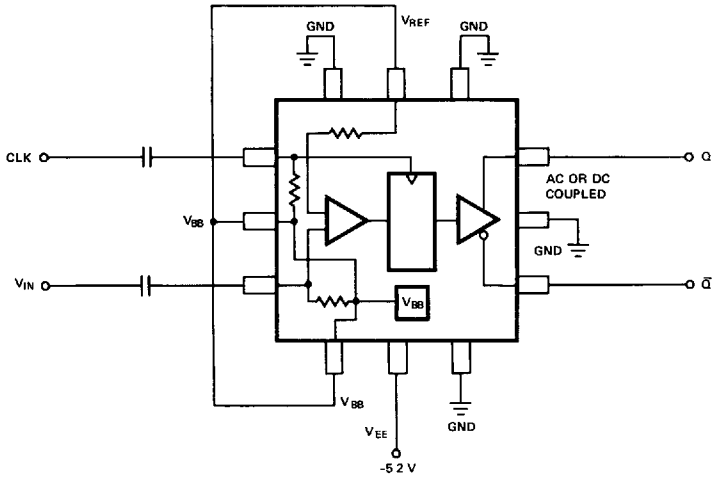


Figure 5. Typical Interfacing Diagram (Top View); HDMP-2003, HDMP-2004.

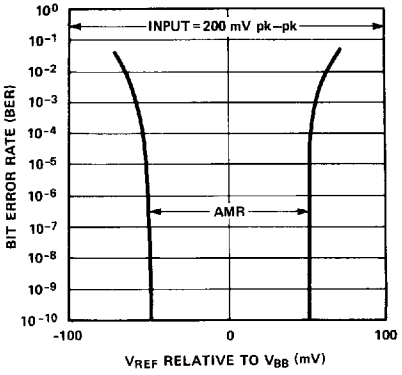


Figure 6. Amplitude Margin (AMR), HDMP-2003.

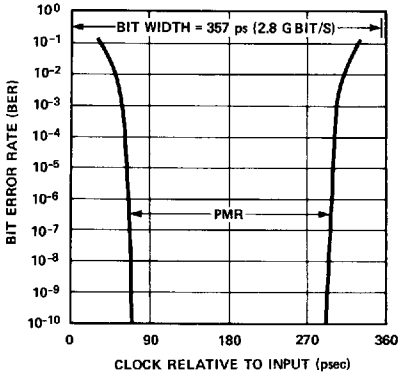


Figure 7. Phase Margin (PMR), HDMP-2003.

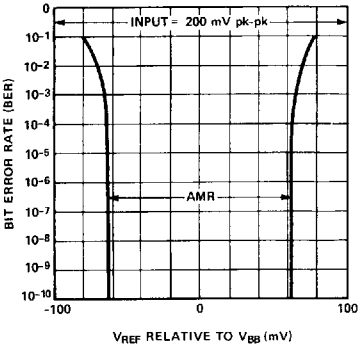


Figure 8. Amplitude Margin (AMR), HDMP-2004.

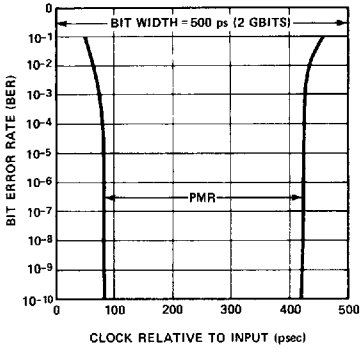


Figure 9. Phase Margin (PMR), HDMP-2004.

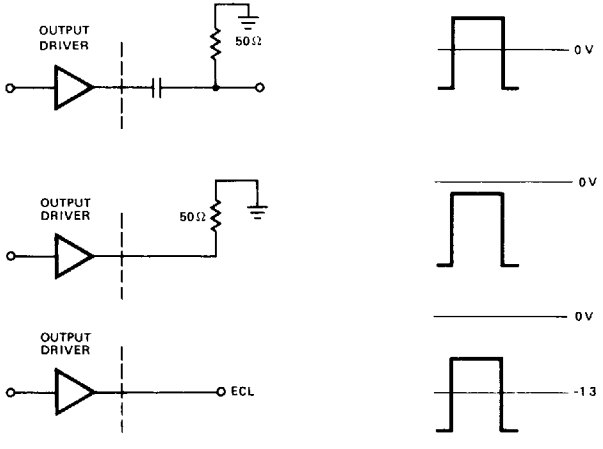


Figure 10. Output with Various Loading Conditions, HDMP-2003, HDMP-2004.

Testing

The characterization test set-up for the HDMP-2003 and -2004 is shown in Figure 11. The input signal is provided by a pseudo random bit sequence (PRBS) generator set at the operating frequency. To insure that the DUT is correctly evaluated, the square wave output from the generator (A) is fed into a high performance AGC amplifier (HAMP-5001), which emulates a typical system. The AGC amplifier output (B), and the sinusoidal clock signals (C) are applied to the DUT. The outputs Q and $\overline{Q}$ are measured with the BER receiver and a sampling scope (D).

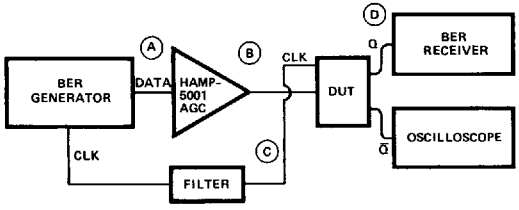
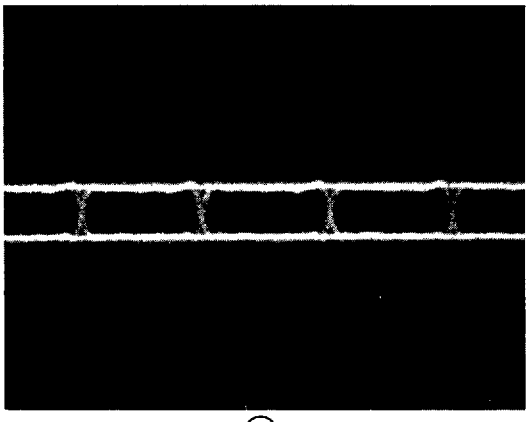
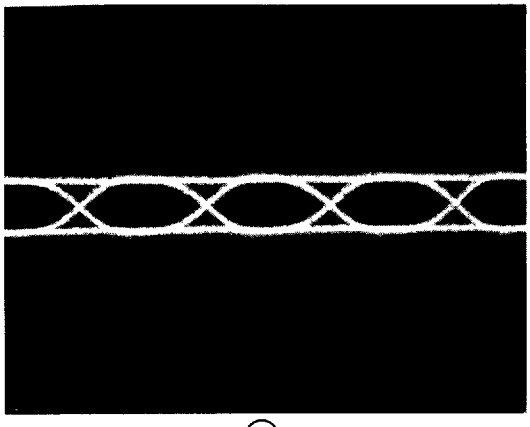


Figure 11. Test Setup

HDMP-2003

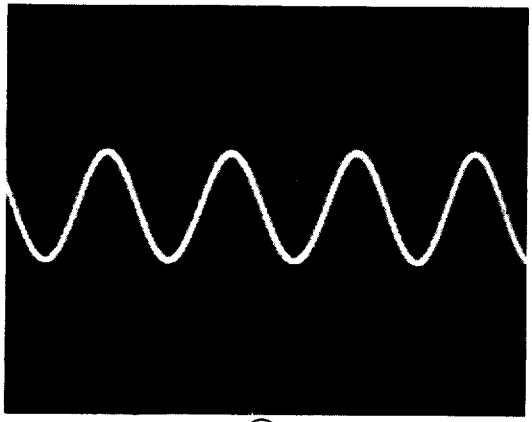


(A)

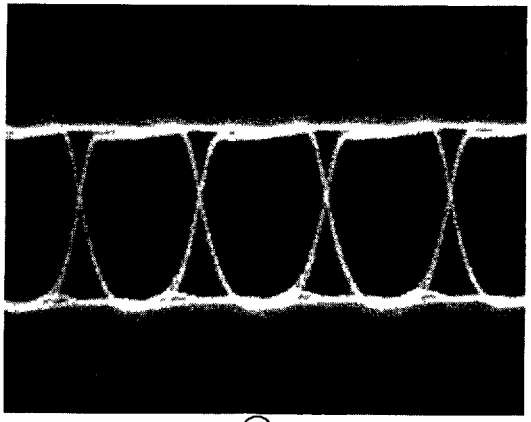


(B)

HDMP-2003 continued

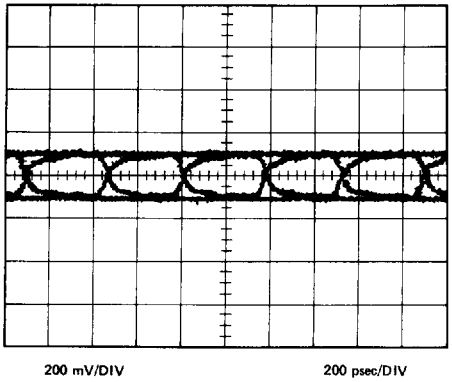


C

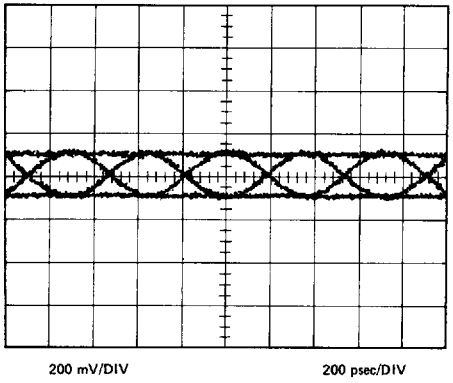


D

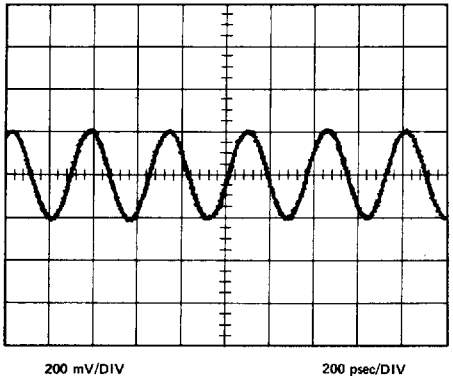
HDMP-2004



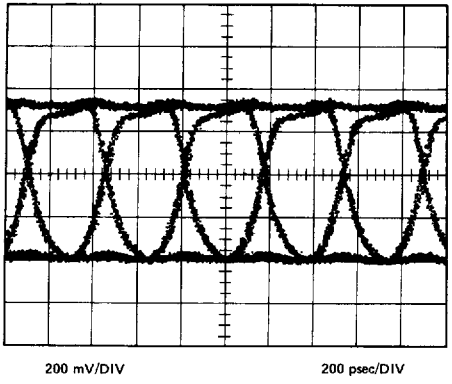
A



B



C



D

Figure 12. Characterization Test Set-up.

Handling and Mounting Procedures for Hermetic, Base is Circuit (HBIC-0512 Packages

1. Storage

Under normal circumstances, storage of the HBIC packages in HP supplied containers is sufficient. However, in particularly dusty or chemically hazardous environments, storage in a clean, inert atmosphere is advised to maintain solderability.

2. Handling

As with any multi-leaded surface mount package, care must be taken during handling of the HBIC package not to cause deformation of the leads. The planarity of the leads to each other and to the bottom of the package must be maintained for successful mounting.

The HBIC package can be handled with tweezers or other tools by clamping the package around the lid, or with vacuum systems on the top of the lid.

3. Grounding

The prime ground contact of the HBIC package is its bottom (with unused leads and the lid as secondary ground points). For optimum circuit performance, the bottom of the package must be soldered to a ground pad on the substrate (PC board or ceramic). This ground pad should be the size of the package bottom and have several plated thru holes to the substrate's ground plane, giving the package a low inductance contact to system ground.

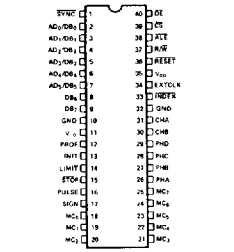
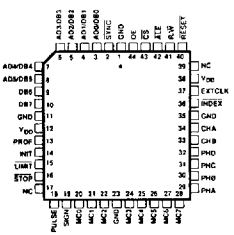
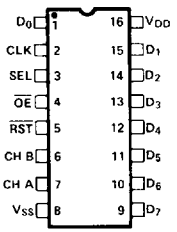
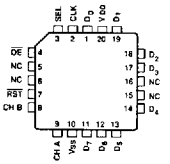
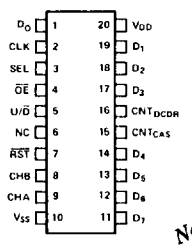
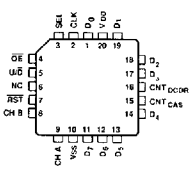
4. Mounting

Solder reflow is the suggested method of attaching HBIC packages onto substrates. The recommended solder is 62% Sn, 36% Pb, 2% Ag, with an RMA flux. This solder paste can be dispensed (for packages with wide lead spacing) or screen printed onto the substrate. The use of a solder mask on the substrate is also recommended. Solder reflow can then be achieved by infrared heating or vapor-phase heating. The packages must not be exposed to more than 260°C for 20 seconds.

Conductive epoxy could be used for mounting the HBIC packages, however, care must be taken due to the potential problem of silver migration between the leads and the ground pad under the package.

Wave soldering is not recommended due to the metal lid and the need for solder under the package base.

Motion Control ICS – HCTL-XXXX Series

Package Outline Drawing	Part No.	Package	Description	Page No.
	HCTL-1100	PDIP	CMOS General Purpose Motion Control IC	1-104
	HCTL-1100 OPT PLC	PLCC	CMOS General Purpose Motion Control IC	
	HCTL-2000	PDIP	CMOS Quadrature Decoder/Counter IC, 12-bit Counter	1-86
	HCTL-2016	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	
	*New* HCTL-2016 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter	1-102
	HCTL-2020	PDIP	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-86
	*New* HCTL-2020 OPT PLC	PLCC	CMOS Quadrature Decoder/Counter IC, 16-bit Counter, Quadrature Decoder Output Signals, Cascade Output Signals	1-102

Accessories for Encoders and Encoder Modules

Package Outline Drawing	Part No.	Description	Page No.
	HEDS-8902	4-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5500 and HEDS-5600 2 channel encoders. Also fits HEDS-9000, HEDS-9100, and HEDS-9200 2 channel encoder modules.	1-61 1-22 1-28
	HEDS-8903	5-wire connector with 15.5 cm (6.1 in.) flying leads. Locks into HEDS-5540 and HEDS-5640 three channel encoders. Also fits HEDS-9040 and HEDS-9140 three channel encoder modules.	1-61 1-32
	HEDS-8905	Alignment Tool for HEDS-9140	1-32
	HEDS-8906	Alignment Tool for HEDS-9040	1-32
	HEDS-8901	Gap Setting shown for film codewheels	1-51
	HEDS-8932	Gap Setting shown for glass codewheels	1-51
	HEDS-8910 OPT 0 □□	Alignment Tool for HEDS-5540/5545 and HEDS-5640/5645. Order in appropriate shaft size.	1-61