Features

- **Four short-circuit protected high-side drivers with a maximum current capability of 50 mA each**
- **Four short-circuit protected low-side drivers with a maximum current capability of 50 mA each**
- **ON resistance high side R_{on}< 10 Ω vs. total temperature range**
- **ON resistance low side R_{on} < 7 Ω vs. total temperature range**
- **Short-circuit detection of each driver stage**
- **Disabling of driver stages in the case of short-circuit detection and overtemperature detection**
- **Independent control of each driver stage via an 8-bit shift register**
- **Status output reports short-circuit condition**
- **Status output reports that all loads are switched off**
- **Timing of Status output reset signalizes the failure mode**
- **Temperature protection in conjunction with short-circuit detection**

Dual Quad Driver IC

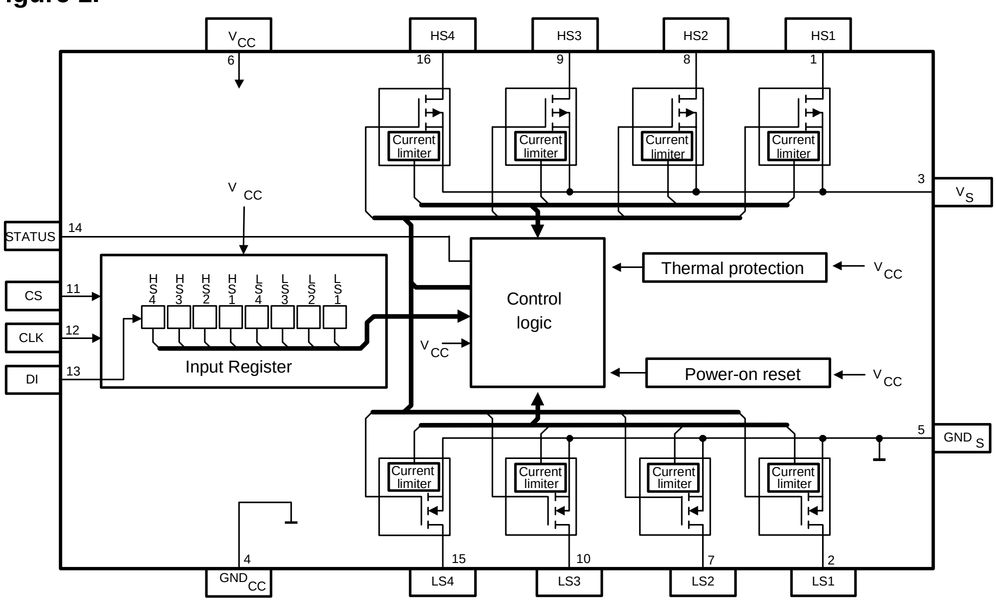
U6820BM

Description

The U6820BM is a driver interface in BCDMOS technology with 8 independent driver stages having a maximum current capability of 50 mA each. Its partitioning into 4 high-side and 4 low-side driver stages allows an easy connection of either 4 half bridges or 2 H-bridges on the pc board. The U6820BM communicates with a microcontroller via an 8-bit serial interface. Integrated protection against short circuit and overtemperature give added value. EMI protection and 2kV ESD protection together with automotive qualification referring to conducted interference (ISO/TR 7637/1) make this IC ideal for both automotive and industrial applications.

Block Diagram

Figure 1.



Ordering Information

Extended Type Number	Package	Remarks
U6820BM-FP	SO16	

Rev. A5, 04-Dec-01

Pin Configuration

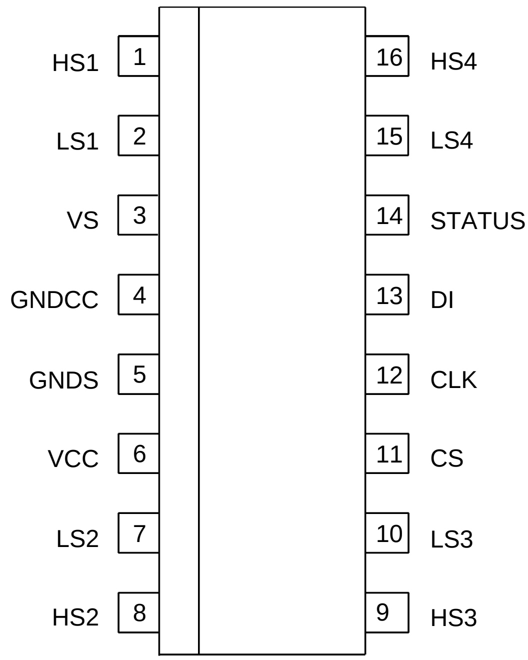


Figure 2. Pinning SO16

Pin Description

Pin	Symbol	Function
1	HS1	Output high side 1
2	LS1	Output low side 1
3	VS	Supply voltage 6 V to 18 V
4	GNDCC	Digital ground
5	GNDS	Power ground
6	VCC	Supply voltage 5 V (external)
7	LS2	Output low side 2
8	HS2	Output high side 2
9	HS3	Output high side 3
10	LS3	Output low side 3
11	CS	Set supply status (chip select)
12	CLK	Clock line for 8-bit control shift register
13	DI	Data line for 8-bit control shift register
14	STATUS	Status output *) (H = fault)
15	LS4	Output low side 4
16	HS4	Output high side 4

Description of the Control Interface to the µC

The serial-parallel-interface includes basically an 8-bit shift register (SR), an 8-bit command register (CR) and a 4-bit counter.

The data input takes place with commands at Pins DI (data input), CS (chip select) and CLK (clock). With a falling edge at CLK, the information at DI is transferred into the SR. The first information written into the SR is the least significant bit (LSB). The Pin STATUS is used for diagnostic purposes and reports any fault condition to the microcontroller.

The input CS in accordance with the CR controls the serial interface. A high level at CS disables the SR. With a falling edge at CS, the SR is enabled. The CR control allows that only the first 8 bits will be transferred into the SR, and further clocks at CLK are ineffective. If a rising edge occurs at CS after 8 clocks precisely, the information from the SR is transferred into the CR. If the number of clock cycles during the low phase of CS was less or more than eight transitions, no transfer will take place. A new command controls the output stages on or off immediately.

Every output stage is controlled by one specific bit of the CR. Low level means “supply off” or inactive, and high level means “supply on” or active. If all 8 bits are on low level, the output stages will be set into standby mode.

If one of the output stages detects a short circuit and additionally overtemperature condition, the corresponding control bit in the CR is set to low. This reset has priority over an external command to CR, thus, this does not affect the 1^{st} control bit. The priority protects the IC against overtemperature by activating the temperature shut down immediately.

The STATUS Output

The STATUS output is on low level during normal operation. If one or more output stages detect short circuit or if overtemperature is indicated, the STATUS output changes to high level (OR-connection).

For diagnostic purposes (self test of the status output), the status output can also be brought into high level during standby mode.

Timing of the Status Output Reset Signalizes the Failure Mode

The use of different reset conditions at the STATUS output simplifies the failure analysis during normal operation, and is also beneficial during testing.

The storage content can be used for STATUS output. It is indicated and latched immediately with the rising edge of CS at STATUS output if less than 8 clocks were received during the low phase of CS. The reset is initiated by the falling edge of the 8^{th} clock (bit 7) of the next data input.

Also, the appearance of more than 8 clocks is latched and indicated at STATUS by the rising edge of the 9^{th} clock. The reset is initiated by the falling edge of the 2^{nd} clock (bit 1) of the next data input.

The detection of overtemperature is latched internally. It is reset by the falling edge of the 4^{th} clock (bit 3) of a data transfer if overtemperature is no longer present.

Power-On Reset

After switching on the supply voltage, all data latches are reset and the outputs are switched off. The typical power-on reset threshold is V_{CC} = 3.7 V. The outputs are activated after the first data transfer.

Short-Circuit Protection

The current of the output stages is limited by an active feedback control. Short circuit at one output stage sets the diagnostic Pin 14 (STATUS) to high. In case of both conditions, short circuit at one of the outputs and temperature detection, the affected output is switched off selectively. It will be activated again after the first new data transfer.

Inductance Protection

Clamping diodes and FETs are integrated to protect the IC against too high or too low voltages at the outputs. They prevent the IC from latch up and parasitic currents which may cause a too high power dissipation.

Temperature Protection

The IC is protected by an overtemperature detection. As soon as the junction temperature T_j = 155°C typically is exceeded, the diagnostic Pin 14 (STATUS) is set "high". General over-temperature detection along with short-circuit condition at a specific output result in temperature shut down at that specific output. After temperature shut down, the data input register has to be set again with a hysteresis of typically DT = 15 K (T_j = 140°C).

ESD Protection

All output stages are protected against electrostatic discharge up to 5 kV (HBM) with external components (see figure 5), all other pins are protected up to 2 kV (HBM).

Table 1. Timing of the STATUS output

Shift register								Command Register								Condition	Low-Side Switch				High-Side Switch				Status	
																	LS1	LS2	LS3	LS4	HS1	HS2	HS3	HS4	Set	Reset
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	All out = OK	off	off	off	off	off	off	off	off	H	New CS
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	All on = OK	on	on	on	on	on	on	on	on	L	
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	E.g. one on = OK	off	off	off	off	off	off	off	on	L	
0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	Short at LS3	off	on	on	on	on	on	on	on	H	No short
1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	Temp & short at HS4	on	on	on	off	on	on	on	on	H	New CS4
1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	V_{VCC} < 3.7 V = P-ON	off	off	off	off	off	off	off	off	H	P-ON, CS
1	1	1	0	0	0	1	1	x	x	x	x	x	x	x	x	CS with less 8 CLK	x	x	x	x	x	x	x	x	H	New CS 8
0	0	0	1	1	1	0	0	x	x	x	x	x	x	x	x	CS with more 8 CLK	x	x	x	x	x	x	x	x	H	New CS 2

Figure 3. Data transfer timing diagram

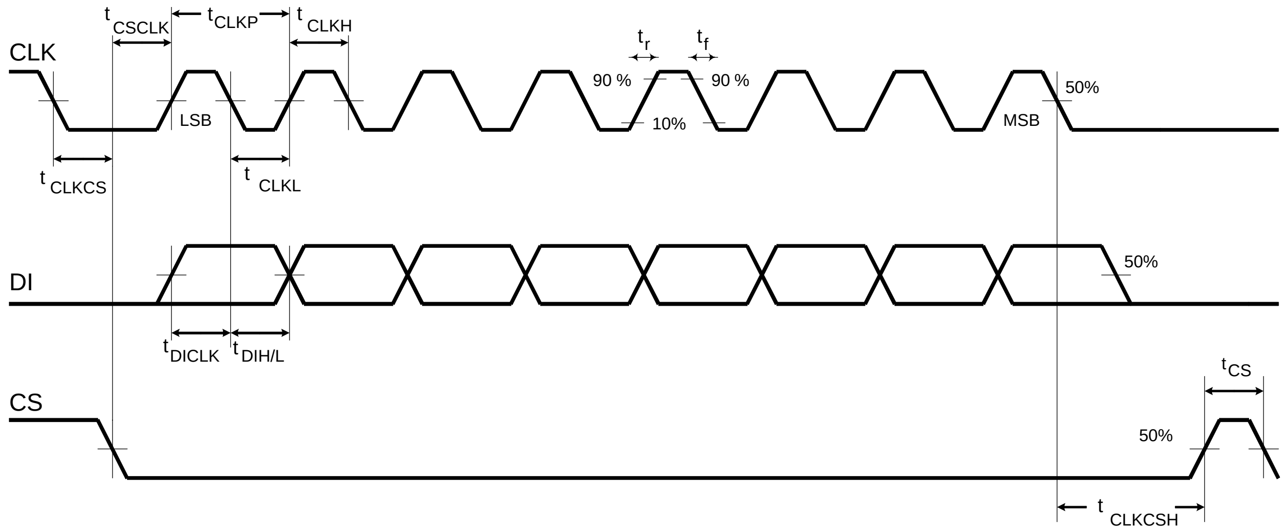
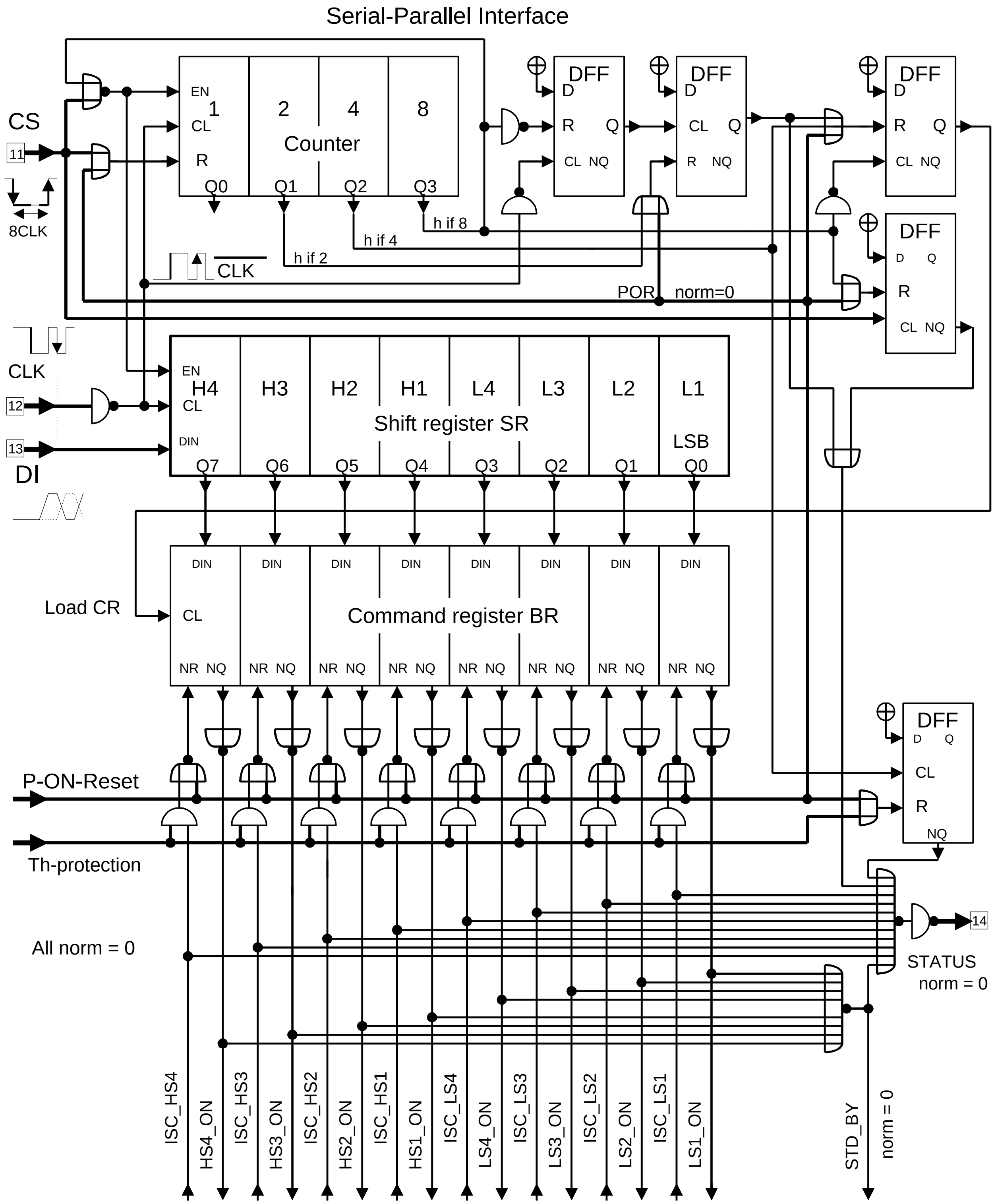


Table 2. AC characteristics for testing

Specification	Conditions	Min.	Max.	Unit
t_r (rise)	10% to 90% V_{CC} on CLK, DI and CS		10	ns
t_f (fall)	10% to 90% V_{CC} on CLK, DI and CS		10	ns
t_{CLKP}	1/2 V_{CC}	250		ns
t_{CLKH}	1/2 V_{CC}	100		ns
t_{CLKL}	1/2 V_{CC}	100		ns
t_{CLKCS}	1/2 V_{CC}	150		ns
t_{CSCLK}	1/2 V_{CC}	100		ns
t_{DICLK}	1/2 V_{CC}	80		ns
$t_{DIH/L}$	1/2 V_{CC}	100		ns
t_{CLKCSH}	1/2 V_{CC}	100		ns
t_{CS}	1/2 V_{CC}	250		ns

Block Diagram of the Control Interface

Figure 4.



Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply voltage ....Pin 3	V_{VS}	-0.3	40	V
Logic supply voltage . ...Pin 6	V_{VCC}	-0.3	7	V
Logic input voltage ... .Pins 11, 12 and13	CS, CLK, DI	-0.3	V_{VCC} + 0.5	V
Logic output voltage . ...Pin 14	STATUS	-0.3	V_{VCC} + 0.3	V
Input current ....Pin 3	I_{VS}		0.2	mA
Input current ....Pin 6	I_{VCC}		5	mA
Output current ....Pins 1-2, 8-11 (internally limited) ....and 15-16	$I_{1H\text{-}4H}$ and $I_{1L\text{-}4L}$	30	65	mA
Junction temperature range	T_j	- 40	150	°C
Storage temperature range	T_{stg}	- 55	150	°C

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient	R_{thJA}	110	K/W
Junction case	R_{thJC}	26	K/W

Operating Range

Parameter	Symbol	Value	Unit
Supply voltage ....Pin 3	V_{VS}	6 to 18	V
Logic supply voltage ....Pin 6	V_{VCC}	4.5 to 5.5	V
Logic input voltage low ......Pins 11, 12 and 13	CS, CLK, DI	-0.2 to (0.2 x V_{VCC})	V
Logic input voltage high.....Pins 11, 12 and 13	CS, CLK, DI	(0.7 x V_{VCC}) to (V_{VCC} + 0.3)	V
Logic output voltage (1 mA load) ...Pin 14	STATUS	0.5 to (V_{VCC} - 1)	V
Clock frequency	f_{CLK}	5	MHz
Junction temperature range	T_j	-40 to 150	°C

Electrical Characteristics

7 V < V_{VS} < 40 V; 4.5 V < V_{VCC} > 5.5 V; -40°C < T_j < 150°C; unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1	**Current consumption**								
1.1	Supply current (VS)	No external load	3	I_{VS}			0.2	mA	A
1.2	Supply current (VCC)	No external load	6	I_{VCC}			5	mA	A
1.3	Power-on reset threshold		6	$V_{CC\ POR}$	3.4	3.7	4.0	V	A
*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter									

Electrical Characteristics

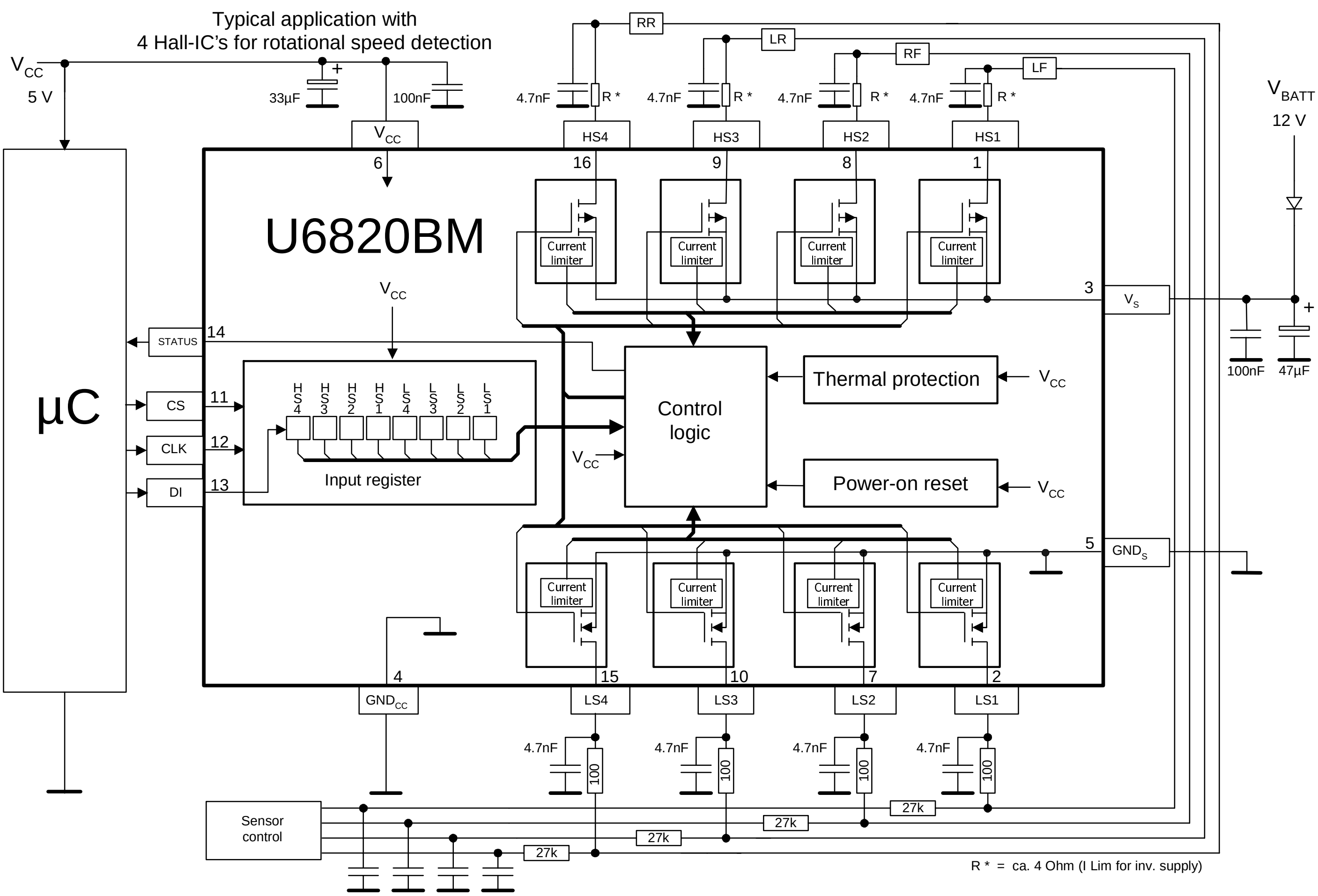
7 V < V_{VS} < 40 V; 4.5 V < V_{VCC} > 5.5 V; -40°C < T_j < 150°C; unless otherwise specified.

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
1.4	Power-on reset delay time	After switching on V_{CC},	6	$T_{d\ POR}$	60	95	130	µs	D
2	**Thermal shutdown**								
2.1	Thermal shutdown set			$t_{j\ PW\ set}$	140	155	165	°C	A
2.2	Thermal shutdown reset			$t_{j\ PW\ reset}$	130	135	155	°C	A
2.3	Thermal hysteresis			Dt		20		K	A
3	**Output specifications (1L - 4L, 1H - 4H)**								
3.1	On-resistance	I_{out} = 26 mA, T_j = 125°C	2, 7, 10, 15	$R_{DSONLOW}$	3	4	7	Ω	A
3.2	On-resistance	I_{out} = 26 mA, T_j = 125°C	1, 8, 9, 16	$R_{DSONHIGH}$	4	6.25	10	Ω	A
3.3	Output leakage current	$V_{LSIDE\ 1-4}$ = 17.5 V	2, 7, 10, 15	$I_{LOWSIDE}$			5	µA	A
3.4	Output leakage current	$V_{HSIDE\ 1-4}$ = 0.5 V	1, 8, 9, 16	$I_{HIGHSIDE}$			-5	µA	A
3.5	Output leakage steepness		1-2, 7-10, 15-16	$dV_{OUT/\ dt}$	50	200	400	mV/µs	D
3.6	Over current limitation		1, 8, 9, 16	$I_{HIGHSIDE}$	27	45	95	mA	A
3.7	Over current limitation		2, 7, 10, 15	$I_{LOWSIDE}$	27	45	80	mA	A
4	**Serial interface - inputs: CS, CLK and DATA**								
4.1	Input voltage low level threshold		11-13	V_{ILOW}			$0.2\times V_{VCC}$	V	A
4.2	Input voltage high level threshold		11-13	V_{IHIGH}	$0.7\times V_{VCC}$			V	A
4.3	Hysteresis of input voltage		11-13	ΔV_i		300		mV	A
4.4	Pull-down current	(internal pull-up resistor: 30 kΩ to 140 kΩ)	11-13	I_i			300	µA	A
5	**Serial interface - output: STATUS**								
5.1	Output voltage low level	I = 1 mA		V_{OLOW}			0.5	V	A
5.2	Output voltage high level	I = 1 mA		V_{OHIGH}	V_{VCC}-1		V_{VCC}	V	A

*) Type means: A =100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Application Circuit

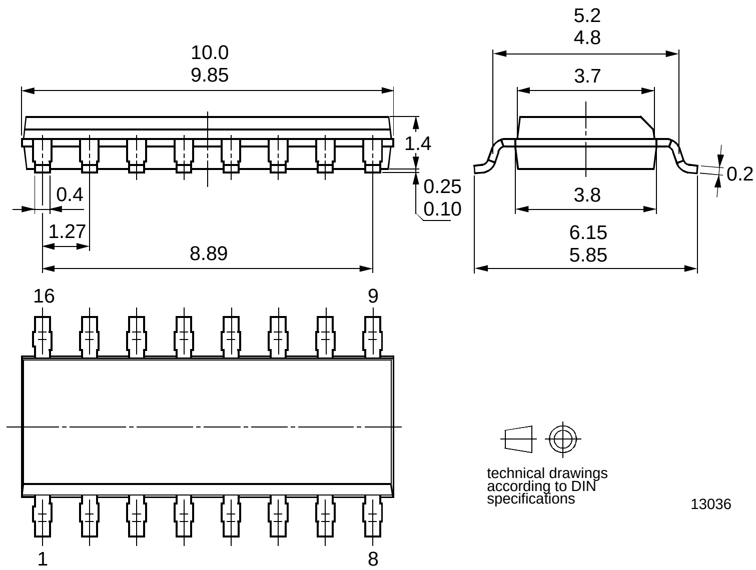
Figure 5.



Note: It is strongly recommended to connect the blocking capacitors at VS and VCC as close as possible to the power supply and GND pins. Recommended value for VS:< 100 µF electrolytic in parallel with 100 nF ceramic. Value for electrolytic capacitor depend on externel loads, noise and surge immunity efforts. Recommended value for VCC: 33 µF electrolytic in parallel with 100 nF ceramic. The 4-Ω resistors connected to the Pins HS1 - HS4 support the protection in case of a short of these pins to V_{Batt}.

Package Information

Package SO16
Dimensions in mm



Ozone Depleting Substances Policy Statement

It is the policy of **Atmel Germany GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Atmel Germany GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Atmel Germany GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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