

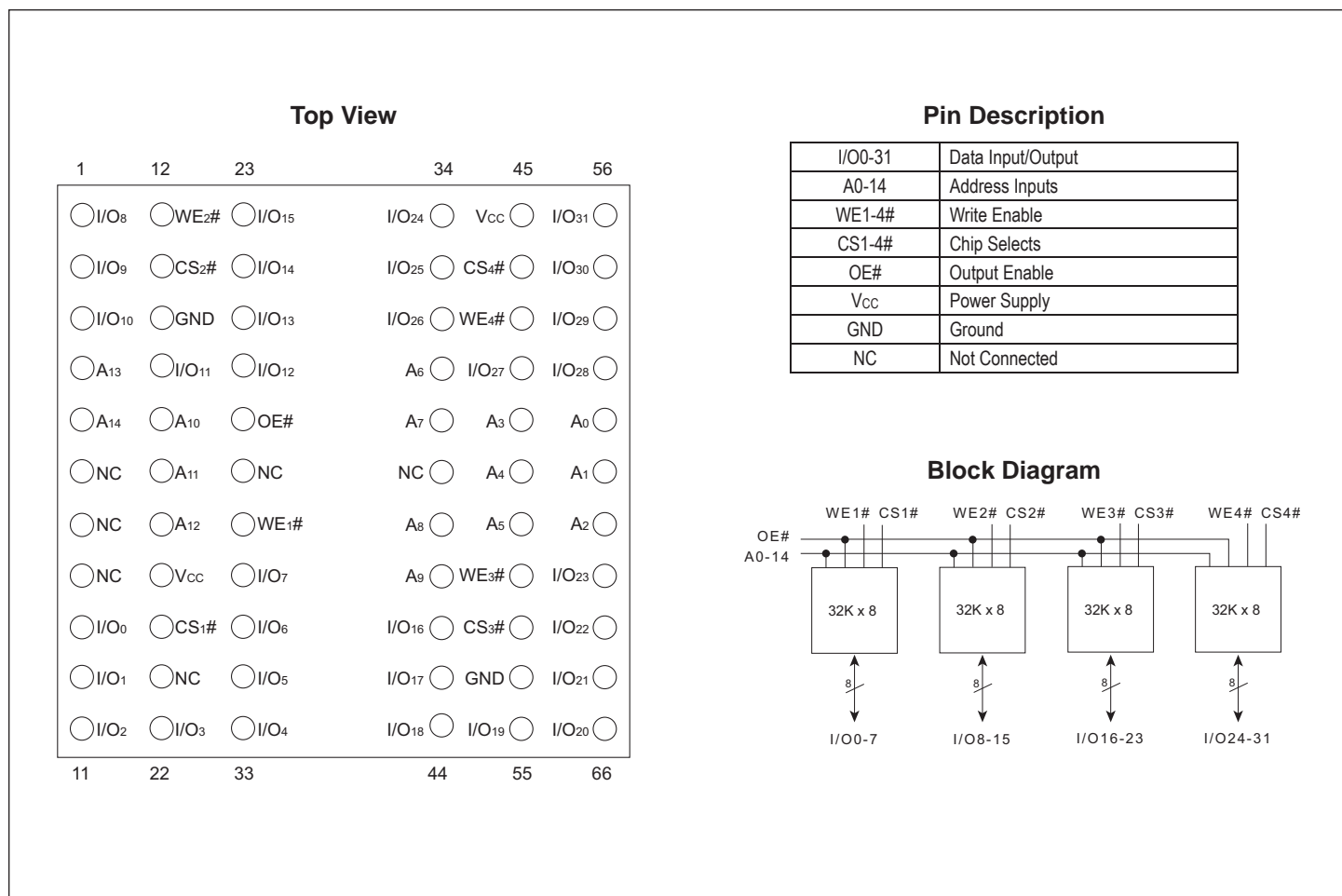
## 32Kx32 EEPROM MODULE, SMD 5962-94614

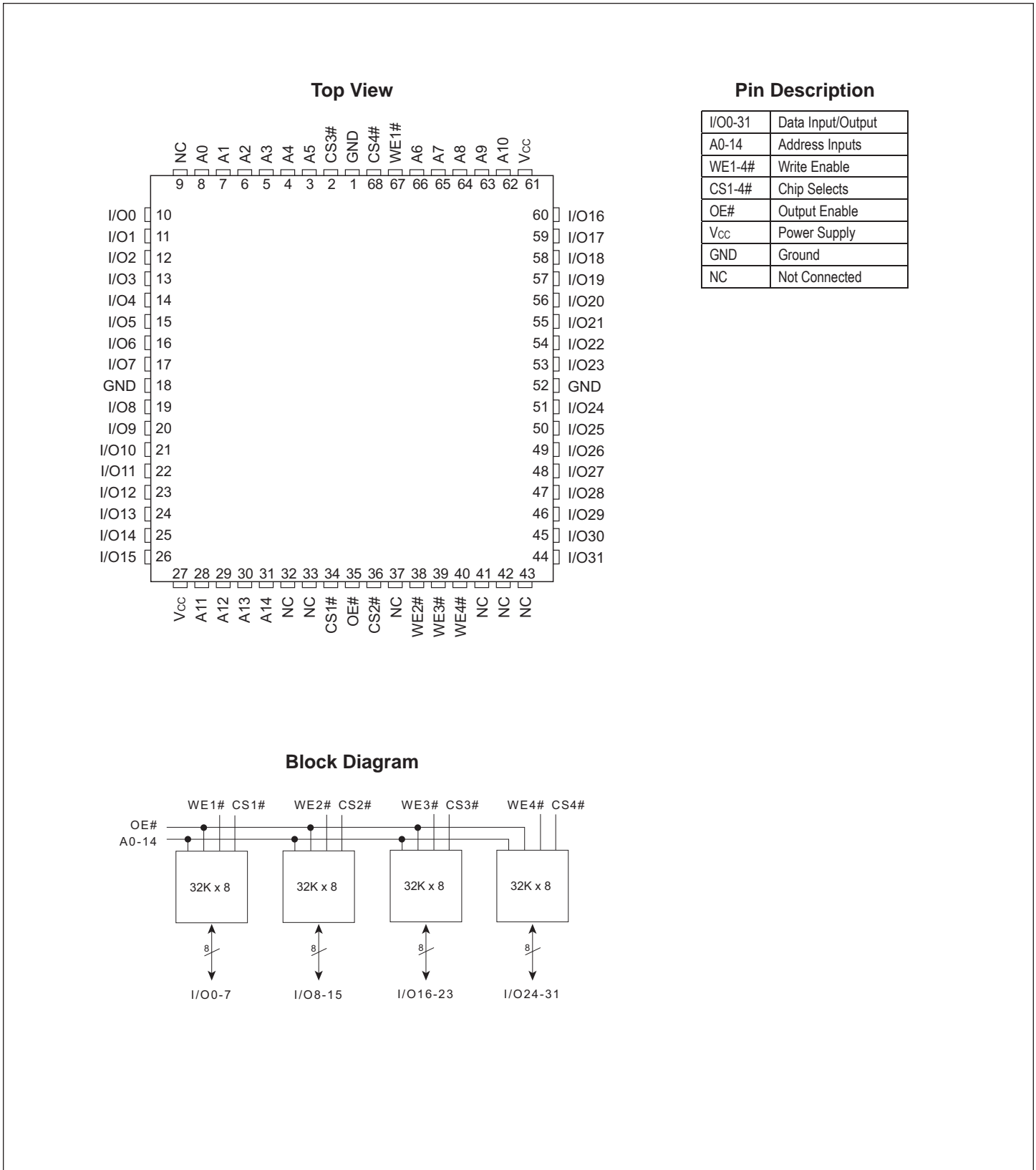
### FEATURES

- Access Times of 125 and 150ns
- MIL-STD-883 Compliant Devices Available
- Packaging:
  - 68 lead, Hermetic CQFP (G2U), 122.4mm (0.880") square, 3.56mm (0.140") height (Package 510).
  - 66-pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400)
- Data Retention at 25°C, 10 Years
- Write Endurance, 10,000 Cycles
- Organized as 32Kx32; User Configurable 64Kx16 or 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- Automatic Page Write Operation
- Page Write Cycle Time: 10ms Max
- Data Polling for End of Write Detection
- Hardware and Software Data Protection
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS, 10mA Standby Typical
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation

\* This product is subject to change without notice.

**FIGURE 1 – PIN CONFIGURATION FOR WE32K32N-XH1X**



**FIGURE 2 – PIN CONFIGURATION FOR WE32K32-XG2UX**


**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol		Unit
Operating Temperature	$T_A$	-55 to +125	°C
Storage Temperature	$T_{STG}$	-65 to +150	°C
Signal Voltage Relative to GND	$V_G$	-0.6 to + 6.25	V
Voltage on OE# and A9		-0.6 to +13.5	V

**NOTE:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Min	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.5	V
Input High Voltage	$V_{IH}$	2.0	$V_{CC} + 0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	+0.8	V
Operating Temp. (Mil.)	$T_A$	-55	+125	°C
Operating Temp. (Ind.)	$T_A$	-40	+85	°C

**TRUTH TABLE**

CS#	OE#	WE#	Mode	Data I/O
H	X	X	Standby	High Z
L	L	H	Read	Data Out
L	H	L	Write	Data In
X	H	X	Out Disable	High Z/Data Out
X	X	H	Write	
X	L	X	Inhibit	

**CAPACITANCE**
 $T_A = +25^\circ\text{C}$ 

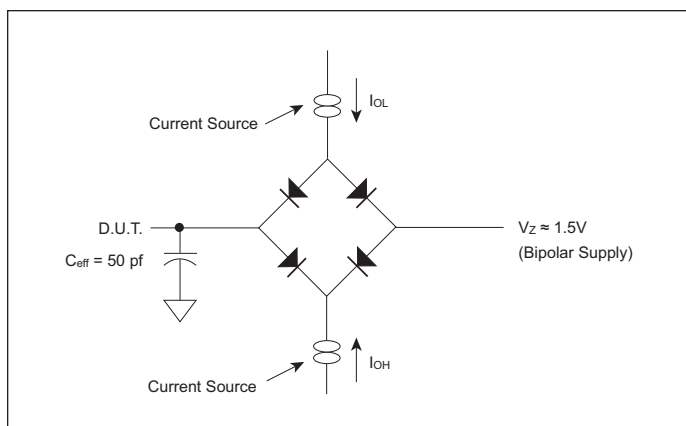
Parameter	Symbol	Conditions	Max	Unit
Address input capacitance OE# capacitance	$C_{AD}$ $C_{OE}$	$V_{IN} = 0\text{ V}, f = 1.0\text{ MHz}$	50	pF
WE# capacitance	$C_{WE}$	$V_{IN} = 0\text{ V}, f = 1.0\text{ MHz}$	50	pF
CS1-4# capacitance	$C_{CS}$	$V_{IN} = 0\text{ V}, f = 1.0\text{ MHz}$	25	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O} = 0\text{ V}, f = 1.0\text{ MHz}$	40	pF

This parameter is guaranteed by design but not tested.

**DC CHARACTERISTICS**
 $V_{CC} = 5.0\text{V}, \text{GND} = 0\text{V}, -55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ 

Parameter	Symbol	Conditions	-80		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	$I_{LI}$	$V_{CC} = 5.5, V_{IN} = \text{GND to } V_{CC}$		10		10		10		10	$\mu\text{A}$
Output Leakage Current	$I_{LOx32}$	$\text{CS\#} = V_{IH}, \text{OE\#} = V_{IH}, \text{VoUT} = \text{GND to } V_{CC}$		10		10		10		10	$\mu\text{A}$
Operating Supply Current (x32)	$I_{CCx32}$	$\text{CS\#} = V_{IL}, \text{OE\#} = V_{IH}, f = 5\text{MHz}$		320		250		200		150	mA
Standby Current	$I_{SB}$	$\text{CS\#} = V_{IH}, \text{OE\#} = V_{IH}, f = 5\text{MHz}$		2.5		2.5		2.5		2.5	mA
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}, V_{CC} = 4.5\text{V}$		0.45		0.45		0.45		0.45	V
Output High Voltage	$V_{OH}$	$I_{OH} = -400\mu\text{A}, V_{CC} = 4.5\text{V}$	2.4		2.4		2.4		2.4		V

NOTE: DC test conditions:  $V_{IH} = V_{CC} - 0.3\text{V}, V_{IL} = 0.3\text{V}$

**FIGURE 3 – AC TEST CIRCUIT**

**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:  $V_Z$  is programmable from -2V to +7V.

$I_{OL}$  &  $I_{OH}$  programmable from 0 to 16mA.

Tester Impedance  $Z_0 = 75\Omega$ .

$V_Z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .

$I_{OL}$  &  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.

## WRITE

A write cycle is initiated when OE# is high and a low pulse is on WE# or CS# with CS# or WE# low. The address is latched on the falling edge of CS# or WE# whichever occurs last. The data is latched by the rising edge of CS# or WE#, whichever occurs first. A byte write operation will automatically continue to completion.

The WE# line transition from high to low also initiates an internal 150 µsec delay timer to permit page mode operation. Each subsequent WE# transition from high to low that occurs before the completion of the 150 µsec time out will restart the timer from zero. The operation of the timer is the same as a retriggerable one-shot.

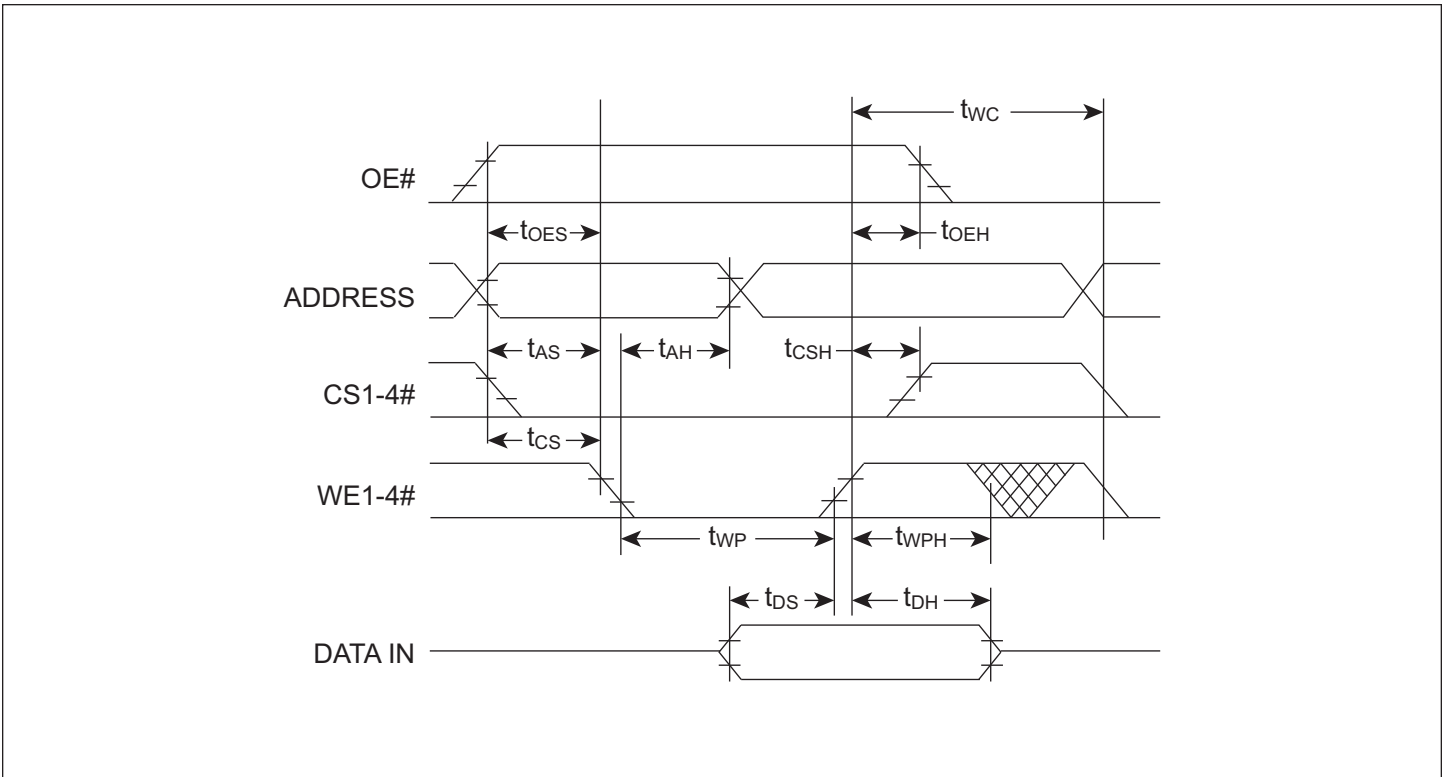
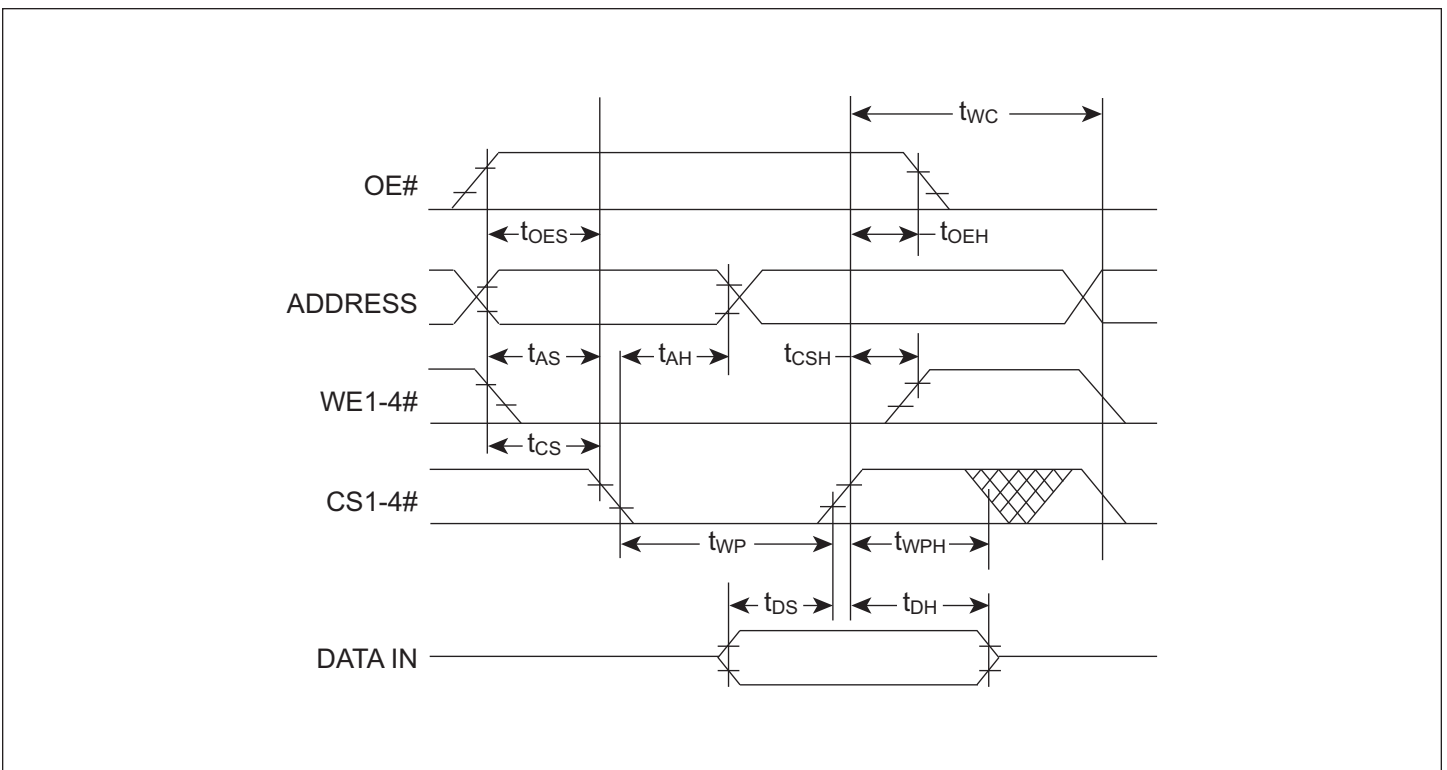
## WRITE CYCLE TIMING

Figures 4 and 5 show the write cycle timing relationships. A write cycle begins with address application, write enable and chip select. Chip select is accomplished by placing the CS# line low. Write enable consists of setting the WE# line low. The write cycle begins when the last of either CS# or WE# goes low.

### AC WRITE CHARACTERISTICS

V<sub>CC</sub> = 5.0V, GND = 0V, -55°C ≤ T<sub>A</sub> ≤ +125°C

WRITE CYCLE Write Cycle Parameter	Symbol	-80		-90		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time, TYP = 6ms	t <sub>WC</sub>		10		10		10		10	ms
Address Set-up Time	t <sub>AS</sub>	0		0		30		30		ns
Write Pulse Width (WE# or CS#)	t <sub>WP</sub>	100		100		150		150		ns
Chip Select Set-up Time	t <sub>CS</sub>	0		0		0		0		ns
Address Hold Time	t <sub>AH</sub>	50		50		100		100		ns
Data Hold Time	t <sub>DH</sub>	0		0		10		10		ns
Chip Select Hold Time	t <sub>CSH</sub>	0		0		0		0		ns
Data Set-up Time	t <sub>DS</sub>	50		50		100		100		ns
Write Pulse Width High	t <sub>WPH</sub>	50		50		50		50		ns
Output Enable Set-up Time	t <sub>OES</sub>	10		10		10		10		ns
Output Enable Hold Time	t <sub>OEH</sub>	10		10		10		10		ns

**FIGURE 4 – WRITE WAVEFORMS WE# CONTROLLED**

**FIGURE 5 – WRITE WAVEFORMS CS# CONTROLLED**


## READ

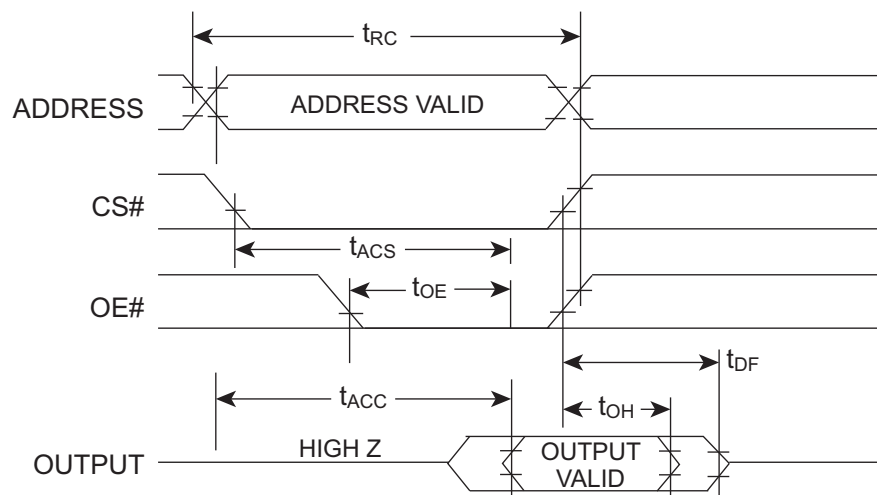
The WE32K32-XXX stores data at the memory location determined by the address pins. When CS# and OE# are low and WE# is high, this data is present on the outputs. When CS# and OE# are high, the outputs are in a high impedance state. This 2 line control prevents bus contention.

### AC READ CHARACTERISTICS (See Figure 6)

$V_{CC} = 5.0V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

READ CYCLE	Symbol	-80		-90		-120		-150		Unit
Parameter		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	$t_{RC}$	80		90		120		150		ns
Address Access Time	$t_{ACC}$		80		90		120		150	ns
CS Access Time	$t_{ACS}$		80		90		120		150	ns
Output Hold from Add. Change, OE# or CS#	$t_{OH}$	0		0		0		0		ns
Output Enable to Output Valid	$t_{OE}$		40		50		85		85	ns
Chip Select or OE# to Output in High Z	$t_{DF}$		40		50		70		70	ns

**FIGURE 6 – READ WAVEFORMS**



**NOTES:**

1. OE# may be delayed up to  $t_{ACS} - t_{OE}$  after the falling edge of CS# without impact on  $t_{OE}$  or by  $t_{ACC} - t_{OE}$  after an address change without impact on  $t_{ACC}$ .
2.  $t_{CHZ}$ ,  $t_{OHZ}$  are specified from OE# or CS# whichever occurs first ( $C_L = 5pF$ ).
3. All I/O transitions are measured  $\pm 200$  mV from steady state with loading as specified in "Load Test Circuits."

## DATA POLLING

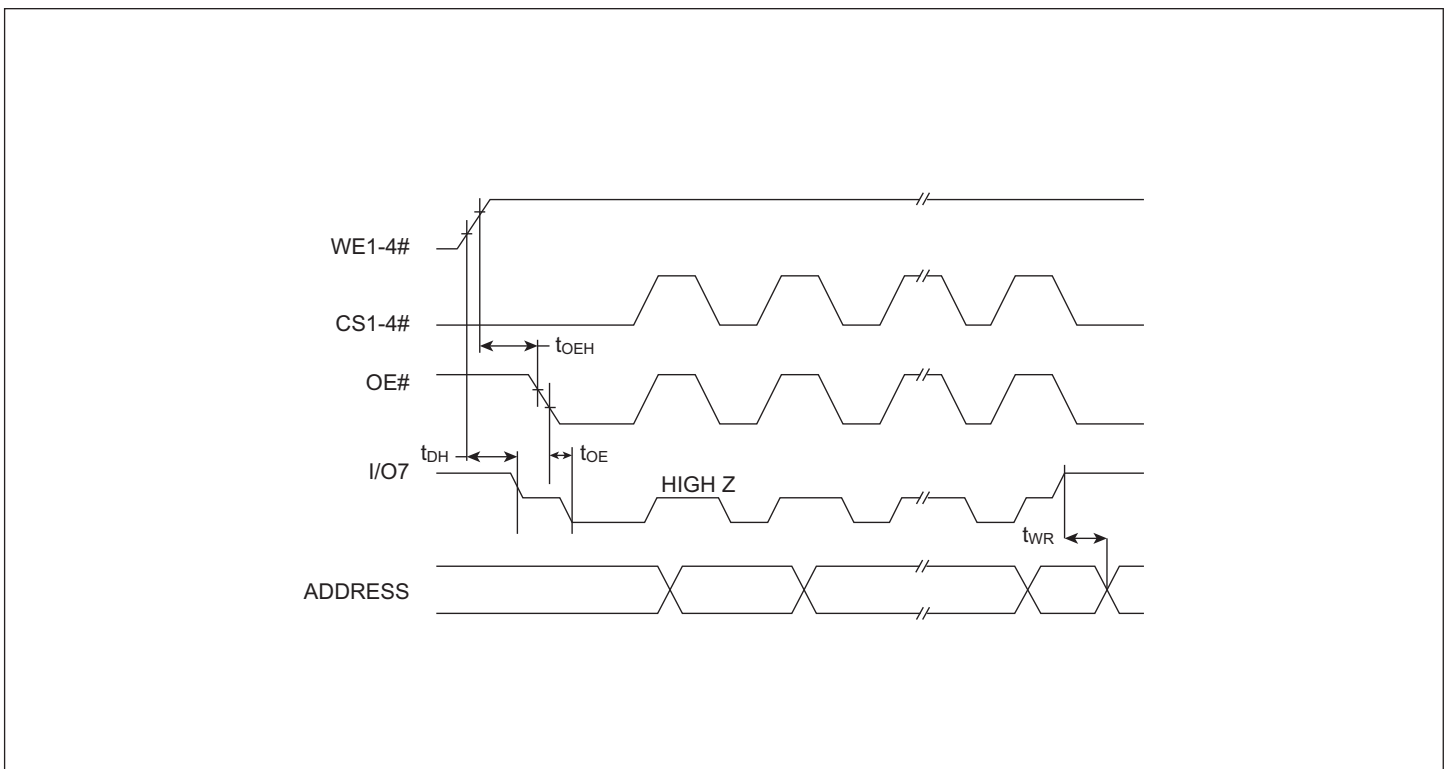
The WE32K32-XXX offers a data polling feature which allows a faster method of writing to the device. Figure 7 shows the timing diagram for this function. During a byte or page write cycle, an attempted read of the last byte written will result in the complement of the written data on D7 (for each chip.) Once the write cycle has been completed, true data is valid on all outputs and the next cycle may begin. Data polling may begin at any time during the write cycle.

## DATA POLLING CHARACTERISTICS

$V_{CC} = 5.0V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

Parameter	Symbol	Min	Max	Unit
Data Hold Time	$t_{DH}$	10		ns
OE# Hold Time	$t_{OE\#}$	10		ns
OE# To Output Valid	$t_{OE}$		100	ns
Write Recovery Time	$t_{WR}$	0		ns

**FIGURE 7 – DATA POLLING WAVEFORMS**



## PAGE WRITE OPERATION

The WE32K32-XXX has a page write operation that allows one to 64 bytes of data to be written into the device and consecutively loads during the internal programming period. Successive bytes may be loaded in the same manner after the first data byte has been loaded. An internal timer begins a time out operation at each write cycle. If another write cycle is completed within 150 $\mu$ s or less, a new time out period begins. Each write cycle restarts the delay period. The write cycles can be continued as long as the interval is less than the time out period.

The usual procedure is to increment the least significant address lines from A0 through A5 at each write cycle. In this manner a page of up to 64 bytes can be loaded in to the EEPROM in a burst mode before beginning the relatively long interval programming cycle.

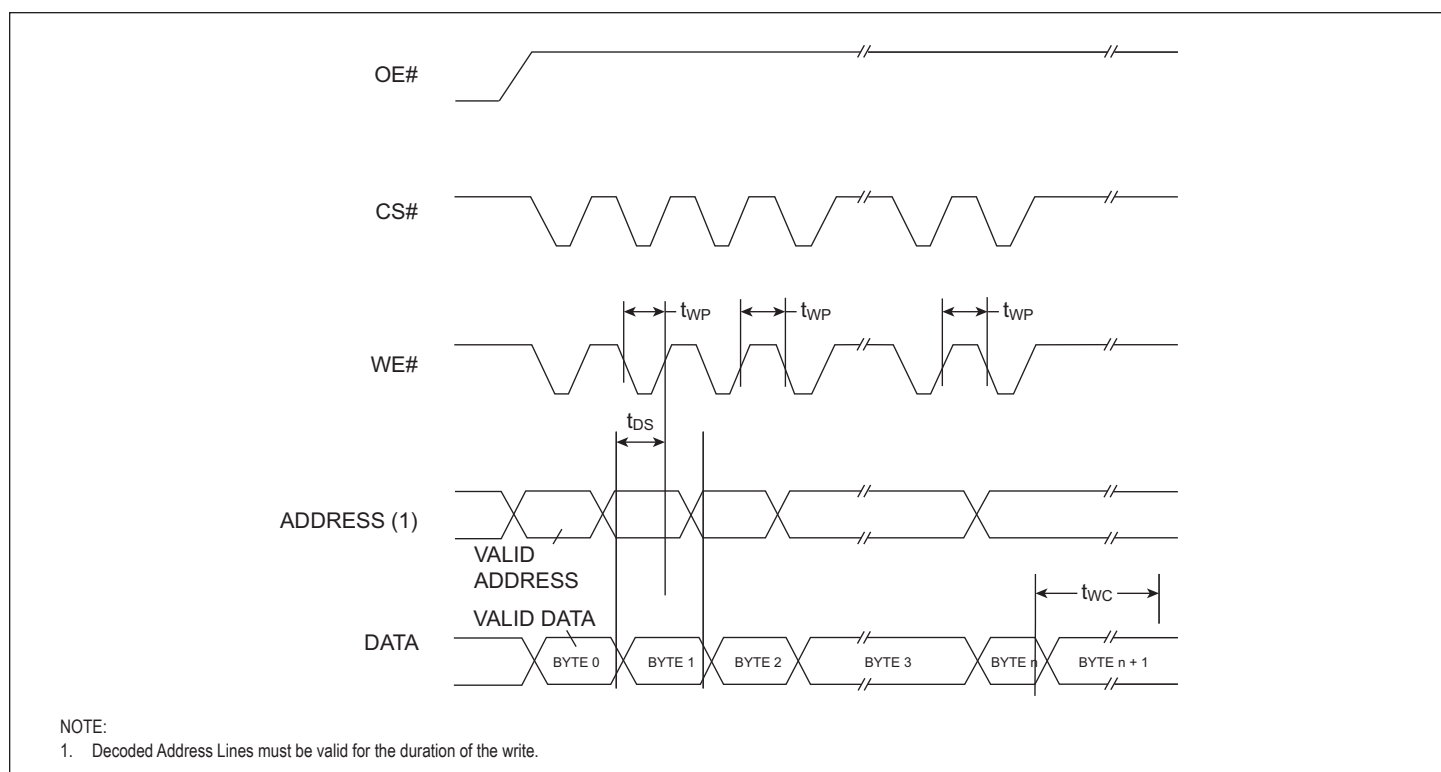
After the 150 $\mu$ s time out is completed, the EEPROM begins an internal write cycle. During this cycle the entire page of bytes will be written at the same time. The internal programming cycle is the same regardless of the number of bytes accessed.

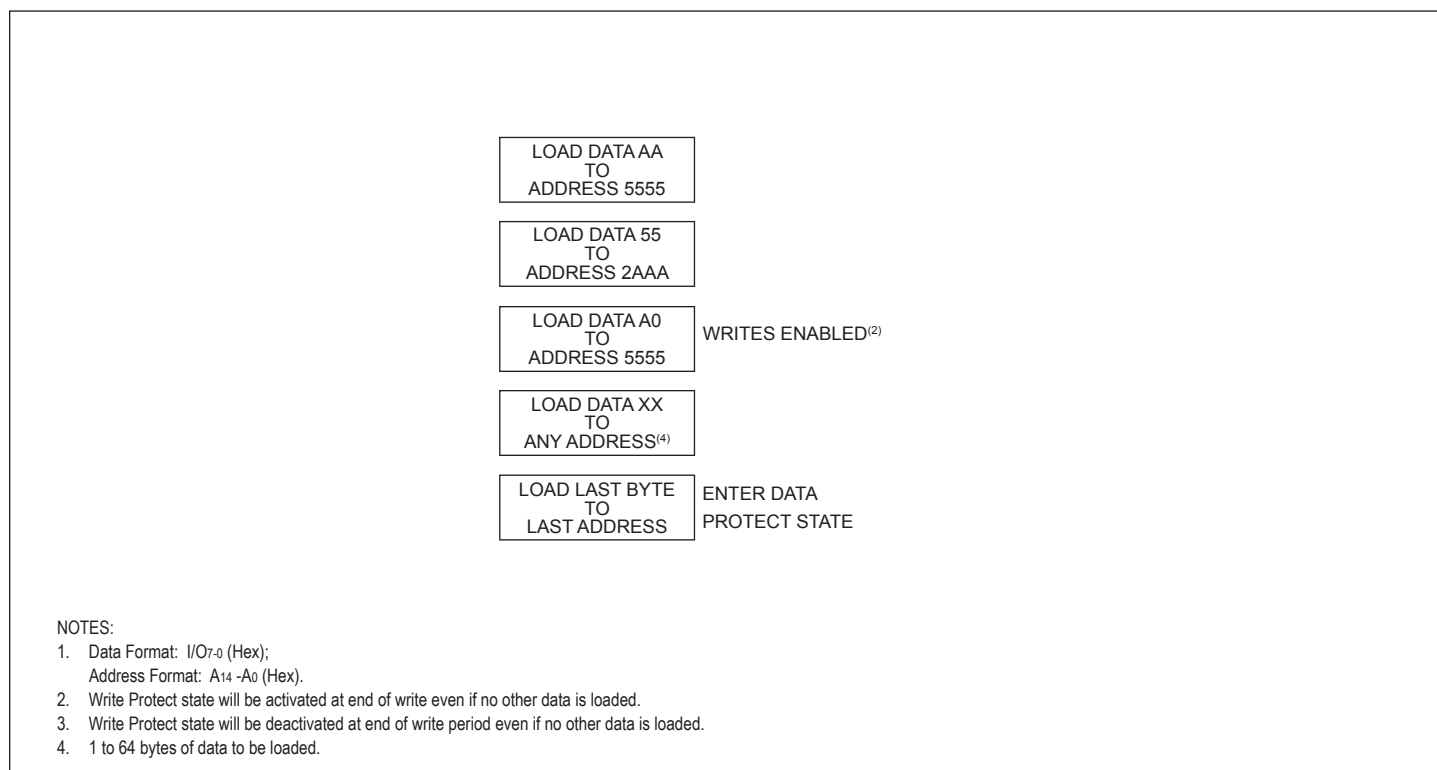
## PAGE WRITE CHARACTERISTICS

$V_{CC} = 5.0V, GND = 0V, -55^{\circ}C \leq T_A \leq +125^{\circ}C$

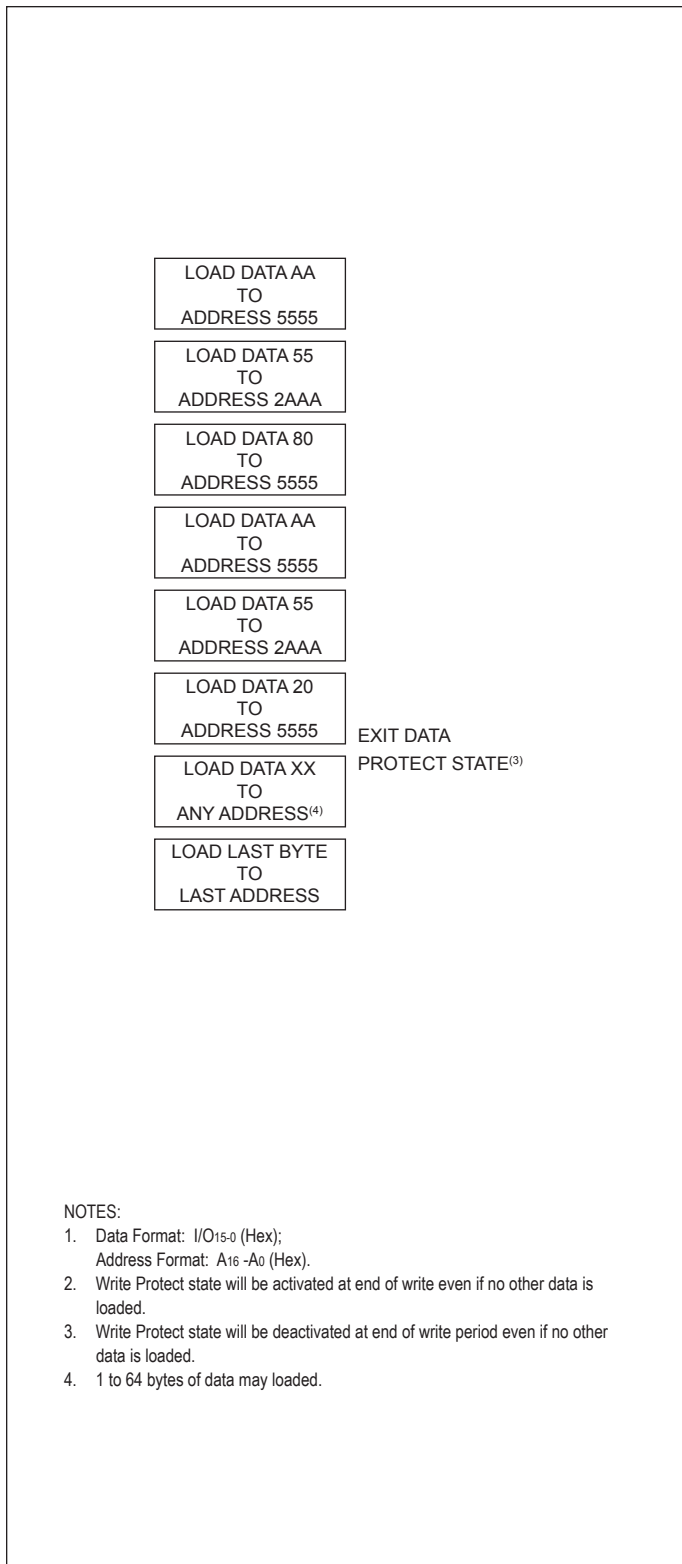
PAGE MODE WRITE CHARACTERISTICS Parameter	Symbol	-80		-90		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time, TYP = 6ms	$t_{WC}$		10		10		10		10	ms
Data Set-up Time	$t_{DS}$	50		50		100		100		ns
Data Hold Time	$t_{DH}$	0		0		10		10		ns
Write Pulse Width	$t_{WP}$	100		100		150		150		ns
Byte Load Cycle Time	$t_{BLC}$		150		150		150		150	$\mu$ s
Write Pulse Width High	$t_{WPH}$	50		50		50		50		ns

FIGURE 8 – PAGE WRITE WAVEFORMS



**FIGURE 9 – SOFTWARE BLOCK DATA PROTECTION ENABLE ALGORITHM<sup>(1)</sup>**

**FIGURE 10 –  
SOFTWARE BLOCK DATA PROTECTION DISABLE  
ALGORITHM<sup>(1)</sup>**



## SOFTWARE DATA PROTECTION

A software write protection feature may be enabled or disabled by the user. When shipped by White Microelectronics, the WE32K32-XXX has the feature disabled. Write access to the device is unrestricted.

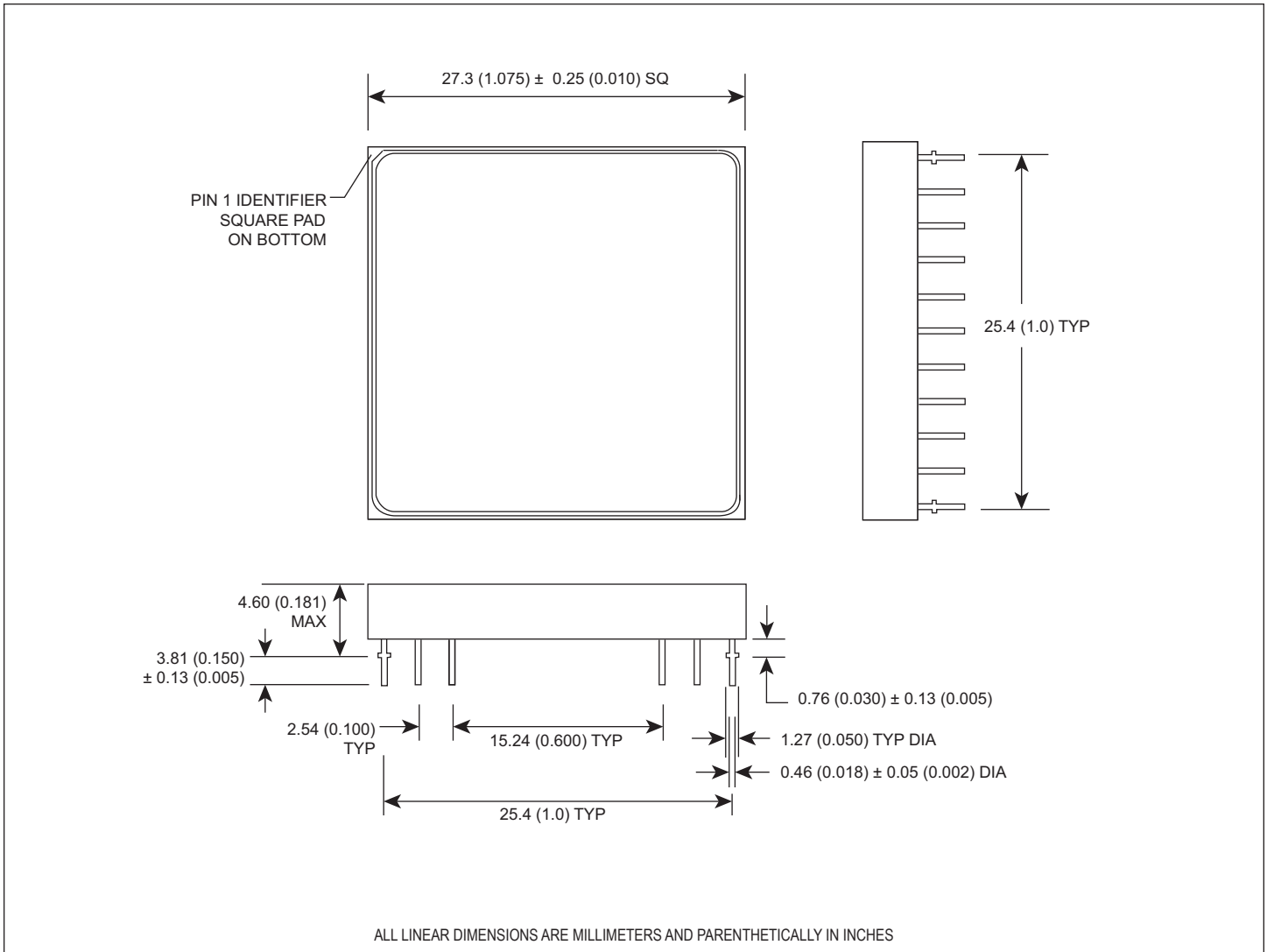
To enable software write protection, the user writes three access code bytes to three special internal locations. Once write protection has been enabled, each write to the EEPROM must use the same three byte write sequence to permit writing. After setting software data protection, any attempt to write to the device without the three-byte command sequence will start the internal write timers. No data will be written to the device, however, for the duration of *t<sub>wc</sub>*. The write protection feature can be disabled by a six byte write sequence of specific data to specific locations. Power transitions will not reset the software write protection.

Each 32KByte block of the EEPROM has independent write protection. One or more blocks may be enabled and the rest disabled in any combination. The software write protection guards against inadvertent writes during power transitions, or unauthorized modification using a PROM programmer.

## HARDWARE DATA PROTECTION

These features protect against inadvertent writes to the WE32K32-XXX. These are included to improve reliability during normal operation:

- Vcc power on delay**  
As Vcc climbs past 3.8V typical the device will wait 5msec typical before allowing write cycles.
- Vcc sense**  
While below 3.8V typical write cycles are inhibited.
- Write inhibiting**  
Holding OE# low and either CS# or WE# high inhibits write cycles.
- Noise filter**  
Pulses of <8ns (typ) on WE# or CS# will not initiate a write cycle.

**PACKAGE 400 – 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)**




**ORDERING INFORMATION**

	<b>W E 32K32 X - XXX X X X</b>
<b>MICROSEMI CORPORATION</b> _____	
<b>EEPROM</b> _____	
<b>ORGANIZATION, 32K x 32</b> _____ User Configurable as 64Kx16 or 128Kx8	
<b>IMPROVEMENT MARK</b> _____ N = No Connect at pins 8, 21, 28, and 39 in HIP for upgrade	
<b>ACCESS TIME (ns)</b> _____	
<b>PACKAGE TYPE:</b> _____ H1 = Ceramic Hex In-line Package, HIP (Package 400) G2U = 22.4mm Ceramic Quad Flat Pack, CQFP Low Profile (Package 510)	
<b>DEVICE GRADE:</b> _____ Q = Military Grade* M = Military Screened    -55°C to +125°C I = Industrial                -40°C to +85°C C = Commercial              0°C to +70°C	
<b>LEAD FINISH:</b> _____ Blank = Gold plated leads A = Solder dip leads	

\* This product is processed the same as the 5962-XXXXHXX product but all test and mechanical requirements are per the Microsemi data sheet.

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
32K x 32 EEPROM Module	150ns	66 pin HIP (H1)	5962-94614 01HXX
32K x 32 EEPROM Module	125ns	66 pin HIP (H1)	5962-94614 02HXX
32K x 32 EEPROM Module	90ns	66 pin HIP (H1)	5962-94614 03HXX
32K x 32 EEPROM Module	150ns	68 lead CQFP/J (G2U)	5962-94614 01HZX
32K x 32 EEPROM Module	125ns	68 lead CQFP/J (G2U)	5962-94614 02HZX
32K x 32 EEPROM Module	90ns	68 lead CQFP/J (G2U)	5962-94614 03HZX

**Document Title**

32Kx32 EEPROM MODULE, SMD 5962-94614

**Revision History**

<b>Rev #</b>	<b>History</b>	<b>Release Date</b>	<b>Status</b>
Rev 6	Changes (Pg. 1-14) 6.1 Change document layout from White Electronic Designs to Microsemi 6.2 Add document Revision History page	August 2011	Final
Rev 7	Changes (Pg. 1, 13) 7.1 Change 120ns to 125ns 7.2 Remove 80ns to 90ns	September 2012	Final
Rev 8	Change (Pg. 13) 8.1 Changed Device Grade "Q" description from "MIL-STD-883 Compliant" to "MIL-PRF-38534 Class H Compliant."	May 2014	Final
Rev 9	Change (Pg. 13) 9.1 Changed Device Grade "Q" description from "MIL-PRF-38534 Class H Compliant" to "Military Grade."	August 2014	Final