Color Palette with Triple 6-Bit DAC

The TMC0171 and TMC0176 are triple 6-bit video DACs with 256 x 18 RAM look-up tables and microprocessor interfaces. The devices were designed specifically for high resolution color graphics, supporting 256 simultaneous colors out of a palette of over a quarter million, at update rates fast enough to generate all common PC display resolutions.

The TTL microprocessor interface allows easy integration into personal computer systems. The three outputs are compatible with RS-170, allowing for a system design using a minimum of external components.

A pixel word mask facilitates such special effects as animation, overlays, and paged graphics without rewriting image RAM or the color look-up table.

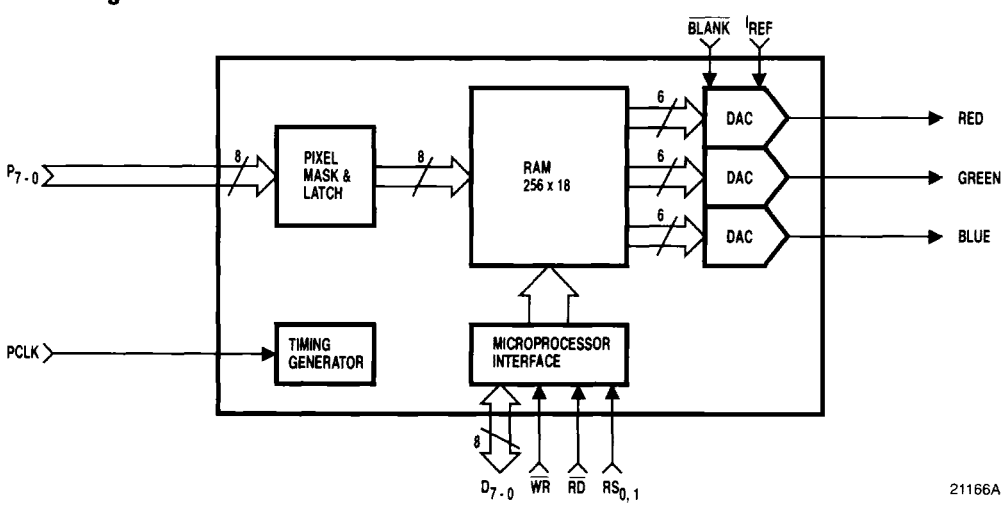
The TMC0171 is pin and function compatible with the industry standard IMS G171 high performance CMOS color look-up table DAC manufactured by Inmos, and the TMC0176 is pin and function compatible with the IMS G176.

Features

- Pixel Rates Of 0 to 80MHz
- 256 x 18 Bit Color Palette
- Color Palette Read-Back
- 75Ω RGB Analog Video Outputs
- Composite Blank
- Single +5V Power Supply
- Low Power Consumption
- TTL Compatible Inputs
- Asynchronous μP Interface
- Available In A 28 Pin Plastic DIP Or 44 Leaded PLCC

B

Interface Diagram



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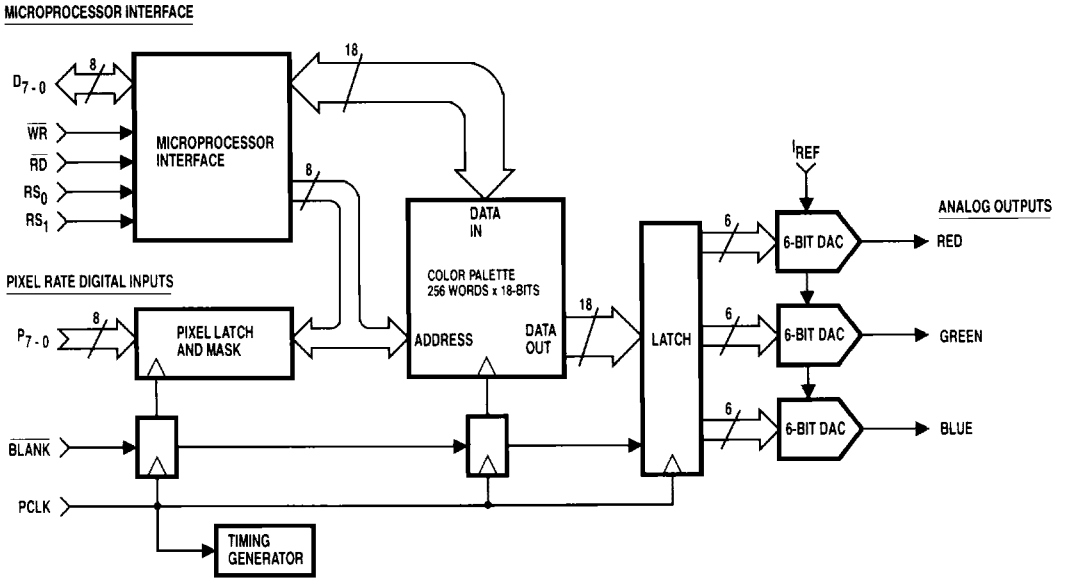
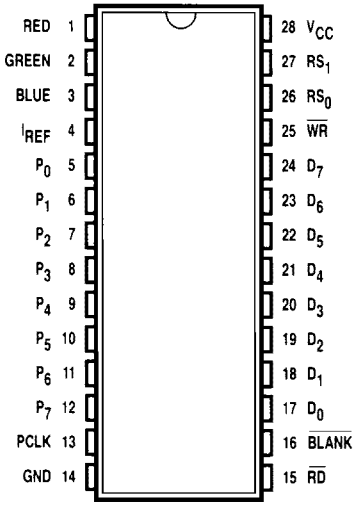
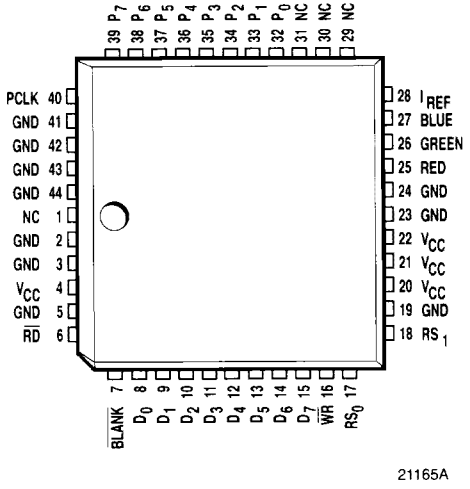
Functional Block Diagram



Pin Assignments



28 Pin Plastic DIP – N6 Package



44 Lead Plastic J-Leaded Chip Carrier – R2 Package

Functional Description

General Information

The TMC0171 and TMC0176 contain a Color Palette with 256 memory locations that are 18 bits wide. The color palette's output is connected to three high-speed current output 6-bit video DACs. The devices on-board registers easily interface with microprocessors.

Microprocessor Interface

The Microprocessor interface consists of three internal registers: Pixel Address Register, Color Value Register and Pixel Mask Register. These are individually accessed by register select signals, RS_0 and RS_1. The following table defines which register is selected by the logic states of RS_0 and RS_1:

RS_0	RS_1	Register
0	0	Pixel Address ($\overline{WRITE}$ Mode)
1	1	Pixel Address ($\overline{READ}$ Mode)
1	0	Color Value
0	1	Pixel Mask

The contents of the color palette can be accessed through the Color Value and Pixel Address registers.

All operations on the microprocessor interface can take place asynchronously to the pixel information being processed by the Color Palette.

The Pixel Address register is a byte-wide latch that receives and latches address information applied to pins P_{7-0}. It can be used in $\overline{READ}$ or $\overline{WRITE}$ mode, depending on the logic state of RS_0 and RS_1. With $RS_0 = RS_1 = 0$ (register select = 0, 0), the Pixel Address register is in the $\overline{WRITE}$ mode. To update one of the color palette's entries, the user writes the address into the Pixel Address register, then its red, green, and blue color definitions into the Color Value register. Refer to *Figures 10* and *11*.

When $RS_0 = RS_1 = 1$ (register select = 1, 1), the Pixel Address register is in the $\overline{READ}$ mode. To read one of the color palette's entries, the user writes its address into the Pixel Address register and then reads the three color definition components. The color definition data input/output sequence is always RED, GREEN, BLUE. Refer to *Figures 9, 12,* and *13*.

The 18-bit Color Value register, used as a buffer between the microprocessor interface and the color palette, is accessed by setting $RS_0 = 1$ and $RS_1 = 0$. A color definition can be read from or written to this register by a sequence of three byte-wide transfers to this register address. When a byte is written to this register, only the least significant six bits (D_{5-0}) are used. When a byte is read from this register address, only the six least significant bits contain information – the most significant two bits are set to zero. Refer to *Figures 9-13*.

After the $\overline{WRITE}$ sequence is completed, the Color Value register's contents are written to the specified color palette address stored in the Pixel Address register. Finally, the Pixel Address register is automatically incremented.

The color definitions can be read from the color palette. After setting RS_0 and RS_1 to 1, the user stores the desired color palette address in the Pixel Address register. The color definition (18 bits) in that color palette location is then transferred to the Color Value register and the Pixel Address is auto-incremented. With successive $\overline{READ}$ cycles, the color definitions pointed to by the incremented address are transferred to the Color Value register. Refer to *Figure 12*.

Attempting to update the color palette when $\overline{BLANK}$ is not asserted results in the data from the Color Value register taking precedence over the bit mapping operation. The output of the three 6-bit DACs will be based on the color definition from the memory location specified by the Pixel Address register and not the address found on P_{7-0}. This conflict causes the DACs to generate unexpected output levels for up to two PCLK periods.

The Pixel Mask register is a byte-wide latch, accessed by the microprocessor interface, D_{7-0}, when $RS_0 = 0$ and $RS_1 = 1$. This register is used to mask selected bits of the Pixel Address values applied to inputs P_{7-0}. A "1" in any location in the Pixel Mask register sets the corresponding bit to zero. The operation of the Pixel Mask register does not affect the address of the color definition when the microprocessor accesses the color palette. The masking operation makes it possible to alter the displayed colors without altering the contents of external video memory or the internal color palette.

Writing to the Color Palette

A new color definition can be stored in the color palette by first specifying the initial address under $\overline{\text{WRITE}}$ mode. This address is stored in the Pixel Address register ($RS_0 = RS_1 = 0$). The initial address is followed by RED, GREEN and BLUE color definition data ($RS_0 = 1$, $RS_1 = 0$). These six-bit inputs are collected together in the Color Value register. This new color definition is then transferred to the location pointed to by the information in the Pixel Address register. As soon as this transfer is completed, the Pixel Address register is auto-incremented. This allows consecutive color palette locations to be updated without the microprocessor specifying each address. The host needs only to continue supplying the RED, GREEN and BLUE data for each consecutive address. Refer to *Figures 10* and *11*.

Reading from the Color Palette

To read a location in the color palette, an address is sent on the Data I/O lines (D_{7-0}) under $\overline{\text{READ}}$ mode and stored in the Pixel Address register ($RS_0 = RS_1 = 1$). The color definition contained in the specified location is then transferred to the Color Value register. Again, the Pixel Address register is auto-incremented. The color definition can now be retrieved with three sequential $\overline{\text{READ}}$ operations ($RS_0 = 1$, $RS_1 = 0$). The first byte placed on the Data I/O lines contains the RED value; the next is GREEN and the final is BLUE. The two most significant bits are set to zero in each case. In a manner similar to the $\overline{\text{WRITE}}$ mode, consecutive color palette locations can be read by simply specifying the beginning address and reading the color palette one or more times. Refer to *Figures 9, 12* and *13*.

If the Pixel address register is updated during a $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ operation, the current data sequence is terminated and a new $\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ operation is initialized.

Video Path

The Video path consists of the Pixel Latch and Mask (inputs P_{7-0}), color palette (256 18-bit wide RAM), 18-bit wide bus, and an 18-bit wide latch on the inputs of the three 6-bit high-speed video DACs. The video path uses a three clock cycle (PCLK) pipeline for the Pixel Address and $\overline{\text{BLANK}}$ inputs. These signals are latched on the rising edge of PCLK.

Analog Outputs

The analog outputs are designed to drive singly-terminated 75Ω loads to a peak-white amplitude of 0.7V.

The reference current (I_{REF}) for this output is set to 4.44mA. The analog outputs can also drive doubly-terminated 75Ω loads with I_{REF} set to 8.88mA.

The active LOW $\overline{\text{BLANK}}$ input forces the analog outputs to ground, ignoring the color definition selected by the Pixel Address. Each of the 63 current sources used in each of the 6-bit DACs produces 1/30 I_{REF}. Therefore, the magnitude of peak white voltage is a function of the output loading and is determined by:

$$V_{PEAK\ WHITE} = 2.1 \cdot I_{REF} \cdot R_L$$
$$V_{BLACK\ LEVEL} = 0V.$$

Signal Descriptions

Signal Name	Package Pin Number N6	Package Pin Number R2	Signal Type	Signal Description
Red Green Blue	1 2 3	25 26 27	O O O	These analog outputs of the 6-bit DACs are the currents used for each of the guns in an RGB (Red, Green, Blue) video display.
I_{REF}	4	28	I	The current forced out of this Reference Current Input pin to ground determines the current sourced by each of the 63 current source in each of the three 6-bit DACs. Each current source produces $I_{REF}/30$ when activated by the 6-bit digital input code.
P_{7-0}	12-5	39-32	I	The byte-wide information on these Pixel Address lines is latched and masked by the Pixel Mask Register. The resulting value addresses a location in the Color Palette RAM. P_0 = LSB.
PCLK	13	40	I	The rising edges of the Pixel Clock signal control the latching of the Pixel Address and Blanking Inputs. They also control the progress of these values through the three stage pipeline of the Color Palette the DACs to the outputs.
GND	14	2, 3, 5, 19, 23, 24, 41-44		This is the power supply ground connection.
V_{CC}	28	4, 20, 21, 22		This positive power supply pin is normally connected to +5V DC and bypassed with a 10μF tantalum capacitor.
$\overline{RD}$	15	6	I	When this $\overline{READ}$ bus control signal is LOW, information present on the internal data bus is available on the Data I/O lines (D_{7-0}).
$\overline{BLANK}$	16	7	I	This active LOW signal forces the DACs' outputs to zero. When $\overline{BLANK}$ is asserted, a video monitor's screen becomes blank and the DACs ignore any output values from the Color Palette. However, the Color Palette can still be updated through D_{7-0}.
D_{7-0}	24-17	15-8	I/O	These bidirectional Data I/O lines are used by the host microprocessor to $\overline{WRITE}$ information (using the active LOW $\overline{WR}$) into and $\overline{READ}$ information (using the active LOW $\overline{RD}$) from the TMC0171's Pixel Address, Color Value and Pixel Mask registers. During the $\overline{WRITE}$ cycle, the rising edge of $\overline{WR}$ latches the data into the selected register. The rising edge of $\overline{RD}$ determines the end of the $\overline{READ}$ cycle. With $\overline{RD}$ and $\overline{WR}$ both HIGH, the Data I/O lines go into a high-impedance state.
$\overline{WR}$	25	16	I	This active LOW $\overline{WRITE}$ signal controls the timing of the $\overline{WRITE}$ operations on the microprocessor interface inputs, D_{7-0}.
RS_0, RS_1	26, 27	17, 18	I	These Register Select lines select one of the three internal registers and are sampled during the falling edges of the enable signals ($\overline{RD}$ or $\overline{WR}$). See the *Functional Description* section for more information regarding the internal registers.
NC		1, 29-31		Not connected internally.

Timing Characteristics

Figure 1. System Timing Diagram

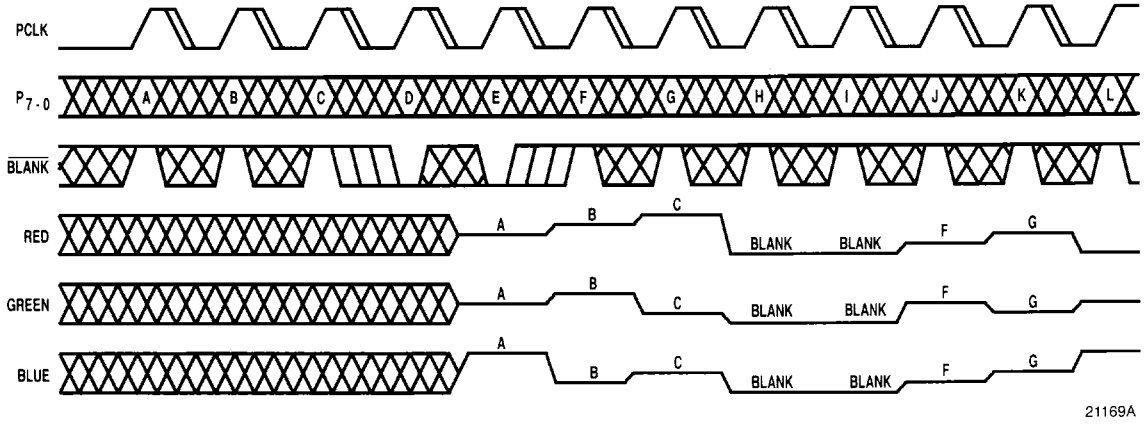


Figure 2. Timing Diagram Detailing Timing Specifications

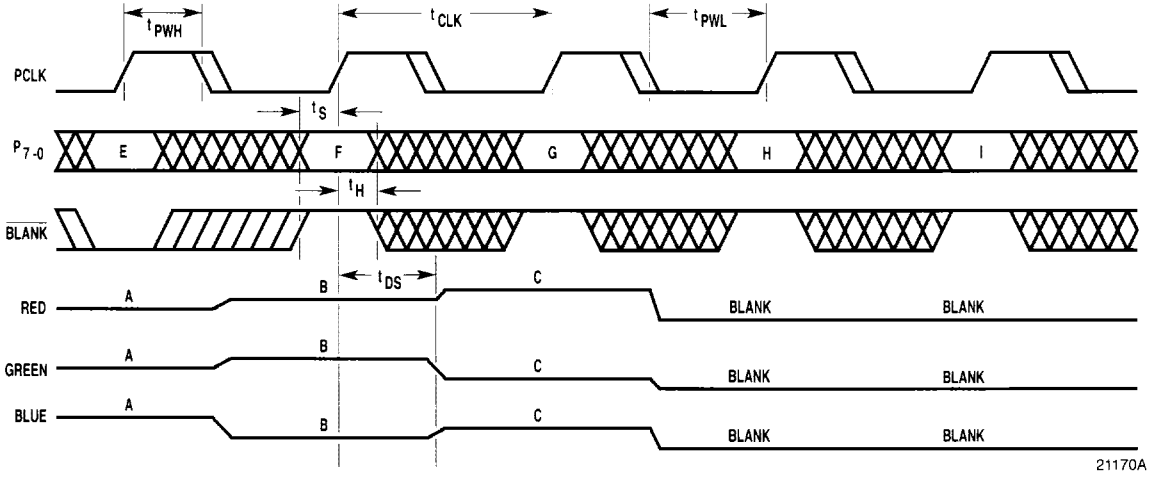


Figure 3. Basic $\overline{\text{WRITE}}$ Cycle Timing Diagram

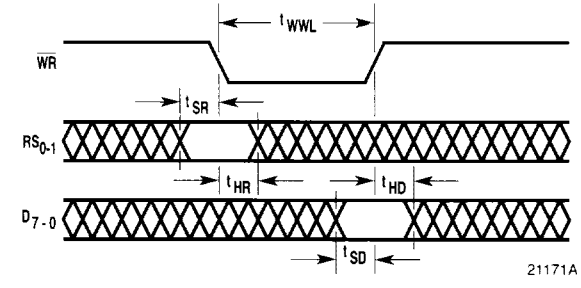


Figure 4. Basic $\overline{\text{READ}}$ Cycle Timing Diagram

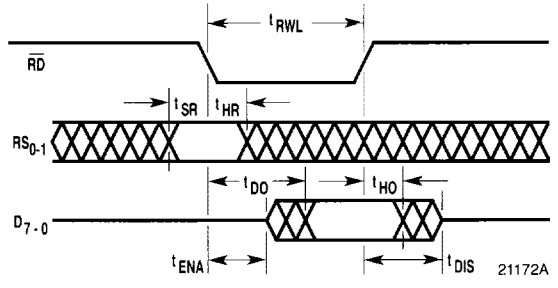
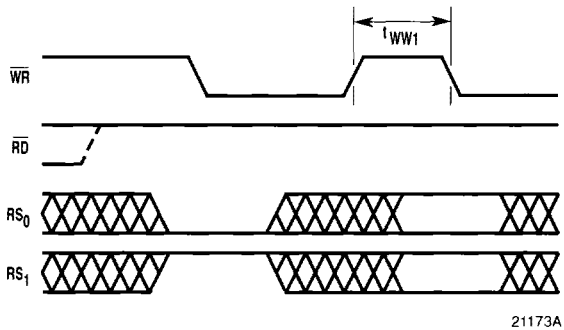


Figure 5. $\overline{\text{WRITE}}$ to Pixel Mask Register Followed by $\overline{\text{WRITE}}$ and $\overline{\text{READ}}$



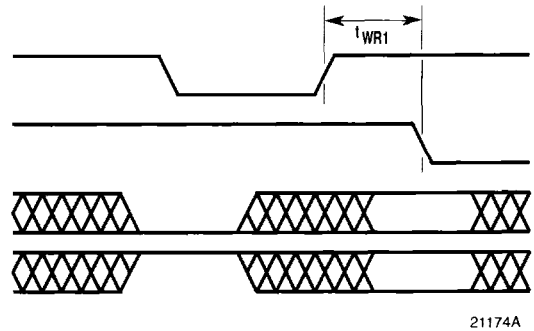


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Figure 6a. $\overline{\text{READ}}$ from Pixel Mask or Pixel Address Register ($\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Mode) Followed by $\overline{\text{READ}}$

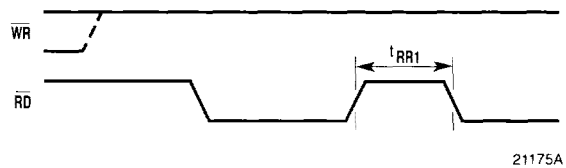

Figure 6b. $\overline{\text{READ}}$ from Pixel Mask or Pixel Address Register ($\overline{\text{READ}}$ or $\overline{\text{WRITE}}$ Mode) Followed by $\overline{\text{WRITE}}$

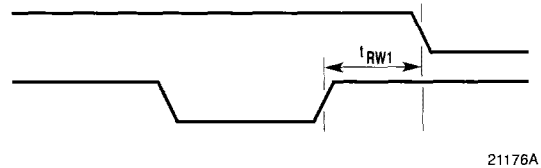

Figure 7. $\overline{\text{WRITE}}$ and $\overline{\text{READ}}$ Back Pixel Address Register ($\overline{\text{READ}}$ Mode)

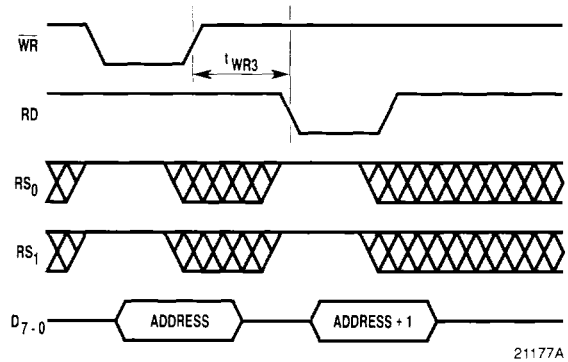

Figure 8. $\overline{\text{WRITE}}$ and $\overline{\text{READ}}$ Back Pixel Address Register ($\overline{\text{WRITE}}$ Mode)

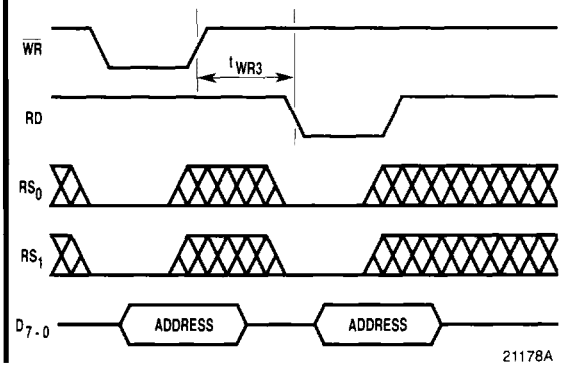

Figure 9. $\overline{\text{READ}}$ Color Value the $\overline{\text{READ}}$ Pixel Address Register ($\overline{\text{READ}}$ Mode)

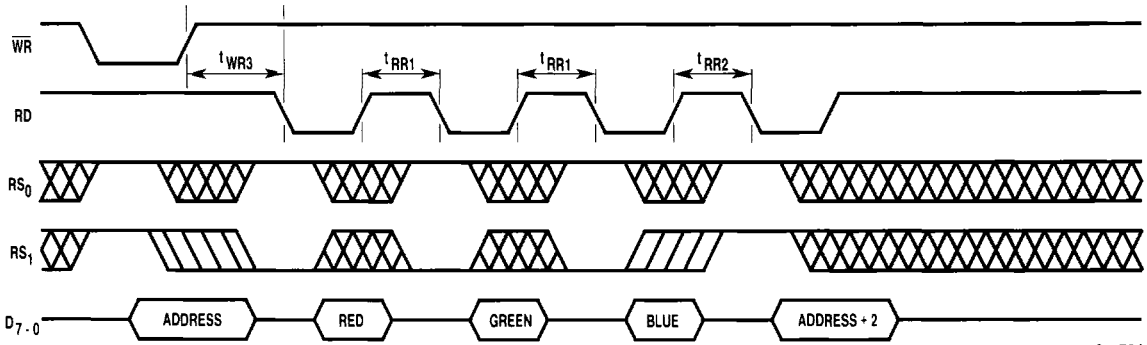

Figure 10. Color Value $\overline{\text{WRITE}}$ Followed by $\overline{\text{READ}}$

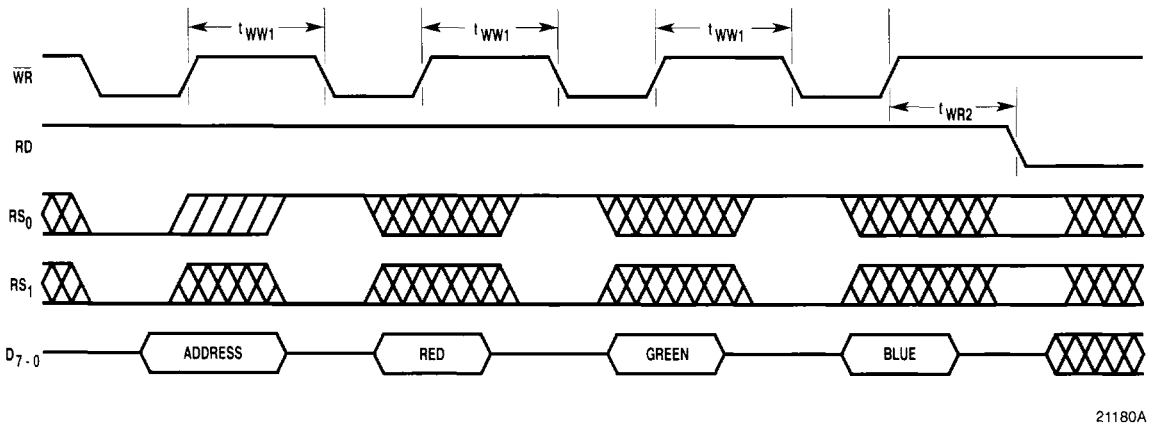

Figure 11. Color Value $\overline{\text{WRITE}}$ Followed by $\overline{\text{WRITE}}$

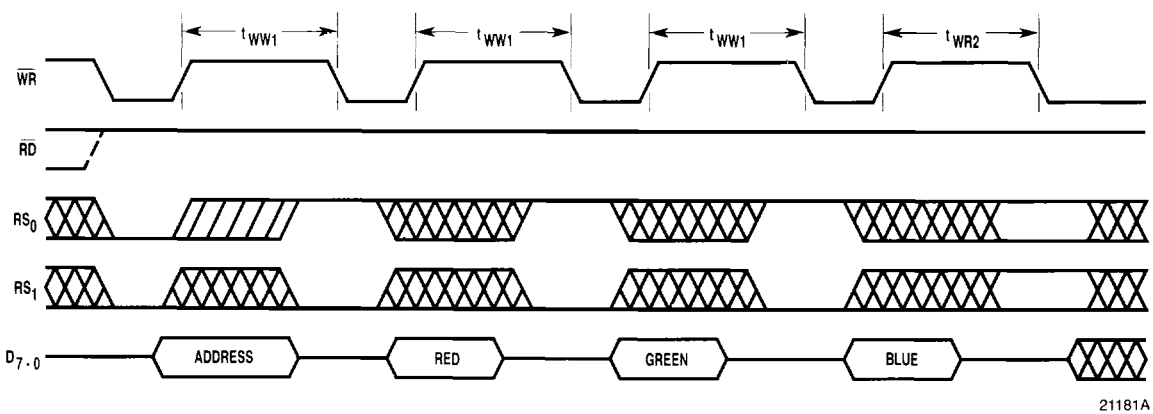

Figure 12. Color Value $\overline{\text{READ}}$ Followed by $\overline{\text{READ}}$

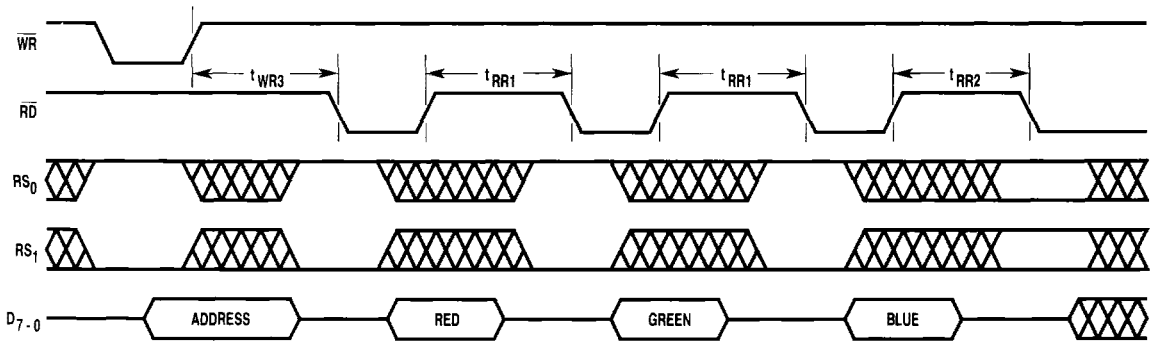

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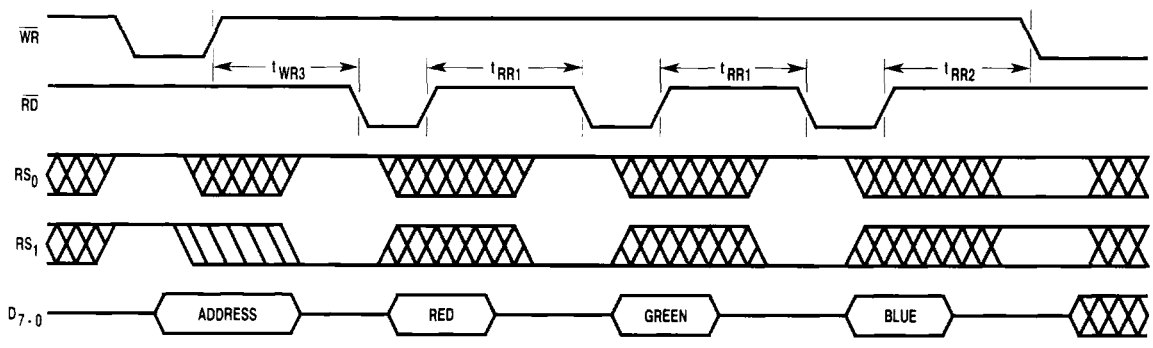
Figure 13. Color Value $\overline{\text{READ}}$ Followed by $\overline{\text{WRITE}}$



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Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to +7.0V
Temperature	
Operating, ambient	0°C to +70°C
Storage	−65 to +150°C

Note: [1] Stresses above those listed may damage the device permanently. Proper operation at these or any other conditions outside those listed in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating conditions

Parameter		Temperature Range: Standard, Min –, Min –4	Min –5	Min –6	Min –8	Max	Units
V_{CC}	Positive Supply Voltage (Measured to GND)	4.5	4.5	4.5	4.5	4.5	5.5	V
I_{REF}	Reference Input Current	−3	−3	−3	−3	−3	−10	mA
V_{IL}	Digital Input Voltage, Logic LOW	−0.5	−0.5	−0.5	−0.5	−0.5	0.8	V
V_{IH}	Digital Input Voltage, Logic HIGH	2.0	2.0	2.0	2.0	2.0	$V_{CC}+0.5$	V
I_{OL}	Output Current, Logic LOW						2.0	mA
I_{OH}	Output Current, Logic HIGH						−4.0	mA
t_{CLK}	PCLK Period	28	25	20	15	12		ns
Δt_C	PCLK Jitter [1]						±2.5	%
t_{PWL}	PCLK Width, LOW	9	8	6	5	4		ns
t_{PWH}	PCLK Width, HIGH	7	7	6	5	4		ns
t_S	Pixel Word or $\overline{BLANK}$ Setup Time [2]	5	4	4	3	3		ns
t_H	Pixel Word or $\overline{BLANK}$ Hold Time [2]	5	4	4	3	3		ns
t_{WWL}	$\overline{WR}$ Pulse Width, LOW	50	50	50	50	50		ns
t_{RWL}	$\overline{RD}$ Pulse Width, LOW	50	50	50	50	50		ns
t_{SR}	Register Select Setup Time	15	12	10	10	10		ns
t_{HR}	Register Select Hold TIme	15	12	10	10	10		ns
t_{SD}	$\overline{WR}$ Data Setup Time	15	12	10	10	10		ns
t_{HD}	$\overline{WR}$ Data Hold TIme	15	12	10	10	10		ns
t_{WW1}	Successive $\overline{WRITE}$ Interval	3	3	3	3	3		t_{CLK}
t_{WR1}	$\overline{WR}$ Followed by $\overline{READ}$ Interval	3	3	3	3	3		t_{CLK}
t_{RR1}	Successive $\overline{READ}$ Interval	3	3	3	3	3		t_{CLK}
t_{RW1}	$\overline{RD}$ Followed by $\overline{WRITE}$ Interval	3	3	3	3	3		t_{CLK}
t_{WW2}	$\overline{WR}$ after Color $\overline{WRITE}$ [3]	3	3	3	3	3		t_{CLK}
t_{WR2}	$\overline{RD}$ after Color $\overline{WRITE}$ [3]	3	3	3	3	3		t_{CLK}
t_{RR2}	$\overline{RD}$ after Color $\overline{READ}$ [3]	6	6	6	6	6		t_{CLK}
t_{RW2}	$\overline{WR}$ after Color $\overline{READ}$ [3]	6	6	6	6	6		t_{CLK}
t_{WR3}	$\overline{RD}$ after Read Address $\overline{WRITE}$ [3]	6	6	6	6	6		t_{CLK}
t_{TRW}	$\overline{READ}/\overline{WRITE}$ Enable Transition Time	50		50				ns
t_A	Ambient Temperature, Still Air	0	0	0	0	0	70	°C

Notes:
1. This parameter is the allowed variation in the pixel clock frequency. It does not permit the pixel clock period to vary below the minimum specified t_{CLK} value.
2. The color palette's pixel address must be valid for the specified minimum setup and hold times at each rising edge of PCLK (this requirement includes the blanking period).
3. This parameter allows synchronization between operations on the microprocessor interface and the pixel stream being processed by the color palette.

Electrical characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range: Standard Min	Temperature Range: Standard Max	Units
V_{OL}	Output Voltage, LOW	I_{OL} = Max		0.4	V
V_{OH}	Output Voltage, HIGH	I_{OH} = Max	2.4		V
C_I	Input Capacitance			7	pF
C_O	Output Capacitance			7	pF
C_{IO}	Input/Output Capacitance			16	pF
I_I	Input Leakage Current		−10	10	µA
I_{OZ}	Output Leakage Current		−10	10	µA
I_{CC}	Operating Supply Current	I_{OUT} = Max, Digital Outputs Unloaded, PCLK = 35MHz		150	mA
V_{REF}	Reference Voltage at I_{REF} Pin	V_{CC} = 4.5V, I_{REF} = 10mA	V_{CC} − 3		V
V_{OC}	Output Voltage Compliance	I_{OUT} < 10mA	1.5		V
I_{OC}	Output Current Compliance	V_{OUT} < 1V, I_{REF} < 10mA	21		mA
E_G	Absolute Gain Error [1]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA or ZL = 37.5Ω + 30pF, I_{REF} = 8.88mA		±5	%
ΔI_{OUT}	DAC to DAC Mismatch [2]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		±1	%
E_{LI}	Integral Linearity, Terminal Based [3]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		±0.5	LSB
t_R	Rise TIme [4]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		8	ns
t_{SET}	Full-Scale Setting Time [5]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		28	ns
GA	Glitch Area [6]	ZL = 75Ω + 30pF, I_{REF} = 4.44mA		200	pV-sec
C_A	DAC Output Capacitance	$\overline{BLANK}$ = Logic LOW		10	pF
$V_{\overline{BLANK}}$	Blanking Output Voltage	$\overline{BLANK}$ = Logic LOW, ZL = 75Ω + 30pF, I_{REF} = 4.44mA		±0.5	LSB
E_{OF}	Unadjusted Output Offset Error	$\overline{BLANK}$ = Logic HIGH, ZL = 75Ω + 30pF, I_{REF} = 4.44mA		±0.5	LSB

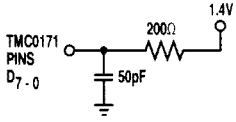
Notes:
1. Absolute gain error is defined as 100% [F.S I_{OUT} − 2.1 • I_{REF}/2.1 • I_{REF}, $V_{BLACK\ LEVEL}$ = 0V.
2. The listed value is relative to the midpoint of the full-scale distribution of the three DACs.
3. Zero and full-scale adjusted linearity error = [V_{OUT} − V_{OFFSET} − (D×VLSB)]/VLSB, where VLSB = ($V_{FULLSCALE}$ − V_{OFFSET})/63.
4. The rise time is measured for 10% to 90% of the full-scale transition.
5. The output signal's setting time is measured from a 2% change at the transition's initial value until it has settled to within 2% of the final value.
6. This value is determined using triangular approximation: glitch area = (area of positive transient) − (area of negative transient).

Switching characteristics within specified operating conditions

Parameter		Temperature Range: Standard – Min	– Max	–4 Min	–4 Max	–5 Min	–5 Max	–6 Min	–6 Max	–8 Min	–8 Max	Units
t_{DS}	PLCK to Valid DAC Output [1]	5	30	5	30	5	30	5	30	5	30	ns
Δt_{DS}	Differential Output Delay [2]		2		2		2		2		2	ns
t_{ENA}	Output Turn-On Delay	5		5		5		5		5		ns
t_{DIS}	Output Turn-Off Delay [3]		20		20		20		20		20	ns
t_{DO}	RD Enable Access Time		40		40		40		40		40	ns
t_{HO}	Output Hold Time	5		5		5		5		5		ns
FT_C	Clock Feedthrough [4]		–30		–30		–30		–30		–30	dB

Notes:
1. A valid analog output is defined as the 50% point between successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.
2. This applies to different analog outputs on the same device. This is a design parameter, not 100% tested.
3. Measured at ±200mV from initial steady state output voltage.
4. Reference to full-scale output.

AC Test Conditions



Input Pulse Levels	GND to 3V
Input Rise and Fall Times (10% to 90%)	2.5ns
Digital Input Timing Reference Level	1.5V
Digital Output Timing Reference Level	0.8V and 2.4V

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Application Hints

Power Supply

The video DAC may draw large transient currents from the power supply. To ensure proper operation, use standard high frequency board layout techniques and power supply distribution.

The transient current required by the device dictates that the ground path impedance must be minimized by using decoupling capacitors, as shown in *Figure 14*. These capacitors' leads must be as short as possible. High-frequency decoupling is accomplished with a 0.1μF chip capacitor, C1. A bead tantalum, between 10μF to 47μF, should be used for C2.

A ground plane will minimize differential ground noise by holding the pin 14 voltage near 0 during the current transitions.

Analog Output-Line Driving

The output connections should be viewed as transmission lines. Impedance changes along these lines will reflect part of the video signal back to the DACs' outputs. To ensure good signal fidelity, RF design techniques should be observed. Any traces connecting the DAC to an onboard connector should form a transmission line of 75Ω impedance, unless the DAC's output termination resistor is placed at the output connector instead of the DAC's output pin. The coaxial cable that connects the outputs to a video monitor should have a characteristic impedance of 75Ω. Since connectors on the coaxial line can cause impedance changes, any connectors used must match the line's characteristic impedance.

The DACs use switched current sources that are summed together to generate the output current. Each 6-bit DAC consists of 63 current sources, each of

Analog Output-Line Driving (cont.)

which has a magnitude of 1/30 (I_{REF}). The digital input code determines the number of current sources that contribute to the total output current. This output current, in conjunction with a termination resistance connected between each DAC output and ground, sets the full-scale magnitude of the output voltage. There are four different methods of terminating the DAC outputs:

1. Single-Termination at the DAC (75Ω)
2. Single-Termination at the Destination (75Ω)
3. Double-Termination (37.5Ω)
4. Buffered Signal

1. Single-termination at the source places a single termination resistor at each DAC output. No other terminating load is present. Therefore, a high-input impedance monitor should be used. The AC load driven by each DAC's outputs is the transmission line impedance in parallel with the load resistor. The transmission line's impedance should match that of the load resistor. Thus, the DACs' output has an initial signal amplitude that is half the DC value expected. This half-amplitude signal is 100% reflected by the open circuit presented by the monitor input, restoring the signal amplitude to the expected value. The reflections from the monitor propogate back to the DAC output, where the load resistor presents a correctly terminated transmission line so that no further reflections occur. This arrangement is relatively tolerant of mismatches in the transmission line between the DAC and the monitor because no reflections occur at the DAC end of the transmission line. However, multiple monitors should not be connected in parallel, despite each monitor's high-input impedance.

2. Single-termination at the destination uses the termination impedance at the input of the monitor as both the load resistor for the DAC and the termination impedance of the cable (transmission line). If the connections are correctly terminated there will be no reflections. However, if there are any line impedance variations along the cable, reflections will occur and create "ghost images" on the display. This occurs because there is a reflection from the point where the mismatch occurs back to the DAC's output. The signal then reflects off the DAC's output back toward the monitor, causing an echo, or "ghosting".

3. Double-termination of the DAC outputs allows each end of the transmission line to be correctly matched. This results in the least amount of reflection and the highest signal and display fidelity. This termination method permits the fastest rise time. The DAC termination's RC time constant sets the outputs' rise time. The greater the time constant, the slower the rise time. Therefore, the rise time will be minimized since the impedance using this termination technique is less than that achieved with single-termination. With double-termination, it is necessary to increase I_{REF} to 8.8mA to ensure a full-scale output voltage of 700mV.

4. With a buffer at its outputs the DACs will be able to drive capacitive loads such as long lossy cables. A high-input impedance buffer, e.g., LM1201 or LM1203, is required. A 75Ω load is placed at the buffer's input.

   The buffer's low output impedance should be matched to the interconnecting cable with a series resistor. The cable should then be terminated with the same resistance at the monitor.

ESD Protection

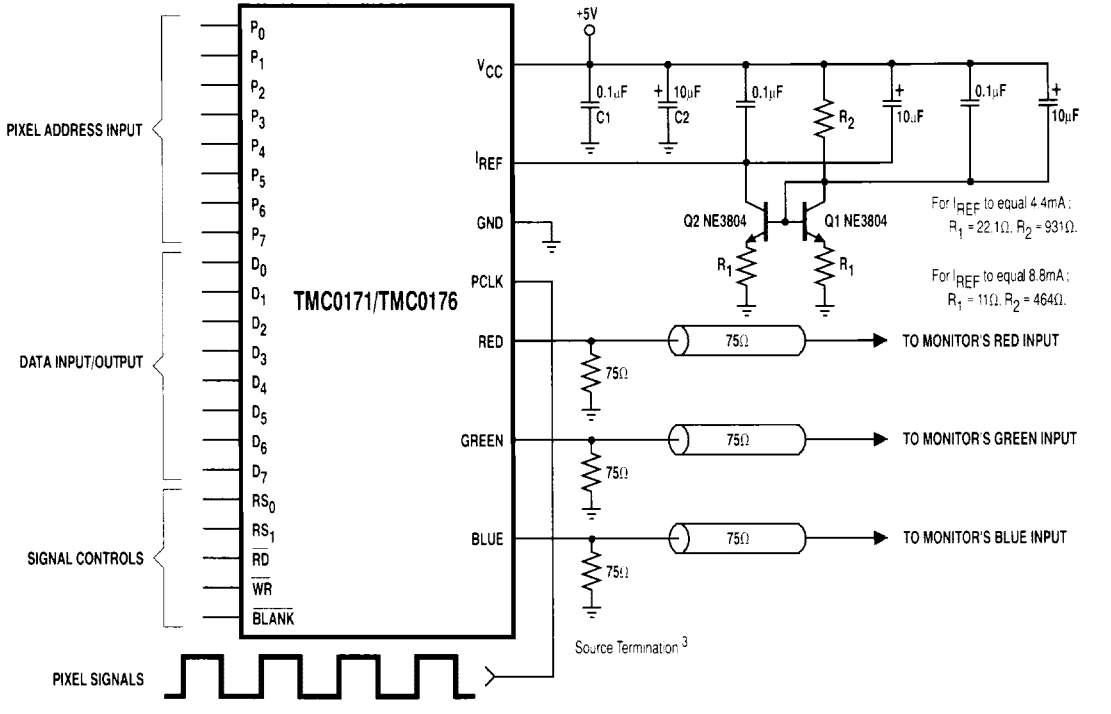
Although each pin has on-chip electrostatic discharge damage (ESD) protection, proper handling precautions during manufacturing will reduce the possibility of ESD.

Generating I_{REF}

An active I_{REF} current source will ensure that the video DAC has predictable and stable output currents. There are numerous methods available to generate the reference current. One of the simplest circuits is shown in ***Figure 14***. As shown, this I_{REF} generator will sink −4.44mA (single-termination) with R1 = 22.1Ω and R2 = 931Ω.

For double-termination applications, R1 = 11Ω and R2 = 464Ω. The diode connected transistor, Q1, across Q2's base-emitter junction compensates for thermal variations to first order.

Figure 14. Typical Connection Showing I_{REF} Generator



NOTE: 1. Bead - style tantalum capacitors should be used for the 10µF devices.
2. Thermally connect the NPN transistors together.
3. For single termination, set I_{REF} to 4.44mA and use either source or destination termination resistors. For double termination, set I_{REF} to 8.88MA and use both source and destination resistors.

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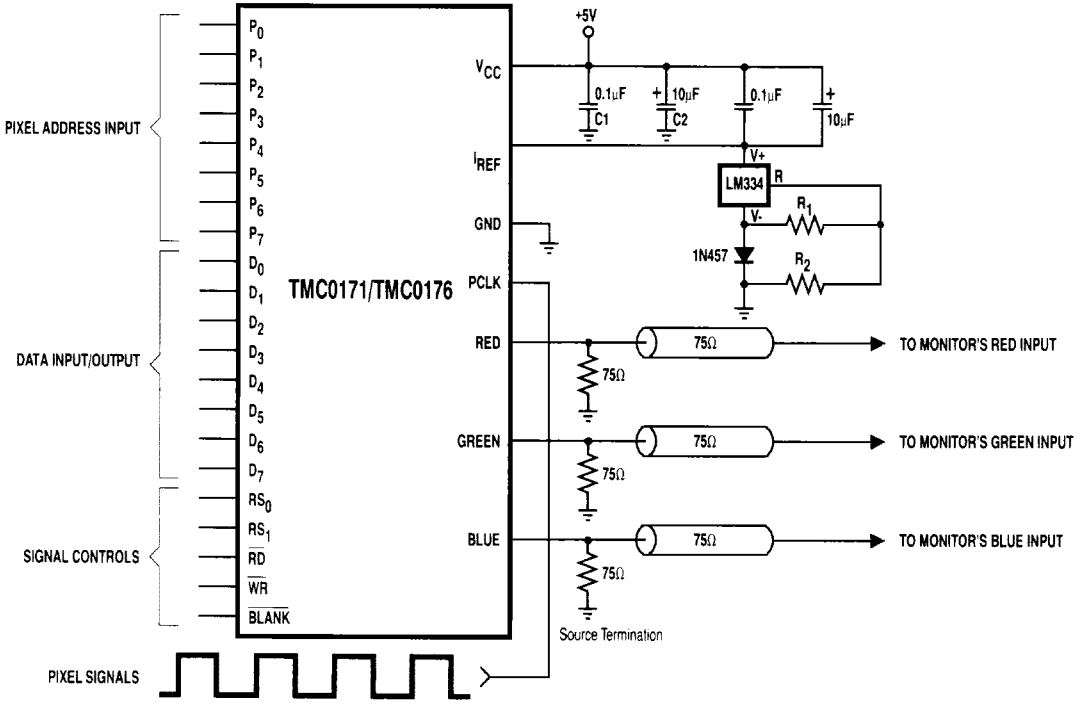
Figure 15 shows an alternative method of generating I_{REF}. The LM334 precision current source is used in a temperature compensated configuration. The reference current is set by a single resistor, R1, independent of V_{CC}. The current's value is:

$$I_{REF} = 130mV/R1$$

This current is not recommended for critical applications, particularly with double-termination.

Figure 15. Typical Connection with LM334 Current Source I_{REF} Generator



NOTE: 1. Bead - style tantalum capacitors should be used for the 10µF devices.
2. R_1 = 30Ω for I_{REF} 4.44mA;
R_2 = 10 times R_1
15Ω for I_{REF} = 8.88mA

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Figure 16 shows a TDC4611 and a discrete transistor generating a very stable I_{REF}.

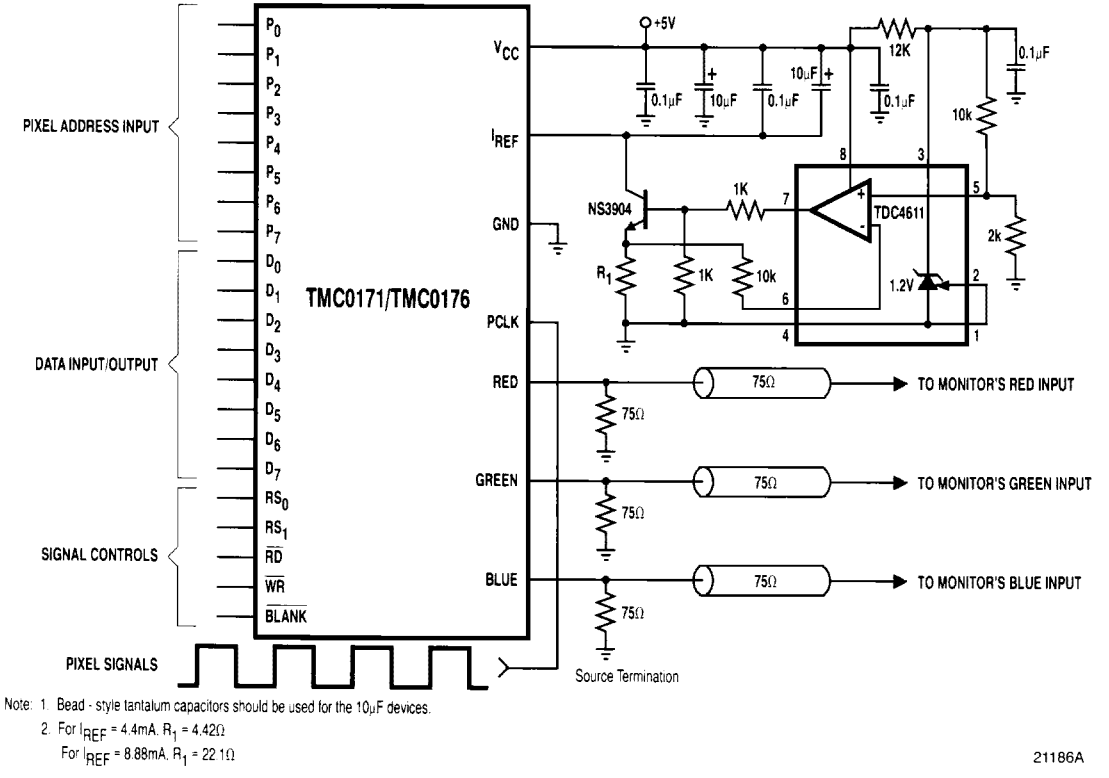
The TDC4611's on-board reference produces a nominal 1.24V. The voltage divider connected to the reference's output, pin 3, creates 200mV that is applied to R1.

Ignoring the small amount of base current, the discrete transistor's collector current (and therefore, I_{REF}) is:

$$I_{REF} = 200mV/R1$$

For $I_{REF} = 4.44mA$, R1 is, to the nearest 1% value 44.2Ω; $I_{REF} = 8.88mA$ gives an R1 of 22.1Ω.

Figure 16. Typical Connection with I_{REF} Generator Using TDC4611



Decoupling I_{REF}

The DACs comprise switched current sources. Each current source is based on a current mirror that produces (I_{REF})/30 when active. The total output current is determined by the number of active current sources switched to the output and the magnitude of I_{REF}.

The magnitude of the current flowing through the internal current sources depends not only on I_{REF}, but also on the voltage at pin 4 relative to V_{CC}. Therefore, voltage variations between V_{CC} and the I_{REF} input can result in variations in the DAC's output current. These variations can be greatly attenuated by using a high-frequency capacitor to couple the I_{REF} input to V_{CC}. This allows the reference current input to track both high and low frequency variations in V_{CC}.

Ordering Information

Product Number	Speed (MHz)	Temperature Range	Screening	Package	Package Marking
TMC0171N6C	35	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0171N6C
TMC0171N6C4	40	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0171N6C4
TMC0171R2C	35	STD – T_A = 0°C to 70°C	Commercial	44 Lead Plastic J-Leaded Chip Carrier	0171R2C
TMC0176N6C4	40	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0176N6C4
TMC0176N6C5	50	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0176N6C5
TMC0176N6C6	66	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0176N6C6
TMC0176N6C8	80	STD – T_A = 0°C to 70°C	Commercial	28 Pin Plastic DIP	0176N6C8
TMC0176R2C4	40	STD – T_A = 0°C to 70°C	Commercial	44 Lead Plastic J-Leaded Chip Carrier	0176R2C4

B