PDSP16318/PDSP16318A

COMPLEX ACCUMULATOR

The PDSP16318 contains two independent 20-bit Adder/ Subtractors combined with accumulator registers and shift structures. The four port architecture permits full 20MHz throughout in FFT and filter applications.

Two PDSP16318As combined with a single PDSP16112A Complex Multiplier provide a complete arithmetic solution for a Radix 2 DIT FFT Butterfly. A new complex Butterfly result can be generated every 50ns allowing 1K complex FFTs to be executed in 256μs.

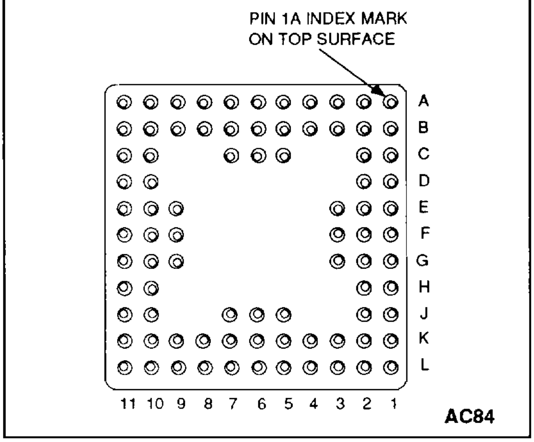


Fig. 1 Pin connections - bottom view (AC84 - PGA)

FEATURES

- Full 20MHz Throughout in FFT Applications
- Four Independent 16-bit I/O Ports
- 20-bit Addition or Accumulation
- Fully Compatible with PDSP16112 Complex Multiplier
- On Chip Shift Structures for Result Scaling
- Overflow Detection
- Independent Three-State Outputs and Clock Enables for 2 Port 20MHz Operation
- 1.4 micron CMOS
- 500mW Maximum Power Dissipation
- 84 Pin PGA or QFP packages

APPLICATIONS

- High speed Complex FFT or DFTs
- Complex Finite Impulse Response (FIR) Filtering
- Complex Conjugation
- Complex Correlation/Convolution

ASSOCIATED PRODUCTS

PDSP16112 16 x 12 Complex Multiplier
PDSP16116 16 x 16 Complex Multiplier
PDSP1601 ALU and Barrel Shifter
PDSP16330 Pythagoras Processor

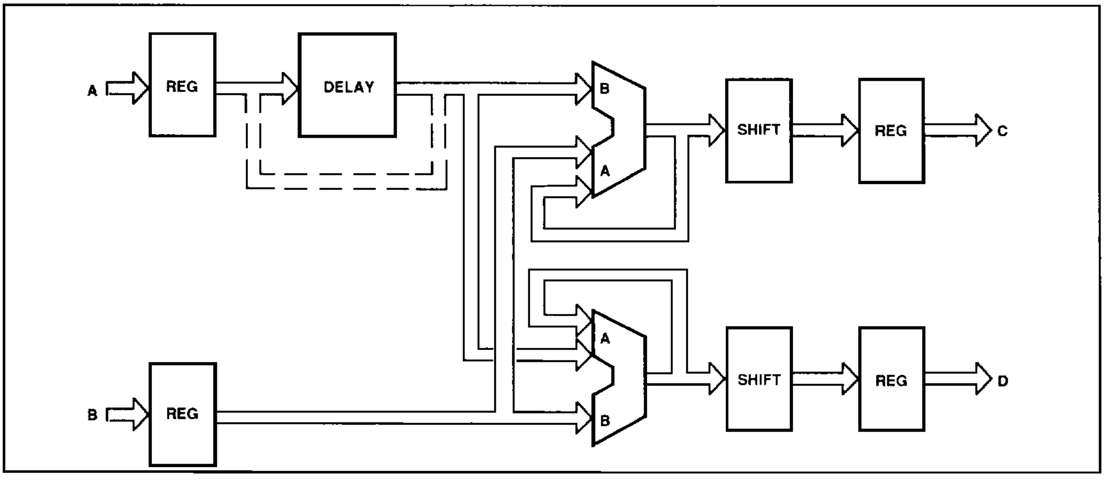


Fig. 2 PDSP16318 simplified block diagram

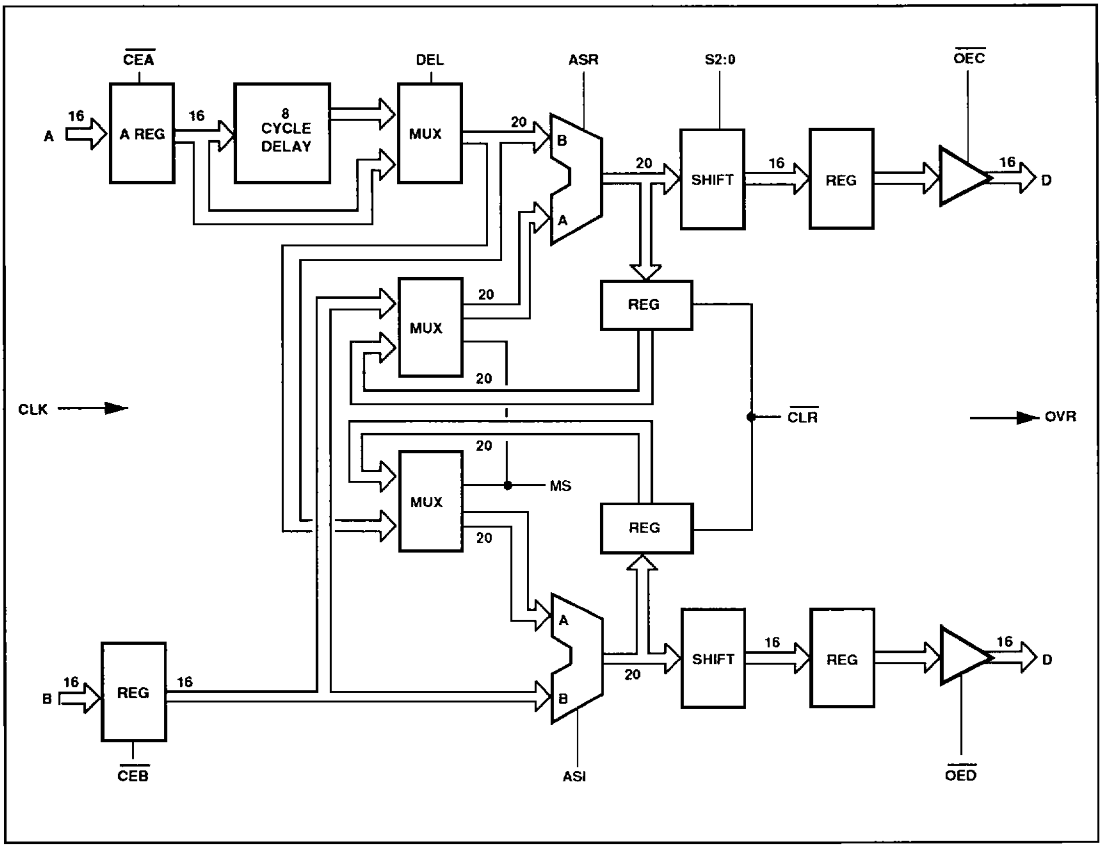


Fig. 3 Block diagram

FUNCTIONAL DESCRIPTION

The PDSP16318 is a Dual 20-bit Adder/Subtractor configured to support Complex Arithmetic. The device may be used with each of the adders allocated to real or imaginary data (e.g. Complex Conjugation), the entire device allocated to Real or Imaginary Data (e.g. Radix 2 Butterflys) or each of the adders configured as accumulators and allocated to real or imaginary data (Complex Filters). Each of these modes ensures that a full 20MHz throughput is maintained through both adders, the first and last mode illustrating true Complex operation, where both real and imaginary data is handled by the single device.

Both Adder/Subtractors may be controlled independently via the ASR and ASI inputs. These controls permit A + B, A - B, B - A or pass A operations, where the A input to the Adder is derived from the input multiplexer. The CLR control line allows the clearing of both accumulator registers. The two multiplexers may be controlled via the MS inputs, to select either new input data, or fed-back data from the accumulator registers. The PDSP16318 contains an 8-cycle deskew register selected via the DEL control. This deskew register is used in FFT applications to ensure correct phasing of data that has not passed through the PDSP16112 Complex Multiplier.

The 16-bit outputs from the PDSP16318 are derived from the 20-bit result generated by the Adders. The three bit S2:0 input selects eight different shifted output formats ranging from the most significant 16 bits of the 20-bit data, to the least significant 13 bits of the 20-bit data. In this mode the 14th, 15th and 16th bits of the output are set to zero. The shift selected is applied to both adder outputs, and determines the function of the OVR flag. The OVR flag becomes active when either of the two adders produces a result that has more significant digits than the MSB of the 16-bit output from the device. In this manner all cases when invalid data appears on the output are flagged.

Symbol	Type	Description
A15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. A15 is the MSB.
B15:0	Input	**Data** presented to this input is loaded into the input register on the rising edge of CLK. B15 is the MSB and has the same weighting as A15.
C15:0	Output	New **data** appears on this output after the rising edge of CLK. C15 is the MSB.
D15:0	Output	New **data** appears on this output after the rising edge of CLK. C15 is the MSB.
CLK	Input	**Common Clock** to all internal registers
$\overline{CEA}$	Input	**Clock enable:** when low the clock to the A input register is enabled.
$\overline{CEB}$	Input	**Clock enable:** when low the clock to the B input register is enabled.
$\overline{OEC}$	Input	**Output enable:** Asynchronous 3-state output control: The C outputs are in a high impedance state when this input is high.
$\overline{OED}$	Input	**Output enable:** Asynchronous 3-state output control: The D outputs are in a high impedance state when this input is high.
OVR	Output	**Overflow flag:** This flag will go high in any cycle during which either the output data overflows the number range selected or either of the adder results overflow. A new OVR appears after the rising edge of the CLK.
ASR1:0	Input	**Add/subtract Real:** Control input for the 'Real' adder. This input is latched by the rising edge of clock.
ASI1:0	Input	**Add/subtract Imag:** Control input for the 'Imag' adder. This input is latched by the rising edge of clock.
$\overline{CLR}$	Input	**Accumulator Clear:** Common accumulator clear for both Adder/Subtractor units. This input is latched by the rising edge of CLK.
MS	Input	**Mux select:** Control input for both adder multiplexers. This input is latched by the rising edge of CLK. When high the feedback path is selected.
S2:0	Input	**Scaling control:** This input selects the 16-bit field from the 20-bit adder result that is routed to the outputs. This input is latched by the rising edge of CLK.
DEL	Input	**Delay Control:** This input selects the delayed input to the real adder for operations involving the PDSP16112. This input is latched by the rising edge of CLK.
VCC	Power	**+5V supply:** Both Vcc pins must be connected.
GND	Ground	**0V supply:** Both GND pins must be connected.

GG pin	AC pin	Function	GG pin	AC pin	Function	GG pin	AC pin	Function	GG pin	AC pin	Function
77	B2	D7	6	K2	C7	31	K10	A1	56	B10	B10
82	C2	D8	7	K3	C6	32	J10	A2	57	B9	B9
83	B1	D9	8	L2	C5	33	K11	A3	58	A10	B8
84	C1	D10	9	L3	C4	34	J11	A4	59	A9	B7
85	D2	GND	10	K4	C3	35	H10	A5	60	B8	B6
86	D1	VCC	11	L4	C2	36	H11	A6	61	A8	B5
87	E3	D11	12	J5	C1	37	F10	A7	62	B6	B4
88	E2	D12	13	K5	C0	38	G10	A8	63	B7	B3
89	E1	D13	14	L5	$\overline{OED}$	39	G11	A9	64	A7	B2
90	F2	D14	15	K6	$\overline{OEC}$	40	G9	A10	65	C7	B1
91	F3	D15	16	J6	S2	41	F9	A11	66	C6	B0
92	G3	C15	17	J7	S1	42	F11	A12	67	A6	CLK
93	G1	C14	18	L7	S0	43	E11	A13	68	A5	$\overline{CEB}$
94	G2	C13	19	K7	MS	44	E10	A14	69	B5	OVR
95	F1	C12	20	L6	ASI1	45	E9	A15	70	C5	D0
96	H1	VCC	21	L8	ASI0	46	D11	$\overline{CEA}$	71	A4	D1
97	H2	GND	22	K8	DEL	47	D10	B15	72	B4	D2
98	J1	C11	23	L9	$\overline{CLR}$	48	C11	B14	73	A3	D3
99	K1	C10	24	L10	ASR1	49	B11	B13	74	A2	D4
100	J2	C9	25	K9	ASR0	50	C10	B12	75	B3	D5
5	L1	C8	26	L11	A0	51	A11	B11	76	A1	D6

Device Pinout for ceramic 84 - pin PGA (AC84) and ceramic QFP (GG100)

ASR or ASI ASX1	ASX0	ALU Function
0	0	A + B
0	1	A
1	0	A - B
1	1	B - A

DEL	Delay Mux Control
0	A port input
1	Delayed A port input

MS	Real and Imag' Mux Control
0	B port input/Del mux output
1	C accumulator/D accumualtor

S2:0			Adder result																			
S2	S1	S0	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
0	0	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
0	1	0			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	1	1				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	0					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1						15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1	1	0							15	14	13	12	11	10	9	8	7	6	5	4	3	2
1	1	1								15	14	13	12	11	10	9	8	7	6	5	4	3

NOTE

This table shows the portion of the adder result passed to the D15:0 and C15:0 outputs. Where fewer than 16 adder bits are selected the output data is padded with zeros.

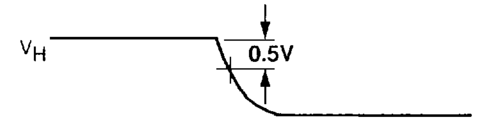
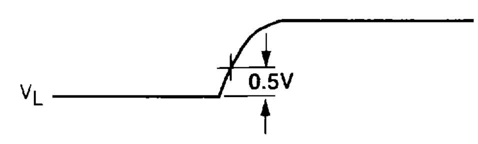
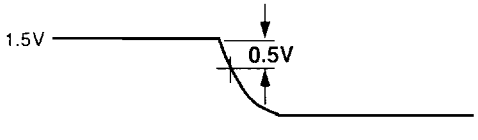
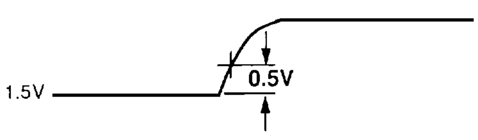
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply voltage V_{CC}	-0.5V to 7.0V
Input voltage V_{IN}	-0.9V to V_{CC} +0.9V
Output voltage V_{OUT}	-0.9V to V_{CC} +0.9V
Clamp diode current per pin I_K (see Note 2)	18mA
Static discharge voltage (HMB) V_{STAT}	500V
Storage temperature range T_S	-65°C to +150°C
Ambient temperature with power applied T_{amb}	
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Junction temperature	150°C
Package power dissipation P_{TOT}	1000mW

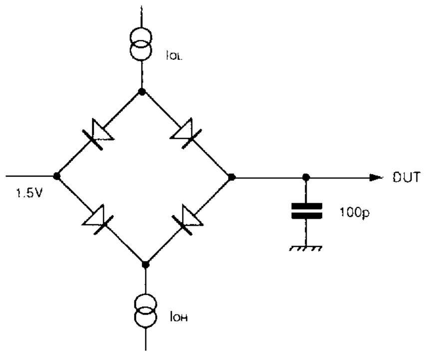
NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Exposure to absolute maximum ratings for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

Package Type	θ_{JC} °C/W	θ_{JA} °C/W
LC	12	35
AC	12	36

Test	Waveform - measurement level
Delay from output high to output high impedance	
Delay from output low to output high impedance	
Delay from output high impedance to Output low	
Delay from output high impedance to Output high	

NOTES
1. V_H - Voltage reached when output driven high
2. V_L - Voltage reached when output driven low



ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} (Commercial) = 0°C to +70°C, Vcc = 5.0V ± 5%, GND = 0V

T_{amb} (Industrial) =-40°C to +85°C, Vcc = 5.0V ± 10%, GND = 0V

T_{amb} (Military) =-55°C to +125°C, Vcc = 5.0V ± 10%, GND = 0V

STATIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4		-	V	I_{OH} = 3.2mA
Output low voltage	V_{OL}	-		0.4	V	I_{OL}=-3.2mA
Input high voltage	V_{IH}	3.5		-	V	
Input low voltage	V_{IL}	-		0.5	V	
Input leakage current	I_{IL}	-10		+10	µA	GND ≤ V_{IN}≤V_{CC}
Output leakage current	I_{OZ}	-50	-	+50	µA	GND ≤V_{OUT} ≤ V_{CC}
Output SC current	I_{OS}	20	-	200	mA	V_{cc} = Max
Input capacitance	C_{IN}	-	9	-	pF	

SWITCHING CHARACTERISTICS

Characteristic	Value Industrial + Commercial				Value Military		Units	Conditions
	PDSP16318		PDSP16318A		PDSP16318			
	Min.	Max.	Min.	Max.	Min.	Max.		
Clock period	100	-	50	-	100	-	ns	
Clock High Time	20	-	15	-	20	-	ns	
Clock Low Time	20	-	15	-	20	-	ns	
A15:0, B15:0 setup to clock rising edge	8	-	5	-	8	-	ns	
A15:0, B15:0 hold after clock rising edge	2	-	2	-	2	-	ns	
MS, S2:0, ASI setup to clock rising edge	10	-	10	-	10	-	ns	
DEL, ASR, $\overline{CLR}$ setup to clock rising edge	8	-	5	-	8	-	ns	
DEL, ASR, $\overline{CLR}$, MS, S2:0, ASI hold after clock rising edge	2	-	2	-	2	-	ns	
$\overline{CEA}$, $\overline{CEB}$ setup to clock falling edge	2	-	2	-	2	-	ns	
$\overline{CEA}$, $\overline{CEB}$ hold after clock rising edge	8	-	8	-	8	-	ns	
Clock rising edge to OVR, C15:0, D15:0	5	40	5	30	5	40	ns	2 x LSTTL + 20pF
$\overline{OEC}$/$\overline{OED}$ low to C15:0/D15:0 high data valid	-	40	-	30	-	40	ns	2 x LSTTL + 20pF
$\overline{OEC}$/$\overline{OED}$ low to C15:0/D15:0 low data valid	-	40	-	30	-	40	ns	2 x LSTTL + 20pF
$\overline{OEC}$/$\overline{OED}$ high to C15:0/D15:0 high impedance	-	40	-	30	-	40	ns	2 x LSTTL + 20pF
Vcc current	-	70	-	110	-	70	mA	Vcc = max, TTL input levels Outputs unloaded, f_{CLK} = max
Vcc current	-	30	-	60	-	30	mA	Vcc = max, CMOS input levels Outputs unloaded, f_{CLK} = max

NOTES

1. LSTTL is equivalent to I_{OH} = 20 microamps, I_{OL} = -0.4mA
2. Current is defined as negative into the device
3. CMOS input levels are defined as:
   V_{IL} = 0.5
   V_{IH} = V_{DD} - 0.5

ORDERING INFORMATION

Comercial (0°C to +70°C)

PDSP16318/C0/AC	(10MHz - PGA)
PDSP16318/C0/GG	(10MHz - QFP)
PDSP16318A/C0/AC	(20MHz - PGA)
PDSP16318A/C0/GG	(20MHz - QFP)

Industrial (-40°C to +85°C)

PDSP16318/B0/AC	(10MHz - PGA)
PDSP16318/B0/GG	(10MHz - QFP)
PDSP16318A/B0/AC	(20MHz - PGA)
PDSP16318A/B0/GG	(20MHz - QFP)

Military (-55°C to +125°C)

PDSP16318/A0/AC	(10MHz - PGA)
PDSP16318/A0/GG	(10MHz - QFP)
PDSP16318A/A0/AC	(20MHz - PGA)
PDSP16318A/A0/GG	(20MHz - QFP)

Call for availability on High Reliability parts and MIL 883C screening.