

## PRELIMINARY INFORMATION

### Introduction

The MC-174 and MC-176 are static RAM cards designed for use in applications where portability is required. They are packaged in a metal container, approximately the same size as a credit card. However, the thickness is 3.4 mm (0.133 inches), which is the thickness of about three credit cards.

The cards use standard 32,768 x 8-bit  $\mu$ PD43256A static RAM that is able to retain data by means of an internal battery when system power is unavailable. The data bus may be configured as either 8 or 16 bits. Furthermore, the upper or lower memory bytes may be connected for input or output to the upper or lower bytes of the data bus.

The MC-174 is organized as 131,072 bytes and the MC-176 as 524,288 bytes. An external switch prevents accidental changing of write data.

### Features

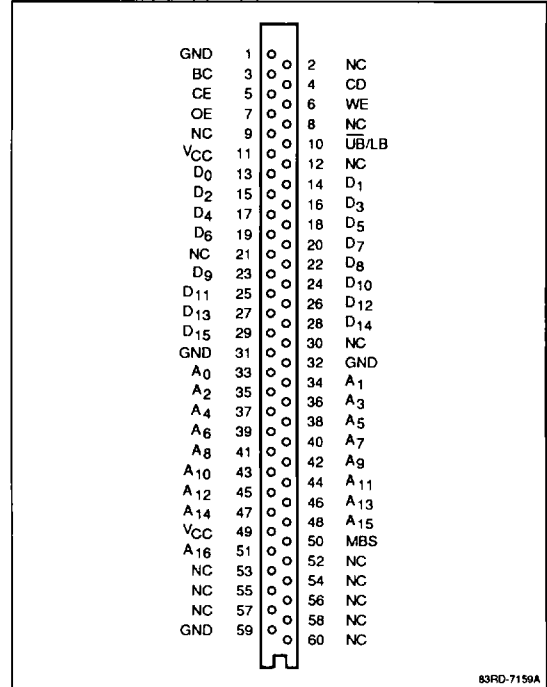
- Credit card size
- Two densities
  - MC-174 = 131,072 bytes
  - MC-176 = 524,288 bytes
- Easily accessible write protection switch
- Electronic card identification
- Selectable data-bus width of 8 or 16 bits
- Replaceable battery
- Battery test circuit
- Single + 5-volt power supply

### Ordering Information

Part Number	Read Access		Package
	Cycle (max)	Organization	
MC-174	250 ns	131,072 bytes	60-pin IC card
MC-176	250 ns	524,288 bytes	60-pin IC card

### Pin Configurations

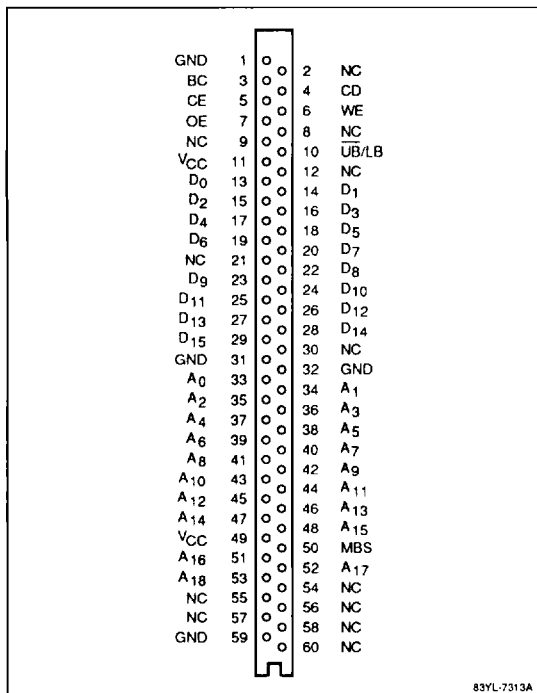
#### 60-Pin IC Card (MC-174)



83RD-7150A

Pin Configurations (cont)

60-Pin IC Card (MC-176)



83YL-7313A

Pin Identification

Symbol	Function
A <sub>0</sub> - A <sub>18</sub>	Addresses
BC	Battery check
CD	Card detect
CE	Card enable
D <sub>0</sub> - D <sub>15</sub>	Data inputs/outputs
MBS	Bus select
OE	Output enable
UB/LB	Upper byte/lower byte
WE	Write enable
GND	Ground
V <sub>CC</sub>	+ 5-volt power supply
NC	No connection

Pin Descriptions

**A<sub>0</sub> through A<sub>18</sub>.** These pins serve as addresses for standard read and write cycles.

**BC (Battery Check).** This pin measures the voltage of the card's internal backup battery.

**CD (Card Detect).** This pin controls reading of the electronic signature.

**CE (Card Enable).** This pin is used to select the card for read or write operation. CE high activates the device and CE low puts it in standby.

**D<sub>0</sub> through D<sub>15</sub>.** These pins serve as the data bus interface between the MC-174/176 and the system.

**MBS (Memory Bus Select).** During a write cycle, the signal from this pin selects a byte of the data bus to be written.

**OE (Output Enable).** The signal from this pin controls the output drivers for D<sub>0</sub> through D<sub>15</sub>.

**UB/LB (Upper Byte/Lower Byte).** The signal from this pin selects the upper or lower byte of the memory card for connection to the upper or lower byte of the data bus.

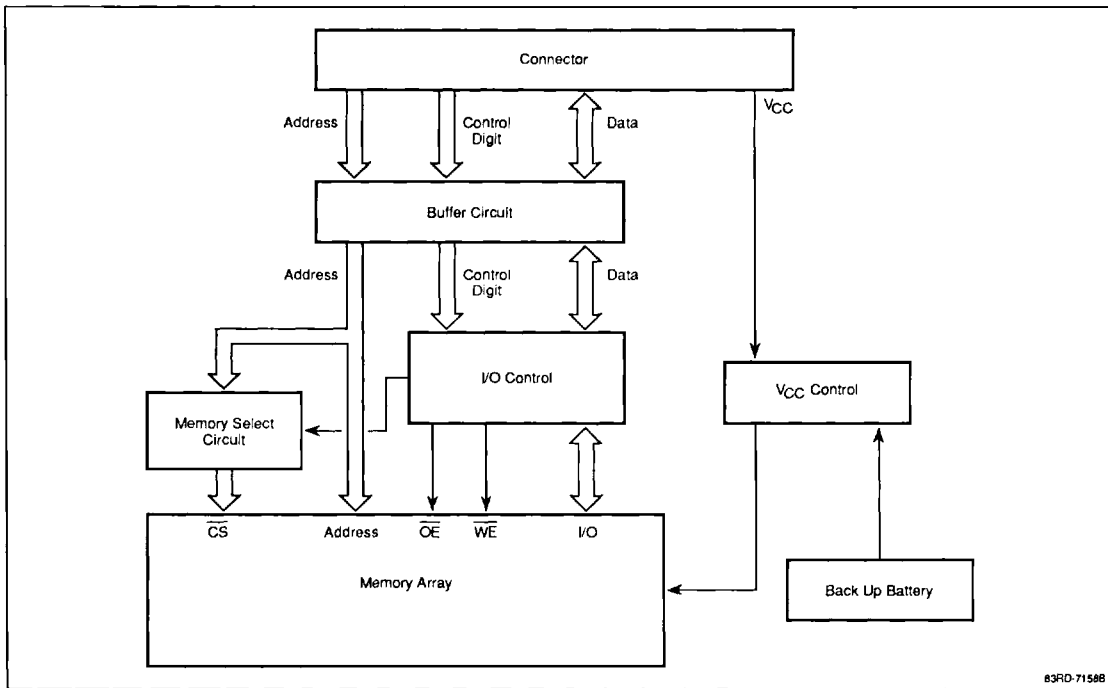
**WE (Write Enable).** This pin controls read and write operation.

Addressing

Addresses on the MC-174/176 designate bytes to be selected. Since the cards are able to be organized as 8 or 16 bits, the lower memory byte is selected when A<sub>0</sub> is low and the upper memory byte is selected when A<sub>0</sub> is high. A<sub>0</sub> is the least significant bit in byte organization. In word organization, A<sub>0</sub> remains low and A<sub>1</sub> becomes the least significant bit.

The MC-174/176 are internally organized as two 8-bit bytes, a lower byte encompassing locations MD<sub>0</sub> through MD<sub>7</sub> and an upper byte encompassing MD<sub>8</sub> through MD<sub>15</sub>. The lower and upper memory bytes may be logically connected to the lower or upper data bus, D<sub>0</sub> through D<sub>7</sub> and D<sub>8</sub> through D<sub>15</sub>, respectively, as specified by a combination of signals from A<sub>0</sub> and UB/LB.

### Block Diagram



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A low on  $\overline{UB/LB}$  while  $A_0$  is toggling connects first the lower and then the upper memory byte to the lower byte of the data bus ( $D_0$  through  $D_7$ ).  $A_0$  first goes low and then high, respectively. The upper byte of the data bus is connected to the upper memory byte while  $\overline{UB/LB}$  is low, regardless of whether  $A_0$  is high or low. A high on  $\overline{UB/LB}$  while  $A_0$  is toggling alternately connects the lower memory byte to both bytes of the data bus when  $A_0$  is low. The upper memory byte is connected to both bytes of the data bus when  $A_0$  is high. See table 1.

If 16-bit data is required, i.e., with the upper memory byte connected to the upper data bus and the lower memory byte to the lower data bus, then  $A_0$  must remain low and  $A_1$  becomes the least significant bit.

**Table 1. Read Data Bus Control**

$\overline{UB/LB}$	$A_0$	$D_8$ through $D_{15}$	$D_0$ through $D_7$
$V_{IL}$	$V_{IL}$	Upper byte	Lower byte
X	$V_{IH}$	Upper byte	Upper byte
$V_{IH}$	$V_{IL}$	Lower byte	Lower byte

**Notes:**

- (1) Lower byte =  $MD_0$  through  $MD_7$ .
- (2) Upper byte =  $MD_8$  through  $MD_{15}$ .

### Read Operation

Read operation is initiated by applying high logic levels to CE and OE and low levels to CD and WE.

**Write Operation**

When WE is high and OE low, either a word or byte write cycle may be executed (table 2). In a word write cycle,  $\overline{UB/LB}$  and  $A_0$  must be low to enable the upper and lower data buses to be written to the upper and lower memory bytes, respectively. The signals of MBS,  $\overline{UB/LB}$  and  $A_0$  are used to select a byte write cycle, during which either the upper (MBS high) or lower data bus (MBS low) is active.  $\overline{UB/LB}$  and  $A_0$  specify whether the active data bus is connected to the upper or lower memory byte.

**Table 2. Write Data Bus Control**

MBS	$\overline{UB/LB}$	$A_0$	$D_8$ through $D_{15}$	$D_0$ through $D_7$
X	$V_{IL}$	$V_{IL}$	Upper byte	Lower byte
$V_{IL}$	X	$V_{IH}$	Not used	Upper byte
$V_{IL}$	$V_{IH}$	$V_{IL}$	Not used	Lower byte
$V_{IH}$	X	$V_{IH}$	Upper byte	Not used
$V_{IH}$	$V_{IH}$	$V_{IL}$	Lower byte	Not used

**Notes:**

- (1) Lower byte =  $MD_0$  through  $MD_7$ .
- (2) Upper byte =  $MD_8$  through  $MD_{15}$ .

**Signature Read Operation**

The existence and type of memory card installed may be detected by the system using a signature read cycle. The card signature is accessed by applying a high logic level to CD and OE and a low to CE and WE. The signature word will then be accessible on  $D_0$  through  $D_{15}$  of the data bus. Table 3 decodes the contents of the signature word.

**Checking the Battery**

When the internal battery is being used to back up the memory, the connector pins should be open.

The BC pin is used for testing the voltage of the internal backup battery (figure 1 shows a diagram of the circuit). The battery (type CR2025) may be discharged through this pin, and it is therefore advisable for external circuits connected to BC to have an impedance of 1 M $\Omega$  or greater. This impedance level will minimize discharge during voltage testing and maximize the life of the battery.

New batteries have a voltage of 3 volts. As the battery is discharged and voltage drops to 2.5 volts, the battery should be replaced within 10 hours. To retain data during battery replacement, ensure that  $V_{CC}$  is connected to a +5-volt source.

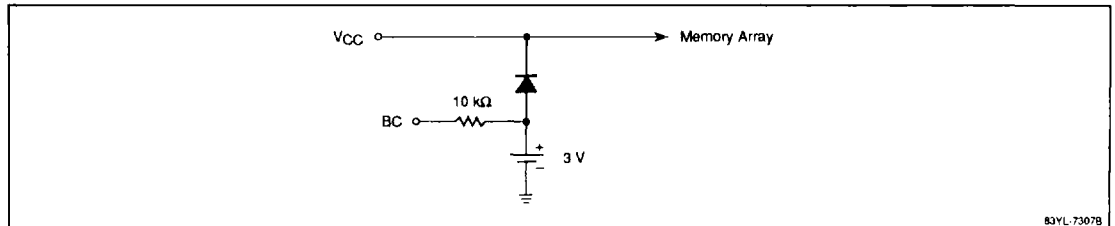
**Connectors**

The JC20-E605-F1-A4 memory card connector and one of two 60-pin mating connectors (either JC20-E60PA-LT1-A4 or JC20-E60PA-LT2-A4, depending on the thickness of gold plating required) are available directly from either of the following:

JAE Electronics (Headquarters)  
 3-1-9, Wakabadai  
 Meguro-ku  
 Tokyo, Japan 153  
 Telephone: 011-81-3-780-2889  
 FAX: 011-81-3-780-2884

JAE Electronics (USA Sales Office)  
 142 Technology Drive, Suite 100  
 Irvine, CA 92718  
 Telephone: (714) 753-2600  
 FAX: (714) 753-2699

**Figure 1. Battery Test Circuit**



**Table 3. Signature Read Operation**

Device	D <sub>15</sub>	D <sub>14</sub>	D <sub>13</sub>	D <sub>12</sub>	D <sub>11</sub>	D <sub>10</sub>	D <sub>9</sub>	D <sub>8</sub>	D <sub>7</sub>	D <sub>6</sub>	D <sub>5</sub>	D <sub>4</sub>	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
MC-174	V <sub>IH</sub>	V <sub>IL</sub>	WP	X	X	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>
MC-176	V <sub>IH</sub>	V <sub>IL</sub>	WP	X	X	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>

**Notes:**

- (1) WP = the status of the write protect switch, where V<sub>IH</sub> indicates write protection has been enabled and V<sub>IL</sub> means it is disabled.
- (2) X can be either V<sub>IL</sub> or V<sub>IH</sub>.

**Absolute Maximum Ratings**

Supply voltage, V <sub>CC</sub>	-0.5 to +7.0 V
Input voltage, V <sub>IN</sub> (Note 1)	-0.5 to V <sub>CC</sub> + 0.5
Output voltage, V <sub>OUT</sub>	-0.5 to V <sub>CC</sub> + 0.5
Storage temperature, t <sub>STG</sub>	-20 to +60°C
Operating temperature, t <sub>OPR</sub>	0 to +50°C
Battery backup operating temperature, t <sub>BU</sub>	0 to +50°C

**Notes:**

- (1) -3.0 V minimum for 50 ns maximum pulse width.

**Capacitance**

T<sub>A</sub> = 25°C; f = 1 MHz; V<sub>CC</sub> = 0 V; V<sub>IN</sub> and V<sub>IO</sub> = 0 V

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C <sub>IN</sub>	10	pF	Addresses, CD, CE, MBS, OE, $\overline{UB/LB}$ , WE
Input/output capacitance	C <sub>IO</sub>	35	pF	D <sub>0</sub> through D <sub>15</sub>

**Notes:**

- (1) X can be either V<sub>IL</sub> or V<sub>IH</sub>.

**Data Bus Control**

$\overline{UB/LB}$	A <sub>0</sub>	MBS	WE	OE	D <sub>15</sub> through D <sub>8</sub>	D <sub>7</sub> through D <sub>0</sub>
V <sub>IL</sub>	V <sub>IL</sub>	X	V <sub>IL</sub>	V <sub>IH</sub>	Upper byte	Lower byte
X	V <sub>IH</sub>	X	V <sub>IL</sub>	V <sub>IH</sub>	Upper byte	Upper byte
V <sub>IH</sub>	V <sub>IL</sub>	X	V <sub>IL</sub>	V <sub>IH</sub>	Lower byte	Lower byte
V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Upper byte	Lower byte
X	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Not used	Upper byte
V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Not used	Lower byte
V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Upper byte	Lower byte
X	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Upper byte	Not used
V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	Lower byte	Not used

**Notes:**

- (1) X can be either V<sub>IL</sub> or V<sub>IH</sub>.
- (2) Lower = MD<sub>0</sub> through MD<sub>7</sub>.
- (3) Upper = MD<sub>8</sub> through MD<sub>15</sub>.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	4.75	5.0	5.25	V
Input voltage, low	V <sub>IL</sub>	0		0.7	V
Input voltage, high	V <sub>IH</sub>	2.3		V <sub>CC</sub>	V
Ambient temperature	T <sub>A</sub>	0		50	°C

**Truth Table**

Function	D <sub>0</sub> - D <sub>15</sub>	CE	CD	WE	OE
Standby	High-Z	V <sub>IL</sub>	V <sub>IL</sub>	X	X
Read cycle	Data out	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>
	High-Z	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>
Write cycle	Data-in	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>
Signature read	Data out	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>
	High-Z	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>
Invalid	High-Z	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>
Prohibited	High-Z	V <sub>IH</sub>	V <sub>IH</sub>	X	X

**Notes:**

- (1) X can be either V<sub>IH</sub> or V<sub>IL</sub>.

### DC Characteristics

$T_A = 0$  to  $50^\circ\text{C}$ ;  $V_{CC} = +5.0\text{ V} \pm 5\%$

Parameter	Symbol	Min	Max	Unit	Test Conditions
I/O leakage current, high	$I_{OH}$		260	$\mu\text{A}$	(Notes 1, 2)
I/O leakage current, low	$I_{OL}$	-10		$\mu\text{A}$	(Notes 1, 2)
Operating supply current	$I_{CCA}$		140	mA	
Standby supply current	$I_{SB}$		2	mA	(Note 3)
Output voltage, high	$V_{OH1}$	$V_{CC} - 0.6$		V	$I_{OH} = -0.1\text{ mA}$
	$V_{OH2}$	$V_{CC} - 1.0$		V	$I_{OH} = -4.0\text{ mA}$
Output voltage, low	$V_{OL}$		0.4	V	$I_{OL} = 4.0\text{ mA}$

#### Notes:

- (1) This parameter is periodically sampled and not 100% tested.
- (2)  $V_{IN} = V_{CC}$  or GND.
- (3)  $CE \leq 2.0\text{ V}$  and  $CD \leq 0.2\text{ V}$ . All other pins  $\leq 0.2\text{ V}$  or  $\geq V_{CC} - 0.2\text{ V}$  or high impedance.

### AC Characteristics

$T_A = 0$  to  $50^\circ\text{C}$ ;  $V_{CC} = +5.0\text{ V} \pm 5\%$

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Read Operation</b>						
Address access time	$t_{AA}$			250	ns	
CE access time	$t_{ACE}$			250	ns	
CE to output in high-Z	$t_{HZ}$			100	ns	
CE to output in low-Z	$t_{LZ}$	5			ns	
Output enable to output valid	$t_{OE}$			120	ns	
Output hold from address change	$t_{OH}$	10			ns	
OE to output in high-Z	$t_{OHZ}$			80	ns	
OE to output in low-Z	$t_{OLZ}$	5			ns	
Read cycle time	$t_{RC}$	250			ns	
<b>Write Operation</b>						
Address setup time	$t_{AS}$	20			ns	
Address valid to end of write	$t_{AW}$	200			ns	
CE to end of write	$t_{CW}$	200			ns	
Data hold time	$t_{DH}$	10			ns	
Data valid to end of write	$t_{DW}$	100			ns	
Write cycle time	$t_{WC}$	250			ns	
Write pulse width	$t_{WP}$	150			ns	
Write recovery time	$t_{WR}$	10			ns	

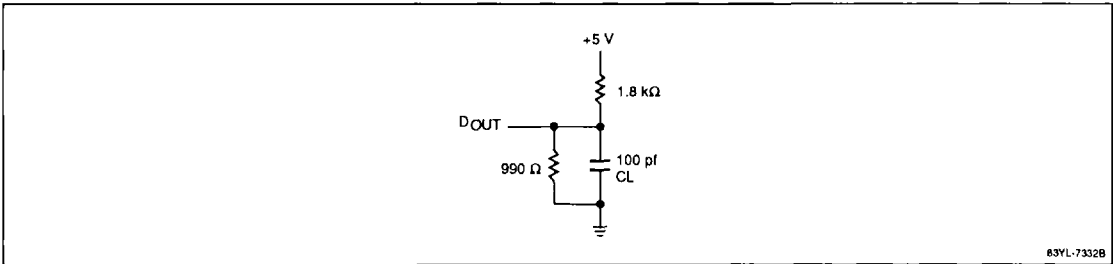
## AC Characteristics (cont)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
<b>Signature Read Operation</b>						
Address access time	$t_{AD1}$			200	ns	
Card signature access time	$t_{CD1}$			100	ns	
Card signature to output in high-Z	$t_{CD2}$			90	ns	
OE access time	$t_{OD1}$			150	ns	
OE to output in high-Z	$t_{OD2}$			60	ns	
Cycle time	$t_{OP}$	180			ns	

**Notes:**

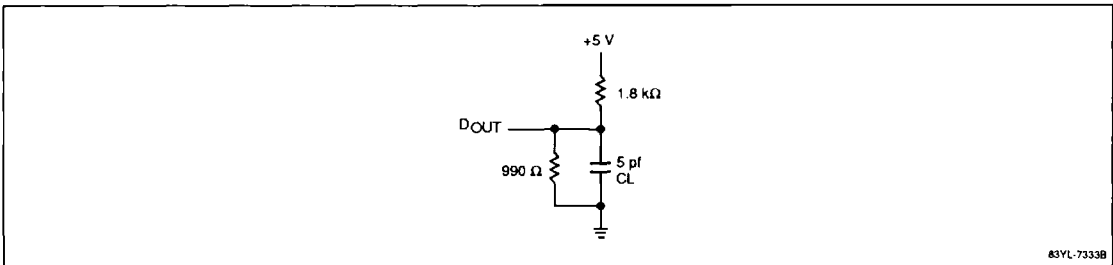
- (1) Input pulse levels = 0.7 to 2.5 V; Input pulse rise and fall times = 5 ns; timing reference levels = 1.5 V. See figures 1 and 2 for output load.

**Figure 2. Output Load**



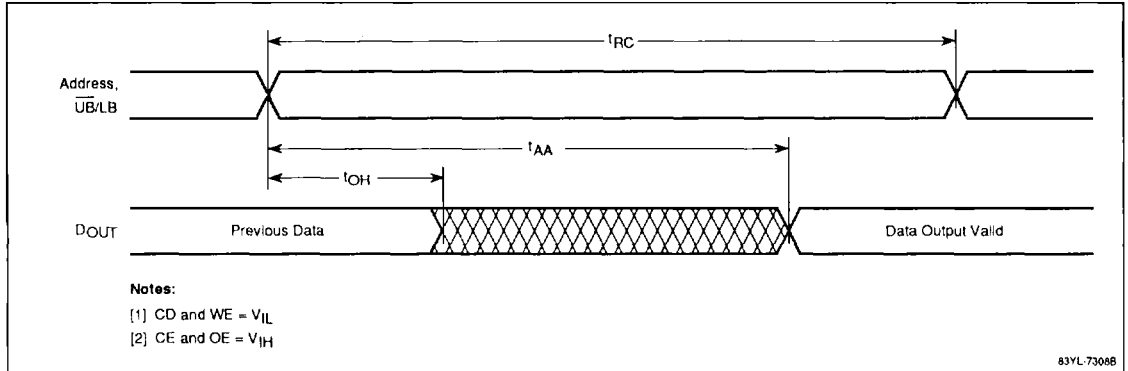
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**Figure 3. Output Load for  $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{OLZ}$**

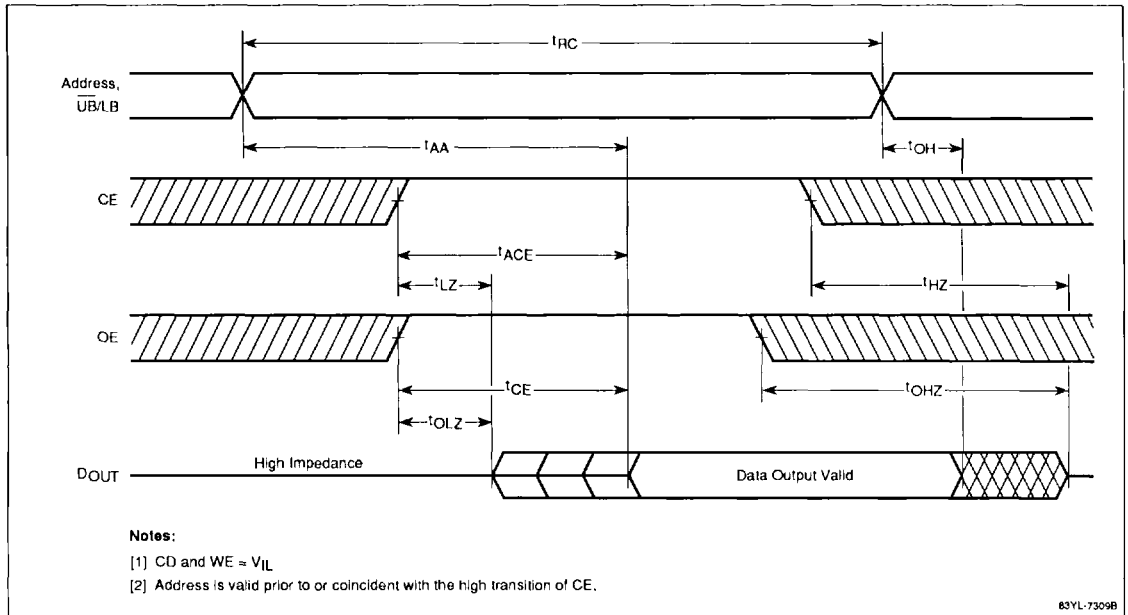


Timing Waveforms

Read Cycle

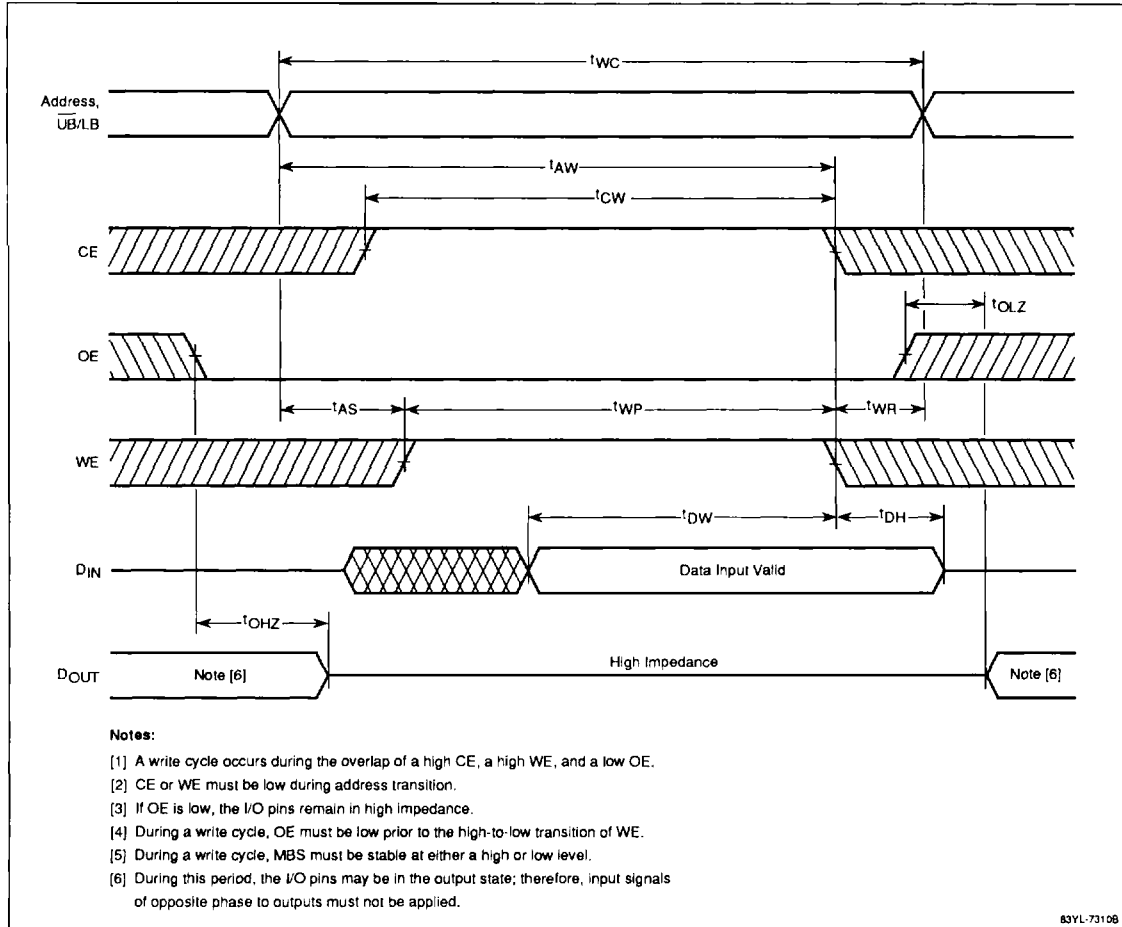


$\overline{CE}$ - and  $\overline{OE}$ -Controlled Read Cycle



## Timing Waveforms (cont)

### Write Cycle



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Timing Waveforms (cont)

Signature Read Cycle

