3.3V CMOS 16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS, 3-STATE OUTPUTS, AND BUS-HOLD

IDT74ALVCHG162280

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 0.40mm pitch TVSOP package
- Commercial range of 0°C to +70°C
- V_{CC} = 3.3V ± 0.3V, Normal Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Low switching noise

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

DESCRIPTION:

This 16-bit to 32-bit registered bus exchanger is manufactured using advanced dual metal CMOS technology. The ALVCHG162280 is intended for use in applications in which data must be transferred from a narrow high-speed bus to a wide lower-frequency bus.

The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low-to-high transition of the clock (CLK) input. For data transfer in the B-to-A direction, the select ($\overline{SEL}$) input selects 1B or 2B data for the A outputs. For data transfer in the A-to-B direction, a two-stage pipeline is provided in the 1B path, with a single storage register in the 2B path. Data flow is controlled by the active-low output enable ($\overline{OE}$) and the direction-control (DIR) inputs. The DIR control pin is registered to synchronize the bus direction changes with the clock.

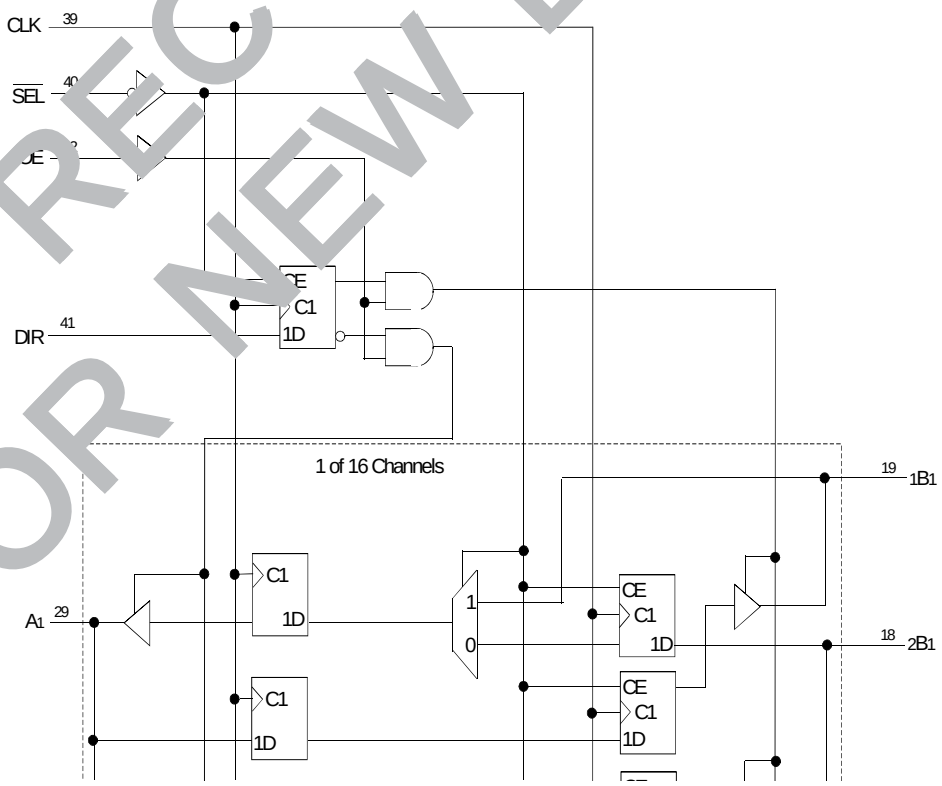
Two mask bits are provided for both data bytes. The data (D) outputs are controlled by $\overline{OE}$.

A port outputs have equivalent 50Ω series resistors. B port outputs have equivalent 20Ω series resistors.

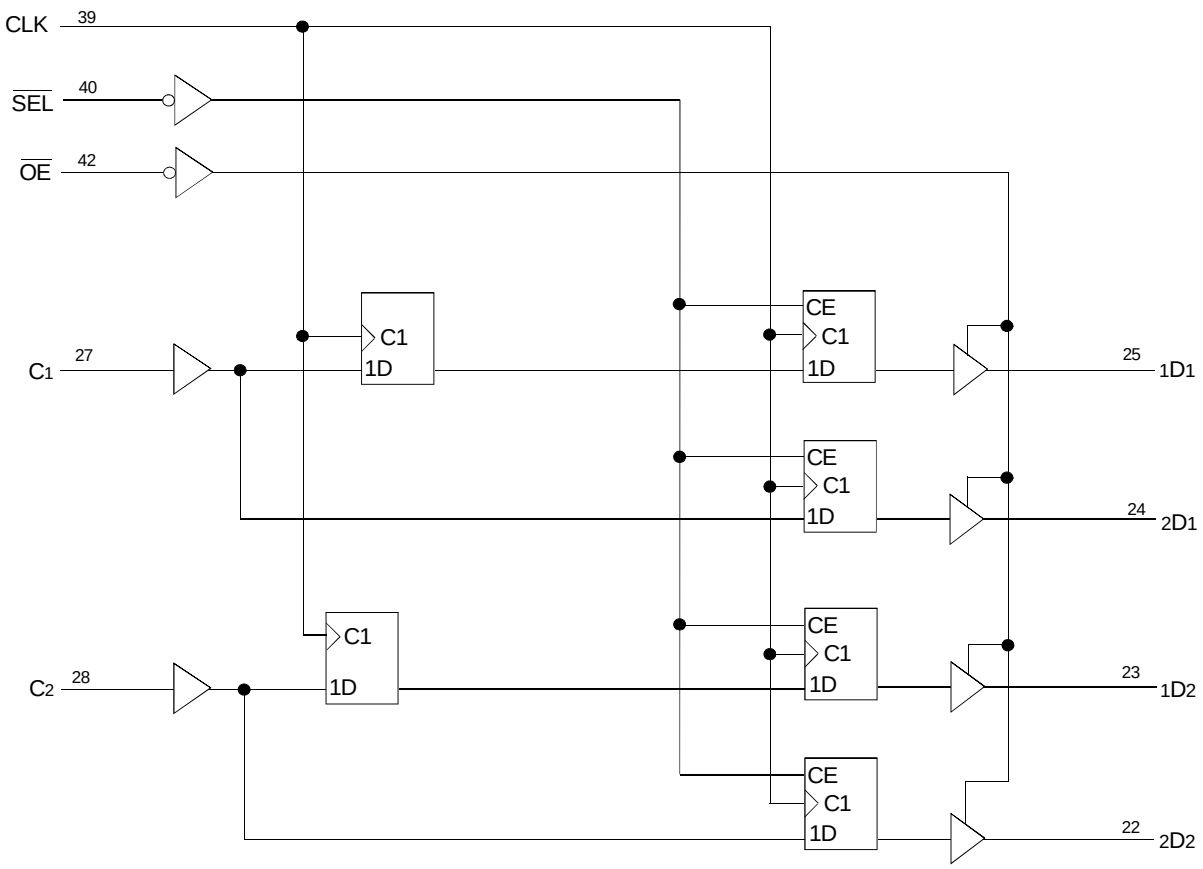
The switching characteristics in this spec, are based on 25pF (A Port) and 80pF (B and D Ports) loads, but production test is accomplished with the standard 50pF load.

The ALVCHG162280 has "bus-hold" which retains the inputs' last state whenever the input bus goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

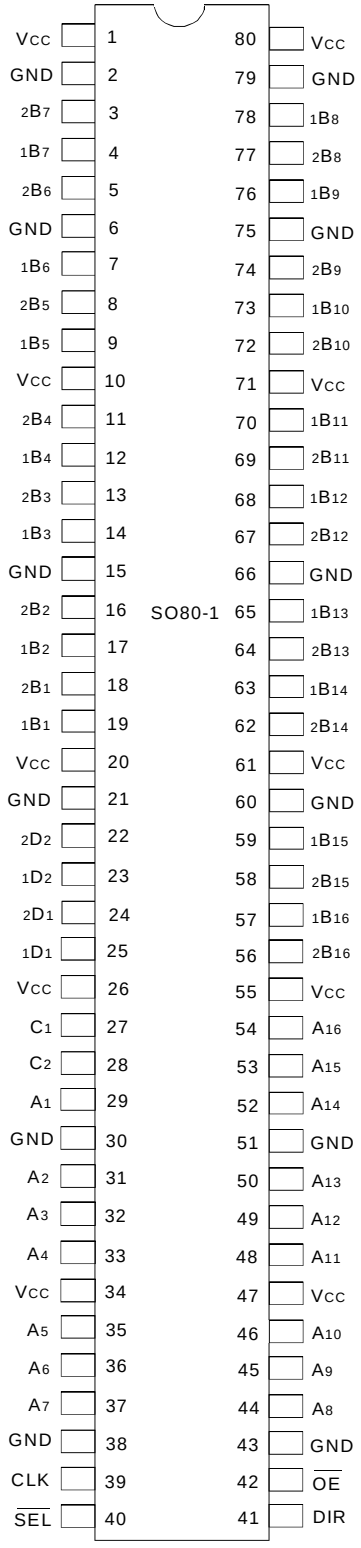
FUNCTIONAL BLOCK DIAGRAM (A and B ports)



FUNCTIONAL BLOCK DIAGRAM (C and D Ports)



PIN CONFIGURATION



TVSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	– 0.5 to + 4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	– 0.5 to V_{CC} + 0.5	V
T_{STG}	Storage Temperature	– 65 to + 150	°C
I_{OUT}	DC Output Current	– 50 to + 50	mA
I_{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I_{OK}	Continuous Clamp Current, $V_O < 0$	– 50	mA
I_{CC} I_{SS}	Continuous Current through each V_{CC} or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance Control Input	V_{IN} = 0V or Vcc	4	—	pF
C_{IN}	Input Capacitance (C port)	V_{IN} = 0V or Vcc	8.5	—	pF
C_{OUT}	Output Capacitance (D port)	V_{OUT} = 0V or GND	7	—	pF
$C_{I/O}$	I/O Port Capacitance (A or B port)	V_{OUT} = 0V or GND	8.5	—	pF

NOTE:
1. As applicable to the device type.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Input (Active LOW)
CLK	Register Input Clock
$\overline{SEL}$	Select Input
Cx	Data Inputs(1)
Ax	Data Inputs(1) and 3-State Outputs
xDx	3-State Outputs
xBx	Data Inputs(1) and 3-State Outputs
DIR	Direction Control Input

NOTE:
1. These pins have “Bus-Hold.” All other pins are standard inputs, outputs, or I/Os.

FUNCTION TABLES(1)

A-TO-B STORAGE ($\overline{OE}$ = L, DIR = H)

Inputs			Outputs	
$\overline{SEL}$	CLK	Ax	$_1$Bx	$_2$Bx
H	X	X	$_1B_0$(2)	$_2B_0$(2)
L	↑	L	L(3)	L
L	↑	H	H(3)	H

C-TO-D STORAGE ($\overline{OE}$ = L)

Inputs			Outputs	
$\overline{SEL}$	CLK	Cx	$_1$Dx	$_2$Dx
H	X	X	$_1D_0$(2)	$_2D_0$(2)
L	↑	L	L(3)	L
L	↑	H	H(3)	H

B-TO-A STORAGE ($\overline{OE}$ = L, DIR = L)

Inputs				Output
$\overline{SEL}$	CLK	$_1$Bx	$_2$Bx	Ax
H	↑	X	L	L(4)
H	↑	X	H	H(4)
L	↑	L	X	L
L	↑	H	X	H

OUTPUT ENABLE

Inputs				Outputs		
CLK	$\overline{OE}$	$\overline{SEL}$	DIR	Ax	$_1$Bx, $_2$Bx	$_1$Dx, $_2$Dx
↑	H	X	X	Z	Z	Z
↑	L	L	H	Z	Active	Active
↑	L	L	L	Active	Z	Active
X	L	H	X	A_0(2)	$1B_0$, $2B_0$(2)	Active

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Transition
   Z = High-Impedance
2. Output level before indicated steady-state input conditions were established.
3. Two CLK edges are needed to propagate the data.
4. Two CLK edges are needed to propagate the data. The data is loaded in the first register when $\overline{SEL}$ is LOW and propagates to the second register when $\overline{SEL}$ is HIGH.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (1)

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: T_A = 0°C to +70°C

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 3V to 3.6V		2	—	—	V
V_{IL}	Input LOW Voltage Level	V_{CC} = 3V to 3.6V		—	—	0.8	V
I_{IH}	Input HIGH Current(2)	V_{CC} = 3.6V	V_I = V_{CC}	—	—	± 5	µA
I_{IL}	Input LOW Current(2)	V_{CC} = 3.6V	V_I = GND	—	—	± 5	
I_{OZH}	High Impedance Output Current	V_{CC} = 3.6V	V_O = V_{CC}	—	—	± 10	µA
I_{OZL}	(excludes bus-hold pins)		V_O = GND	—	—	± 10	µA
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V V_{IN} = GND or V_{CC}		—	0.1	40	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V, other inputs at V_{CC} or GND	V_{CC} = 3-3.6V	—	—	750	µA

NOTES:
1. Typical values are at Vcc = 3.3V, +25°C ambient.
2. For control I/P's only excludes bus-hold current.

BUS-HOLD CHARACTERISTICS

Symbol	Parameter[1]	Test Conditions		Min.	Typ.[2]	Max.	Unit
I_{BHH}	Bus-Hold Input Sustain Current	V_{CC} = 3.0V	V_I = 2.0V	– 75	—	—	µA
I_{BHL}			V_I = 0.8V	75	—	—	
I_{BHHO}	Bus-Hold Input Overdrive Current	V_{CC} = 3.6V	V_I = 0 to 3.6V	—	—	± 500	µA
I_{BHLO}							

NOTES:
1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
	(A port to B port) or (C port to D port)	V_{CC} = 3.0V	I_{OH} = – 8mA	2	—	
	(B port to A port)		I_{OH} = – 6mA	2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3.0V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
	(A port to B port) or (C port to D port)	V_{CC} = 3.0V	I_{OL} = 8mA	—	0.8	
	(B port to A port)		I_{OL} = 6mA	—	0.8	

NOTE:

1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = 0°C to + 70°C.

OPERATING CHARACTERISTICS, T_A = 25ºC

Symbol	Parameter	Test Conditions	V_{CC} = 3.3V ± 0.3V Typical	Unit
C_{PD}	Power Dissipation Capacitance Outputs enabled	C_L = 0pF, f = 10Mhz	80	pF
C_{PD}	Power Dissipation Capacitance Outputs disabled		60	pF

SWITCHING CHARACTERISTICS, C_L = 25pF (A port), 80pF (B and D ports) (1)

Symbol	Parameter	Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay, CLK to Ax	1.5	5	ns
t_{PLH} t_{PHL}	Propagation Delay, CLK to xBx	1.5	7.4	ns
t_{PLH} t_{PHL}	Propagation Delay CLK to xDx	1.5	7.2	ns
t_{PZH} t_{PZL}	Output Enable Time CLK to Ax	1.5	6.2	ns
t_{PZH} t_{PZL}	Output Enable Time CLK to xBx	1.5	9.4	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Ax	1.5	6	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to xBx	1.5	9.5	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to xDx	1.5	7.9	ns
t_{PHZ} t_{PLZ}	Output Disable Time CLK to Ax	1.5	6.4	ns
t_{PHZ} t_{PLZ}	Output Disable Time CLK to xBx	1.5	7.8	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Ax	1.5	5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to xBx	1.5	7.6	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to xDx	1.5	6.7	ns
t_{SU}	Setup Time, HIGH or LOW, Ax data before CLK↑	1.4	—	ns
t_{SU}	Setup Time, HIGH or LOW, xBx data before CLK↑	2	—	ns
t_{SU}	Setup Time, HIGH or LOW, Cx data before CLK↑	1.3	—	ns
t_{SU}	Setup Time, HIGH or LOW, DIR before CLK↑	2	—	ns
t_{SU}	Setup Time, HIGH or LOW, $\overline{SEL}$ before CLK↑	2	—	ns
t_H	Hold Time, HIGH or LOW, Ax data after CLK↑	0.3	—	ns
t_H	Hold Time, HIGH or LOW, xBx data after CLK↑	0.3	—	ns
t_H	Hold Time, HIGH or LOW, Cx data after CLK↑	0.3	—	ns
t_H	Hold Time, HIGH or LOW, DIR after CLK↑	0.3	—	ns
t_H	Hold Time, HIGH or LOW, $\overline{SEL}$ after CLK↑	0.3	—	ns
t_W	Pulse Duration, CLK HIGH or LOW	2.3	—	ns
f_{CLOCK}		—	160	MHz

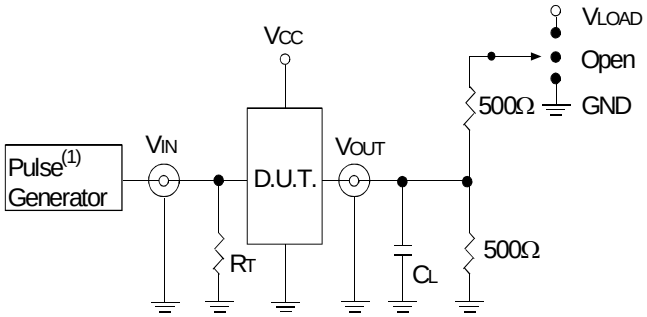
NOTE:
1. See test circuits and waveforms. T_A = 0°C to + 70.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$ = 3.3V ± 0.3V	Unit
V_{LOAD}	6	V
V_{IH}	2.7	V
V_T	1.5	V
V_{LZ}	300	mV
V_{HZ}	300	mV
C_L	25pF (A Port), 80pF (B and D Ports)	pF

TEST CIRCUITS FOR ALL OUTPUTS



ALVC Link

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

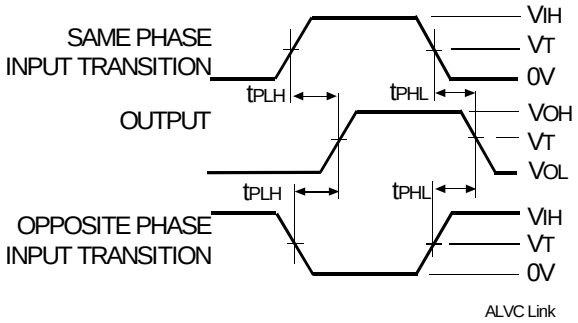
NOTE:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; tF ≤ 2.5ns; tR ≤ 2.5ns

SWITCH POSITION

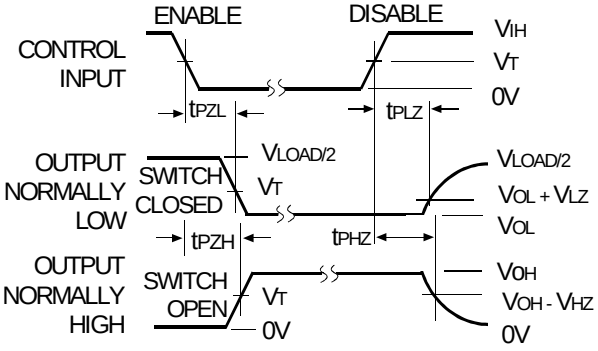
Test	Switch
Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

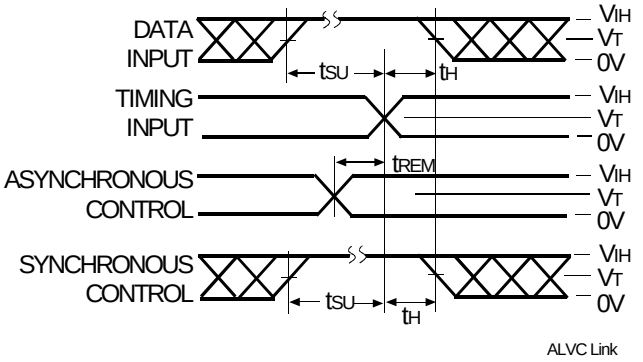


ALVC Link

NOTE:

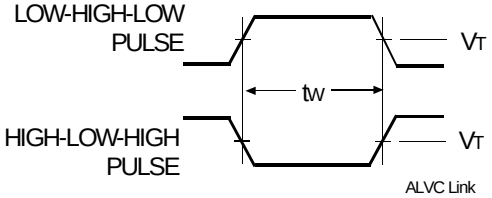
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



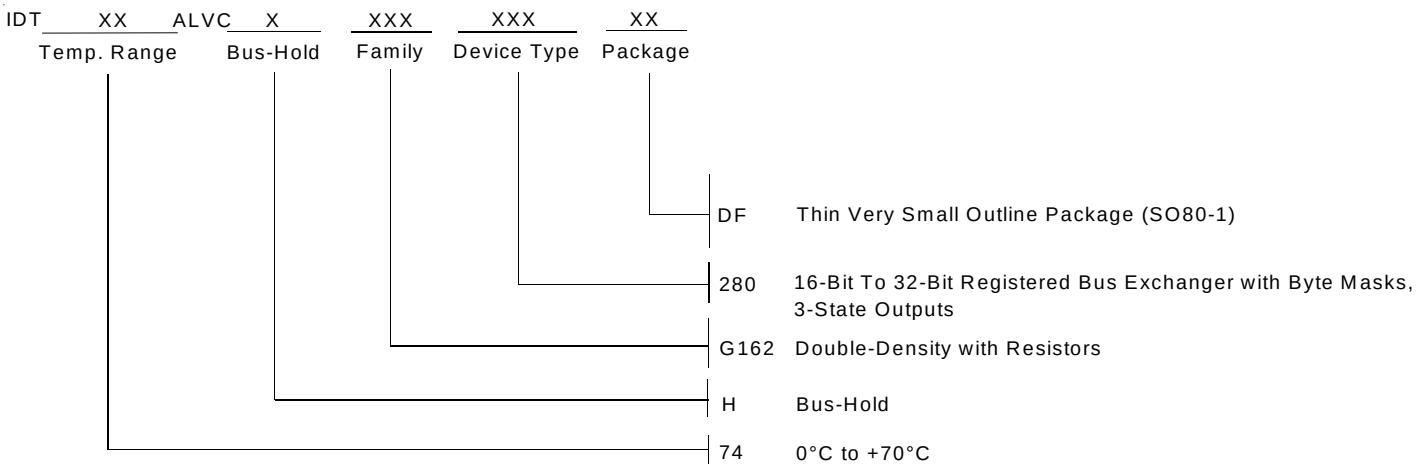
ALVC Link

PULSE WIDTH



ALVC Link

ORDERING INFORMATION



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