NEC

MOS INTEGRATED CIRCUIT

MC-458DA724

8M-WORD BY 72-BIT SYNCHRONOUS DYNAMIC RAM MODULE BUFFERED TYPE

Description

The MC-458DA724 is a 8,388,608 words by 72 bits synchronous dynamic RAM module on which 9 pieces of 64M SDRAM : μPD4564841 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 72 bits organization (ECC type)
- Clock frequency and clock access time

Family	/CAS latency	Clock frequency (MAX.)	Clock access time (MAX.)	Power consumption (MAX.)	
				Active	Standby
MC-458DA724-A80	CL = 3	125 MHz	6.5 ns	4,752 mW	65 mW (CMOS level input)
	CL = 2	83 MHz	8.5 ns	4,590 mW	
MC-458DA724-A10	CL = 3	100 MHz	8.5 ns	4,104 mW	
	CL = 2	67 MHz	9.5 ns	3,942 mW	

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length : 1, 2, 4, 8 and full page
- Programmable wrap sequence (sequential / interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- All I/Os have 10 Ω ± 10 % of series resistor
- Single 3.3 V ± 0.3 V power supply
- LVTTL compatible
- 4,096 refresh cycles / 64 ms
- Burst termination by Burst Stop command and Precharge command
- 168-pin dual in-line memory module (Pin pitch = 1.27 mm)
- Buffered type
- Buffer mode, register mode
- Serial PD

The information in this document is subject to change without notice.

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The mark ★ shows major revised points.

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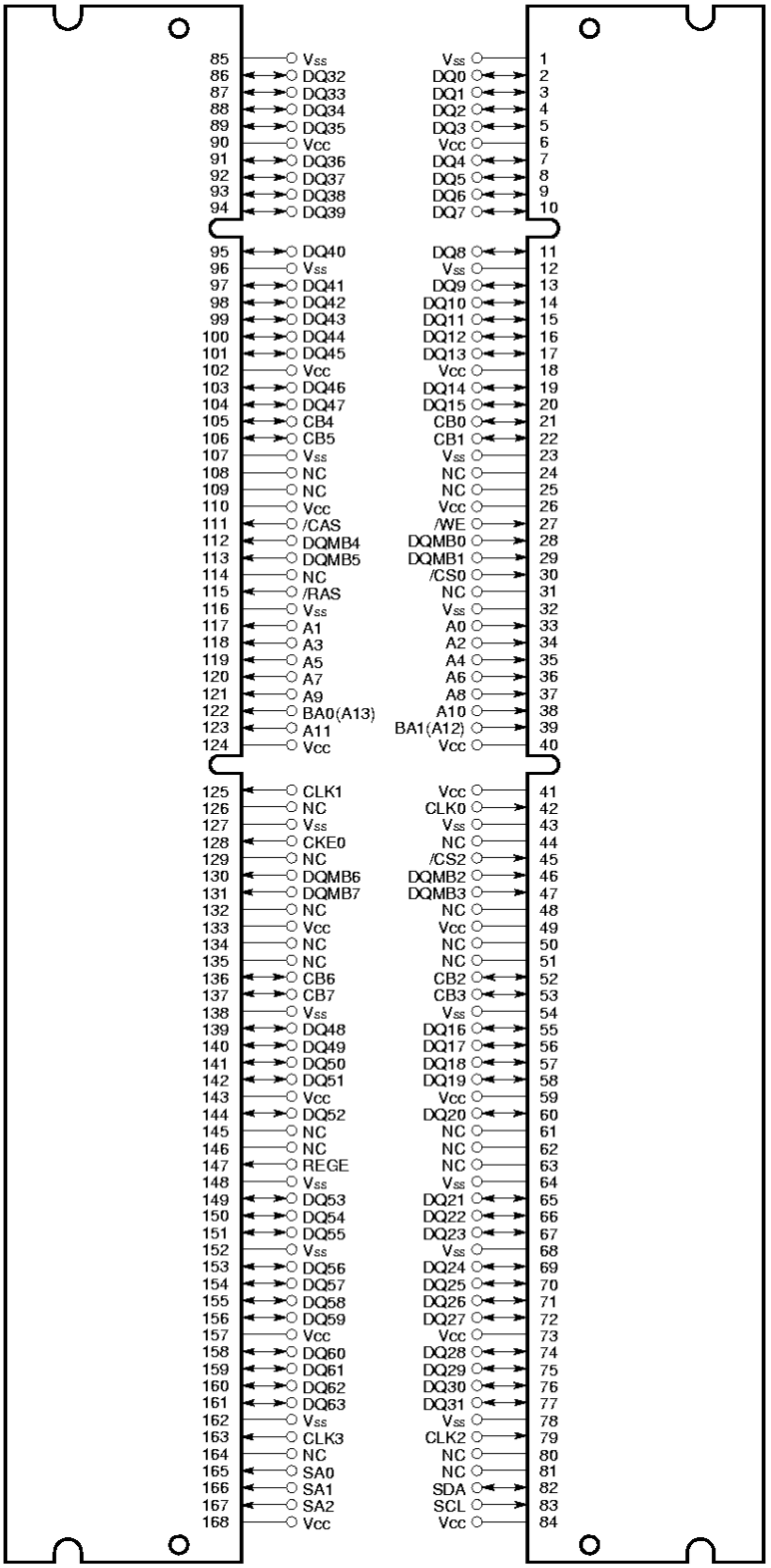
Ordering Information

Part number	Clock frequency (MAX.)	Package	Mounted devices
MC-458DA724F-A80	125 MHz	168-pin Dual In-line Memory Module (Socket Type) Edge connector : Gold plated 41.91 mm (1.65 inch) height	9 pieces of μPD4564841G5 (400 mil TSOP (II)) [Single side]
MC-458DA724F-A10	100 MHz		

Pin Configuration

168-pin Dual In-line Memory Module Socket Type (Edge connector: Gold plated)

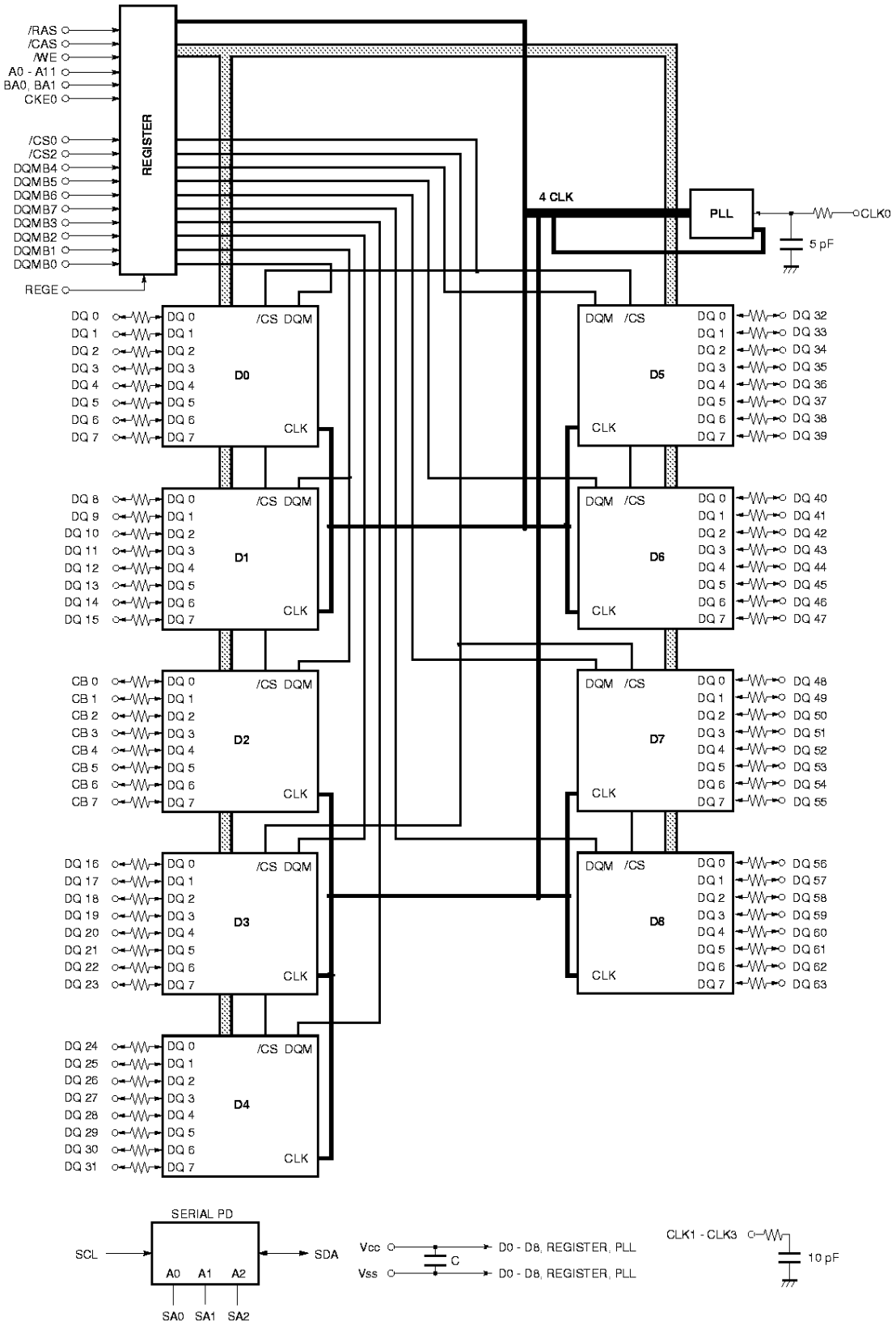
[MC-458DA724F]



/XXX indicates active low signal.

A0 - A11	:	Address Inputs
[Row : A0 - A11, Column : A0 - A8]		
BA0 (A13),		
BA1 (A12)	:	SDRAM Bank Select
DQ0 - DQ63,		
CB0 - CB7	:	Data Inputs / Outputs
CLK0 - CLK3	:	Clock Input
CKE0	:	Clock Enable Input
/CS0, /CS2	:	Chip Select Input
/RAS	:	Row Address Strobe
/CAS	:	Column Address Strobe
/WE	:	Write Enable
DQMB0 - DQMB7	:	DQ Mask Enable
SA0 - SA2	:	Address Input for EEPROM
SDA	:	Serial Data I/O for PD
SCL	:	Clock Input for PD
Vcc	:	Power Supply
Vss	:	Ground
REGE	:	Register / Buffer Enable
NC	:	No Connection

Block Diagram



Remarks 1. The value of all resistors is 10 Ω.

2. D0 - D8 : μPD4564841 (2M words × 8 bits × 4 banks)

3. REGE ≤ V_{IH} : Buffer Mode

REGE ≥ V_{IL} : Register Mode

Electrical Specifications

- All voltages are referenced to V_{SS} (GND).
- After power up, wait more than 100 μs and then, execute power on sequence and auto refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		–0.5 to +4.6	V
Voltage on input pin relative to GND	V_T		–0.5 to +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		12	W
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC}+0.3	V
Low level input voltage	V_{IL}		–0.3		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_{I1}	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE, CKE0, /CS0, /CS2, DQMB0 - DQMB7			10	pF
	C_{I2}	CLK0 - CLK3			8	
Data input / output capacitance	$C_{I/O}$	DQ0 - DQ63, CB0 - CB7			10	pF

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition		Grade	MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC\ (MIN.)}$, I_O = 0 mA	/CAS latency = 2	-A80		870	mA	1
				-A10		780		
			/CAS latency = 3	-A80		915		
				-A10		825		
Precharge standby current in power down mode	$I_{CC2}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns				450	mA	
	$I_{CC2}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞				18		
Precharge standby current in non power down mode	$I_{CC2}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.				330	mA	
	$I_{CC2}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞ , Input signals are stable.				54		
Active standby current in power down mode	$I_{CC3}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 15 ns				195	mA	
	$I_{CC3}PS$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = ∞				36		
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 15 ns, /CS ≥ $V_{IH\ (MIN.)}$, Input signals are changed one time during 30 ns.				375	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞ , Input signals are stable.				90		
Operating current (Burst mode)	I_{CC4}	$t_{CK} \geq t_{CK\ (MIN.)}$, I_O = 0 mA	/CAS latency = 2	-A80		1,005	mA	2
				-A10		870		
			/CAS latency = 3	-A80		1,275		
				-A10		1,095		
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC\ (MIN.)}$	/CAS latency = 2	-A80		1,275	mA	3
				-A10		1,095		
			/CAS latency = 3	-A80		1,320		
				-A10		1,140		
Self refresh current	I_{CC6}	CKE ≤ 0.2 V				18	mA	
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V, All other pins not under test = 0 V			–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V			–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA			2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA				0.4	V	

Notes 1. I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

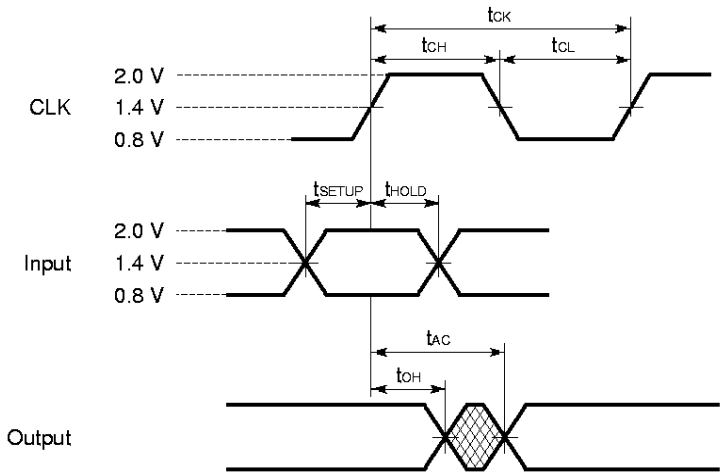
2. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

3. I_{CC5} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

AC Characteristics Test Conditions

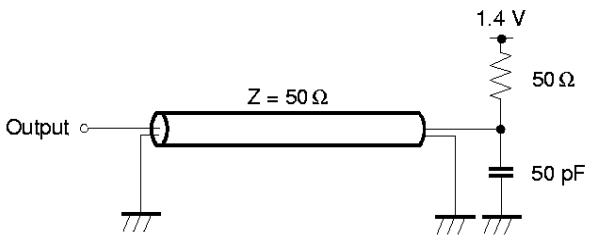
- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\,(MIN.)}$ and $V_{IL\,(MAX.)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics

Parameter		Symbol	-A80				-A10				Unit	Note
			Buffer mode		Register mode		Buffer mode		Register mode			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t_{CK3}	8		8		10		10		ns	
	/CAS latency = 2	t_{CK2}	12		12		15		15		ns	
Access time from CLK	/CAS latency = 3	t_{AC3}		6.5		6.5		8.5		8.5	ns	1
	/CAS latency = 2	t_{AC2}		8.5		8.5		9.5		9.5	ns	1
Input CLK duty cycle			40	60	40	60	40	60	40	60	%	
Data-out hold time	/CAS latency = 3	t_{OH3}	2.5		2.5		2.5		2.5		ns	1
	/CAS latency = 2	t_{OH2}	2.5		2.5		2.5		2.5		ns	1
Data-out low-impedance time		t_{LZ}	0		0		0		0		ns	
Data-out high-impedance time	/CAS latency = 3	t_{HZ3}	3	6	3	6	3	8	3	8	ns	
	/CAS latency = 2	t_{HZ2}	3	8	3	8	3	9	3	9	ns	
Data-in setup time		t_{DS}	2.5		2.5		3.0		3.0		ns	
Data-in hold time		t_{DH}	1.5		1.5		1.5		1.5		ns	
Address setup time		t_{AS}		6.5		2.2		7.0		2.2	ns	
Address hold time		t_{AH}		–2.5		1.2		–2.5		1.2	ns	
CKE setup time		t_{CKS}		6.5		2.2		7.0		2.2	ns	
CKE hold time		t_{CKH}		–2.5		1.2		–2.5		1.2	ns	
CKE setup time (Power down exit)		t_{CKSP}		6.5		2.2		7.0		2.2	ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t_{CMS}		6.5		2.2		7.0		2.2	ns	
Command (/CS0, /CS2, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t_{CMH}		–2.5		1.2		–2.5		1.2	ns	

Note 1. Output load



★ **Remark** These specifications are applied to the monolithic device.

Asynchronous Characteristics

	Parameter		Symbol	-A80		-A10		Unit	Note
				MIN.	MAX.	MIN.	MAX.		
	REF to REF/ACT command period		t_{RC}	80		100		ns	
	ACT to PRE command period		t_{RAS}	48	120,000	60	120,000	ns	
	PRE to ACT command period		t_{RP}	24		30		ns	
	Delay time ACT to READ/WRITE command		t_{RCD}	24		30		ns	
	ACT (0) to ACT (1) command period		t_{RRD}	16		20		ns	
	Data-in to PRE command period		t_{DPL}	8		10		ns	
	Data-in to ACT (REF) command period (Auto precharge)	/CAS latency = 3	t_{DAL3}	1CLK+24		1CLK+30		ns	
		/CAS latency = 2	t_{DAL2}	1CLK+24		1CLK+30		ns	
★	Mode register set cycle time		t_{RSC}	2		2		CLK	
	Transition time		t_T	1	30	1	30	ns	
	Refresh time		t_{REF}		64		64	ms	

Serial PD (1/2)

Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
0	Defines the number of bytes written into serial PD memory		80H	1	0	0	0	0	0	0	0	128 bytes
1	Total number of bytes of serial PD memory		08H	0	0	0	0	1	0	0	0	256 bytes
2	Fundamental memory type		04H	0	0	0	0	0	1	0	0	SDRAM
3	Number of rows		0CH	0	0	0	0	1	1	0	0	12 rows
4	Number of columns		09H	0	0	0	0	1	0	0	1	9 columns
5	Number of banks		01H	0	0	0	0	0	0	0	1	1 bank
6	Data width		48H	0	1	0	0	1	0	0	0	72 bits
7	Data width (continued)		00H	0	0	0	0	0	0	0	0	0
8	Voltage interface		01H	0	0	0	0	0	0	0	1	LVTTL
9	CL = 3 cycle time	-A80	80H	1	0	0	0	0	0	0	0	8 ns
		-A10	A0H	1	0	1	0	0	0	0	0	10 ns
10	CL = 3 access time	-A80	65H	0	1	1	0	0	1	0	1	6.5 ns
		-A10	85H	1	0	0	0	0	1	0	1	8.5 ns
11	DIMM configuration type		02H	0	0	0	0	0	0	1	0	ECC
12	Refresh rate / type		80H	1	0	0	0	0	0	0	0	Normal
13	SDRAM width		08H	0	0	0	0	1	0	0	0	×8
14	Error checking SDRAM width		08H	0	0	0	0	1	0	0	0	×8
15	Minimum clock delay		01H	0	0	0	0	0	0	0	1	1 clock
16	Burst length supported		8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F
17	Number of banks on each SDRAM		04H	0	0	0	0	0	1	0	0	4 banks
18	/CAS latency supported		06H	0	0	0	0	0	1	1	0	2, 3
19	/CS latency supported		01H	0	0	0	0	0	0	0	1	0
20	/WE latency supported		01H	0	0	0	0	0	0	0	1	0
21	SDRAM module attributes		1FH	0	0	0	1	1	1	1	1	Buffered
22	SDRAM device attributes : General		0EH	0	0	0	0	1	1	1	0	
23	CL = 2 cycle time	-A80	C0H	1	1	0	0	0	0	0	0	12 ns
		-A10	F0H	1	1	1	1	0	0	0	0	15 ns
24	CL = 2 access time	-A80	85H	1	0	0	0	0	1	0	1	8.5 ns
		-A10	95H	1	0	0	1	0	1	0	1	9.5 ns
25-26			00H	0	0	0	0	0	0	0	0	
27	$t_{RP\ (MIN.)}$	-A80	18H	0	0	0	1	1	0	0	0	24 ns
		-A10	1EH	0	0	0	1	1	1	1	0	30 ns
28	$t_{RRD\ (MIN.)}$	-A80	10H	0	0	0	1	0	0	0	0	16 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
29	$t_{RCD\ (MIN.)}$	-A80	18H	0	0	0	1	1	0	0	0	24 ns
		-A10	1EH	0	0	0	1	1	1	1	0	30 ns
30	$t_{RAS\ (MIN.)}$	-A80	30H	0	0	1	1	0	0	0	0	48 ns
		-A10	3CH	0	0	1	1	1	1	0	0	60 ns
31	Module bank density		10H	0	0	0	1	0	0	0	0	64M bytes

(2/2)

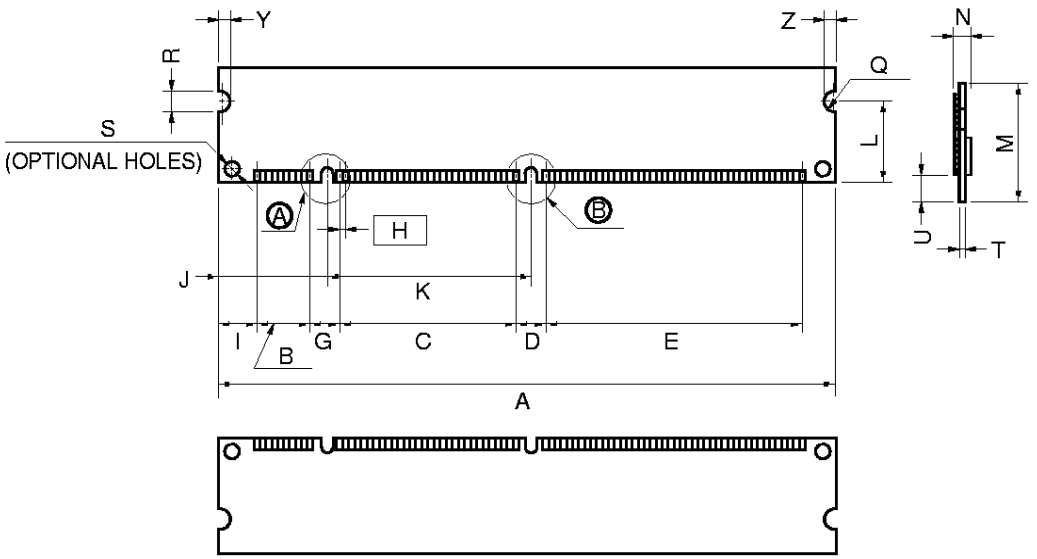
Byte No.	Function Described		Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes
32-61			00H	0	0	0	0	0	0	0	0	
62	SPD revision		01H	0	0	0	0	0	0	0	1	1
63	Checksum for bytes 0 - 62	-A80	F1H	1	1	1	1	0	0	0	1	
		-A10	8DH	1	0	0	0	1	1	0	1	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency		66H	0	1	1	0	0	1	1	0	66 MHz
127	Intel specification /CAS latency support		06H	0	0	0	0	0	1	1	0	2, 3

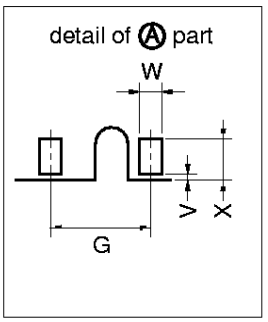
Timing Chart

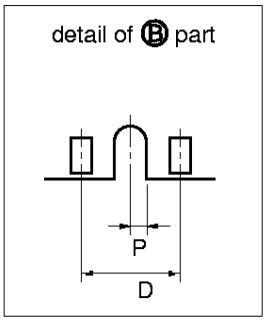
Please refer to NEC Synchronous DRAM Data sheet.

Package Drawing

168 PIN DUAL IN-LINE MODULE (SOCKET TYPE)







ITEM	MILLIMETERS	INCHES
A	133.35±0.13	5.250±0.006
B	11.43	0.450
C	36.83	1.450
D	6.35	0.250
E	54.61	2.150
G	6.35	0.250
H	1.27 (T.P.)	0.050 (T.P.)
I	8.89	0.350
J	24.495	0.964
K	42.18	1.661
L	17.78	0.700
M	41.91	1.650
N	4.0 MAX.	0.158 MAX.
P	1.0	0.039
Q	R2.0	R0.079
R	4.0±0.1	$0.157^{+0.005}_{-0.004}$
S	ϕ3.0	ϕ0.118
T	1.27±0.1	0.05±0.004
U	4.0 MIN.	0.157 MIN.
V	0.25 MAX.	0.010 MAX.
W	1.0±0.05	$0.039^{+0.003}_{-0.002}$
X	2.54 MIN.	0.100±0.004
Y	3.0 MIN.	0.118 MIN.
Z	3.0 MIN.	0.118 MIN.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed imme-diately after power-on for devices having reset function.

[MEMO]

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

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Anti-radioactive design is not implemented in this product.

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