HARRIS SEMICONDUCTOR

NOT RECOMMENDED FOR NEW DESIGNS
See HIP4082

HIP4084

PRELIMINARY

February 1998

80V, 0.50A Four Phase Driver

Features

- Independently Drives 8 N-Channel MOSFETs in Either Four Phase Bridge Configuration or Dual H-Bridge Configuration
- 1.25A Peak Turn-Off Current
- Bootstrap Supply Max Voltage to 95VDC
- Bias Supply Operation from 7V to 15V
- User-Programmable Dead Time (0.25µs to 4.5µs)
- Charge-Pump and Bootstrap Maintain Upper Bias Supplies
- Drives 1000pF Load with Typical Rise Time of 20ns and Fall Time of 10ns
- $\overline{EN}$ (Disable) Overrides Input Control
- Input Logic Thresholds Compatible with 3V to 15V Logic Levels
- Dead Time Disable Capability
- Programmable Undervoltage Set Point

Applications

- Brushless Motors
- AC Motor Drives
- Stepper Motors
- Switched Reluctance Motor Drives

Description

The HIP4084 is a Four Phase Bridge N-Channel MOSFET driver IC.

Specifically targeted for PWM and stepper motor control applications, the HIP4084 makes bridge based designs simple and flexible. With operation up to 80V and undervoltage detection, the device is best suited to applications of moderate power levels.

Like the HIP4081, the HIP4084 has a flexible input protocol for driving every possible switch combination. Like the HIP4082, the HIP4084 provides a typical drive currents of 0.5A and a programmable dead time from 0.25µs to 4.5µs. Like the HIP4086, the HIP4084 allows override of shoot-through protection for switched reluctance applications. The HIP4084 is suitable for applications requiring DC to 100kHz. Unlike other HIP4080 family products, the HIP4084 provides, from a single pin, a programmable undervoltage set point and an enable/disable function.

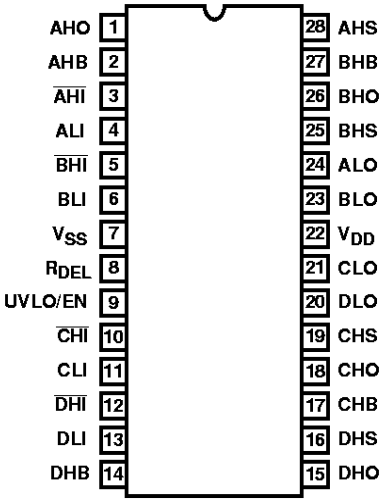
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HIP4084AB	-40 to 105	28 Ld SOIC	M28.3
HIP4084AP	-40 to 105	28 Ld PDIP	E28.6

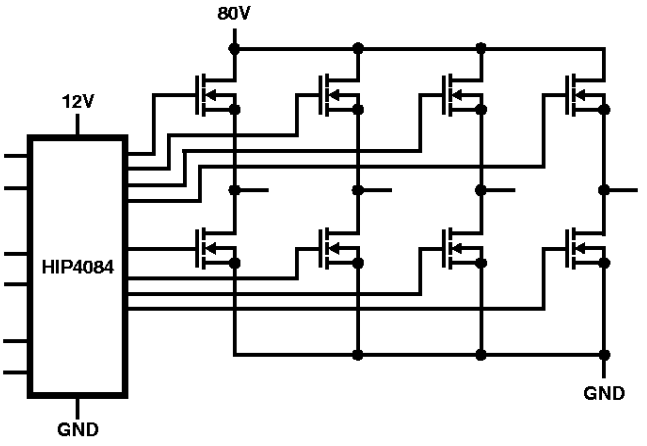
For additional information contact Ivars Lauzums at (407) 729-5531.

Pinout

HIP4084
(PDIP, SOIC)
TOP VIEW



Application Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4222.1**

TRUTH TABLE

INPUT				OUTPUT	
ALI, BLI, CLI, DLI	$\overline{AHI}$, $\overline{BHI}$, $\overline{CHI}$, $\overline{DHI}$	UVLO/EN	R_{DEL}	ALO, BLO, CLO, DLO	AHO, BHO, CHO, DHO
X	X	0	X	0	0
1	X	1	>100mV	1	0
0	0	1	X	0	1
0	1	1	X	0	0
1	0	1	<100mV	1	1

NOTE: X signifies that input can be either a "1" or "0".

Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
2 27 17 14	AHB BHB CHB DHB (xHB)	High-side Bootstrap supplies. One external bootstrap diode and one capacitor are required for each. Connect cathode of bootstrap diode and positive side of bootstrap capacitor to each xHB pin.
3 5 10 12	AHI BHI CHI DHI ($\overline{xHI}$)	High-Side Logic Level Inputs. Logic at these three pins controls the three high-side output drivers, AHO (Pin 1), BHO (Pin 26) and CHO (Pin 18) and DHO (Pin 15). When $\overline{xHI}$ is low, xHO is high. When $\overline{xHI}$ is high, xHO is low. Unless the dead time is disabled by connecting R_{DEL} (Pin 8) to ground, the low side input of each phase will override the corresponding high side input on that phase. If R_{DEL} is tied to ground, dead time is disabled and the outputs follow the inputs. Care must be taken to avoid shoot-through in this application. $\overline{EN}$ (Pin 9) also overrides the high side inputs. $\overline{xHI}$ can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold each $\overline{xHI}$ high if the pins are not driven.
4 6 11 13	ALI BLI CLI DLI (xLI)	Low-Side Logic Level Inputs. Logic at these three pins controls the three low-side output drivers ALO (Pin 24), BLO (Pin 23) and CLO (Pin 21) and DLO (Pin 20). If the upper inputs are grounded then the lower inputs controls both xLO and xHO drivers, with the dead time set by the resistor at R_{DEL} (Pin 8). $\overline{EN}$ (Pin 9) high level input overrides xLI, forcing all outputs low. xLI can be driven by signal levels of 0V to 15V (no greater than V_{DD}). An internal 100µA pull-up to V_{DD} will hold xLI high if these pins are not driven.
7	V_{SS}	Ground. Connect the sources of the low-side power MOSFETs to this pin.
8	R_{DEL}	Dead Time Setting. Connect resistor from this pin to V_{DD} to set timing current that defines the dead time between drivers. All drivers turn-off with no adjustable delay, so the R_{DEL} resistor guarantees no shoot-through by delaying the turn-on of all drivers. When R_{DEL} is tied to V_{SS}, both upper and lowers can be commanded on simultaneously. While not necessary in most applications, a decoupling capacitor of 0.1µF or smaller may be connected between R_{DEL} and V_{SS}.
9	RUV/EN	A resistor can be connected between this pin and V_{SS} to program the under voltage set point. With this pin not connected the undervoltage setpoint is typically 6.6V. When this pin is tied to V_{DD}, the undervoltage setpoint is typically 6.2V. With this pin tied to V_{SS}, all six outputs are taken low, overriding all other inputs.
1 26 18 15	AHO BHO CHO DHO (xHO)	High-Side Outputs. Connect the gates of the high-side power MOSFETs to these pins.
28 25 19 16	AHS BHS CHS DHS (xHS)	High-Side Source connection. Connect the sources of the high-side power MOSFETs to these pins. The negative side of the bootstrap capacitors should also be connected to these pins.
22	V_{DD}	Positive supply. De-couple this pin to V_{SS} (Pin 7).
24 23 21 20	ALO BLO CLO DLO (xLO)	Low-Side Outputs. Connect the gates of the low-side power MOSFETs to these pins.

NOTE: x = A, B, C and D

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, V_{DD} . . . . . -0.3V to 16V
Logic I/O Voltages . . . . . -0.3V to V_{DD} +0.3V
Voltage on xHS . . . . . -6V (Transient) to +85V (-40°C to 150°C)
Voltage on xHB . . . . . V_{xHS} -0.3V to V_{xHS} +V_{DD}
Voltage on xLO . . . . . V_{SS} -0.3V to V_{DD} +0.3V
Voltage on xHO . . . . . V_{xHS} -0.3V to V_{xHB} +0.3V
Phase Slew Rate 20V/ns

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	75°C
PDIP Package	65°C

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

Supply Voltage, V_{DD} . . . . . +7.0V to +15V
Voltage on V_{xHS} . . . . . .0V to 80V
Voltage on xHB . . . . . V_{xHS} + V_{DD}
Operating Ambient Temperature Range . . . . . -40°C to 105°C
Operating Junction Temperature Range . . . . . -40°C to 105°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
2. All voltages are relative to VSS unless otherwise specified.
3. x = A, B, C, and D. For example, xHS refers to AHS, BHS, CHS, and DHS.

Electrical Specifications $V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $R_{DEL} = 20K$, UVLO/EN = ∞, Gate Capacitance (C_{GATE}) = 1000pF

PARAMETER	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 150^oC		UNITS
		MIN	TYP	MAX	MIN	MAX	
SUPPLY CURRENTS AND UNDER VOLTAGE PROTECTION							
V_{DD} Quiescent Current	$\overline{xHI}$ = 5V, xLI = 5V	3	4	5	2	6	mA
V_{DD} Operating Current	f = 20kHz, 50% Duty Cycle	8	9.5	12	7	13	mA
xHB On Quiescent Current	$\overline{xHI}$ = 0V	-	40	80	-	100	µA
xHB Off Quiescent Current	$\overline{xHI}$ = V_{DD}	0.6	0.8	1.3	0.5	1.4	mA
xHB Operating Current	f = 20kHz, 50% Duty Cycle	0.7	0.9	1.3		2.0	mA
Q_{PUMP} Output Voltage	No Load	11.5	12.5	14	10.5	14.5	V
Q_{PUMP} Output Current	V_{xHB} = 10V	-	100	130	-	140	µA
xHB, xHS Leakage Current	V_{xHS} = 80V, V_{xHB} = 93V	7	24	45	-	50	µA
V_{DD} Rising Undervoltage Threshold	R_{UV} Open	6.2	7.1	8.0	6.1	8.1	V
V_{DD} Falling Undervoltage Threshold	R_{UV} Open	5.75	6.6	7.5	5.6	7.6	V
Minimum Undervoltage Threshold	R_{UV} = V_{DD}	5	6.2	6.8	4.9	6.9	V
INPUT PINS: ALI, BLI, CLI, DLI, $\overline{AHI}$, $\overline{BHI}$, $\overline{CHI}$, $\overline{DHI}$, AND $\overline{EN}$							
Low Level Input Voltage		-	-	1.0	-	0.8	V
High Level Input Voltage		2.5	-	-	2.7	-	V
Input Voltage Hysteresis		-	35	-	-	-	mV
Low Level Input Current	V_{IN} = 0V	60	100	135	55	140	µA
High Level Input Current	V_{IN} = 5V	-1	-	1	-10	10	µA
GATE DRIVER OUTPUT PINS: ALO, BLO, CLO, DLO, AHO, BHO, CHO, AND DHO							
Low Level Output Voltage (V_{OUT}-V_{SS})	$I_{SINKING}$ = 30mA	-	100	-	-	200	mV
Peak Pulse Pullup Current	V_{OUT} 0V to 5V	0.3	0.5	0.7	-	1.0	A

Electrical Specifications $V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $R_{DEL} = 20K$, UVLO/EN = ∞, Gate Capacitance (C_{GATE}) = 1000pF

PARAMETER	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 150^oC		UNITS
		MIN	TYP	MAX	MIN	MAX	
Peak Pulse Pulldown Current	V_{OUT} 12V to 4V	0.7	1.1	1.5	0.5	1.7	A

Switching Specifications $V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $R_{DEL} = 10K$, Gate Capacitance (C_{GATE}) = 1000pF

PARAMETER	TEST CONDITIONS	$T_J = 25^oC$			$T_J = -40^oC$ TO 150^oC		UNITS
		MIN	TYP	MAX	MIN	MAX	
TURN ON DELAY AND PROPAGATION DELAY							
Dead Time	$R_{DEL} = 100K$	3.8	4.5	6	3	7	µs
	$R_{DEL} = 10K$	0.38	0.5	0.65	0.3	0.7	µs
Dead Time Channel Matching	$R_{DEL} = 10K$	-	7	15	-	20	%
Lower Turn-Off Propagation Delay (xLI-xLO)	No Load	-	25	50	-	70	ns
Upper Turn-Off Propagation Delay (xHI-xHO)	No Load	-	55	80	-	100	ns
Lower Turn-On Propagation Delay (xLI-xLO)	No Load	-	40	85	-	100	ns
Upper Turn-On Propagation Delay (xHI-xHO)	No Load	-	75	110	-	150	ns
Rise Time	$C_{GATE} = 1000pF$	-	20	40	-	50	ns
Fall Time	$C_{GATE} = 1000pF$	-	10	20	-	25	ns
Turn-On Input Pulse Width		50	-	-	50	-	ns
Turn-Off Input Pulse Width		50	-	-	50	-	ns
Disable ($\overline{EN}$) Turn-Off Propagation Delay ($\overline{EN}$ - $\overline{xLO}$)		-	50	80		90	ns
Disable ($\overline{EN}$) Turn-Off Propagation Delay ($\overline{EN}$ - $\overline{xHO}$)		-	75	100	-	125	ns
Enable to Lower Turn-On Propagation Delay (EN - xLO)		-	50	80	-	100	ns
Enable to Upper Turn-On Propagation Delay (EN- xHO)	$R_{DEL} = 10K$	-	1.2	2	-	3	µs
Refresh Pulse Width (xLO)		375	580	900	350	950	µs