

PSRAM

2-Mbit (128K x 16)

Pseudo Static RAM

Features

- Wide voltage range: 2.7V–3.6V
- Access Time: 55 ns, 70 ns
- Ultra-low active power
  - Typical active current: 1mA @ f = 1 MHz
  - Typical active current: 14 mA @ f = fmax (For 55-ns)
  - Typical active current: 8 mA @ f = fmax (For 70-ns)
- Ultra low standby power
- Automatic power-down when deselected
- CMOS for optimum speed/power

Functional Description

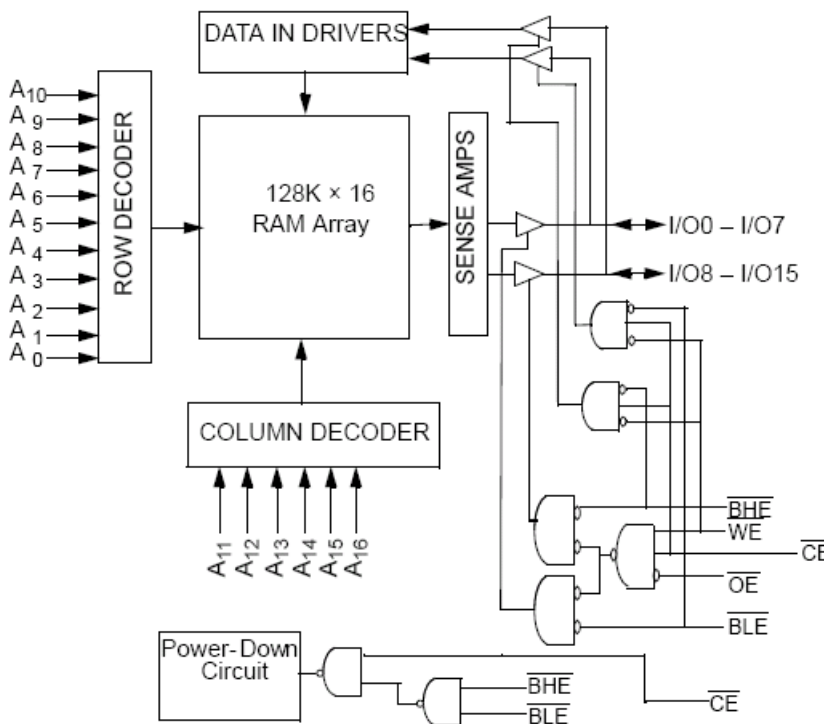
The M24L216128SA is a high-performance CMOS Pseudo Static RAM organized as 128K words by 16 bits that supports an asynchronous memory interface. This device features advanced circuit design to provide ultra-low active current. This is ideal for portable applications such as cellular telephones. The device can be put into standby mode when deselected ( $\overline{CE}$  HIGH or both  $\overline{BHE}$  and  $\overline{BLE}$  are HIGH). The input/output pins (I/O<sub>0</sub> through I/O<sub>15</sub>) are placed in a high-impedance state when the chip is deselected ( $\overline{CE}$  HIGH), or when the outputs are disabled ( $\overline{OE}$  HIGH), or

when both Byte High Enable and Byte Low Enable are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

Writing to the device is accomplished by asserting Chip Enable ( $\overline{CE}$  LOW) and Write Enable ( $\overline{WE}$ ) input LOW. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins (I/O<sub>0</sub> through I/O<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins (I/O<sub>8</sub> through I/O<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>16</sub>).

Reading from the device is accomplished by asserting Chip Enable ( $\overline{CE}$  LOW) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on I/O<sub>8</sub> to I/O<sub>15</sub>. Refer to the truth table for a complete description of read and write modes.

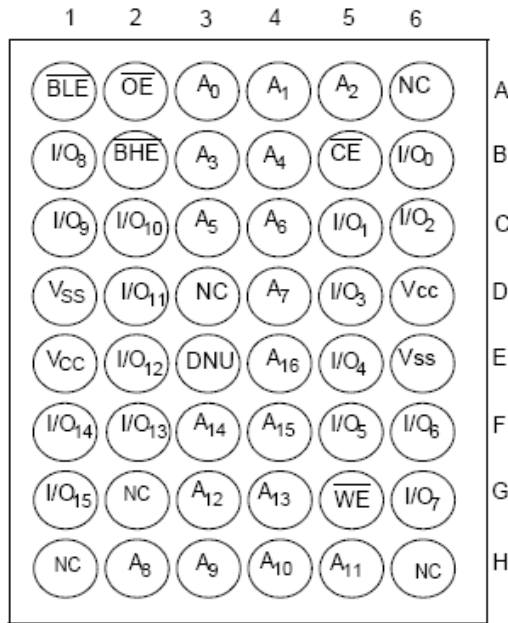
Logic Block Diagram



Pin Configuration[2, 3, 4]

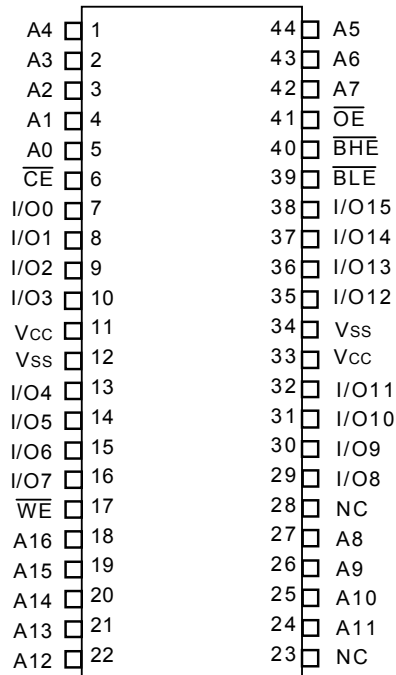
48-ball VFBGA

Top View



44-pin TSOPII

Top View



## Product Portfolio Product

Product	V <sub>CC</sub> Range (V)			Speed(ns)	Power Dissipation					
					Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub> (μA)	
	f = 1MHz		f = fmax							
	Min.	Typ.	Max.		Typ.[5]	Max.	Typ.[5]	Max.	Typ. [5]	Max.
M24L216128SA	2.7	3.0	3.6	55	1	5	14	22	9	40
				70			8	15		

### Notes:

2. Ball D3, H1, G2 and ball H6 for the FBGA package can be used to upgrade to a 4-Mbit, 8-Mbit, 16-Mbit and a 32-Mbit density, respectively.
3. NC "no connect"—not connected internally to the die.
4. DNU (Do Not Use) pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ.)</sub>, T<sub>A</sub> = 25°C.

### Maximum Ratings

(Above which the useful life may be impaired. For user guide-lines, not tested.)  
 Storage Temperature .....-65°C to +150°C  
 Ambient Temperature with Power Applied .....-55°C to +125°C  
 Supply Voltage to Ground Potential .....-0.4V to 4.6V  
 DC Voltage Applied to Outputs in High-Z State[3, 4, 5] .....-0.4V to 3.7V  
 DC Input Voltage[3, 4, 5] .....-0.4V to 3.7V  
 Output Current into Outputs (LOW) .....20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)  
 Latch-up Current .....> 200 mA

### Operating Range

Range	Ambient Temperature(T <sub>A</sub> )	V <sub>CC</sub>
Extended	-25°C to +85°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

### Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions	-55			-70			Unit
			Min.	Typ [5]	Max.	Min.	Typ. [5]	Max.	
V <sub>CC</sub>	Supply Voltage		2.7	3.0	3.6	2.7	3.0	3.6	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA, V <sub>CC</sub> = 2.70V	V <sub>CC</sub> -0.4			V <sub>CC</sub> -0.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA, V <sub>CC</sub> = 2.70V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 2.7V to 3.6V	0.8* V <sub>CC</sub>		V <sub>CC</sub> +0.4V	0.8* V <sub>CC</sub>		V <sub>CC</sub> +0.4V	V
V <sub>IL</sub>	Input LOW Voltage		-0.4		0.4	-0.4		0.4	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>MAX</sub> = 1/t <sub>RC</sub> , V <sub>CC</sub> = V <sub>CCmax</sub> , I <sub>OUT</sub> = 0mA, CMOS levels		14	22		8	15	mA
		f = 1 MHz		1	5		1	5	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≤ 0.2V, f = f <sub>MAX</sub> (Address and Data Only), f = 0 ( $\overline{OE}$ , $\overline{WE}$ , $\overline{BHE}$ and $\overline{BLE}$ ), V <sub>CC</sub> =3.6V		40	250		40	250	μA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.2V$ V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or V <sub>IN</sub> ≤ 0.2V, f = 0, V <sub>CC</sub> =3.6V		9	40		9	40	μA

### Capacitance[9]

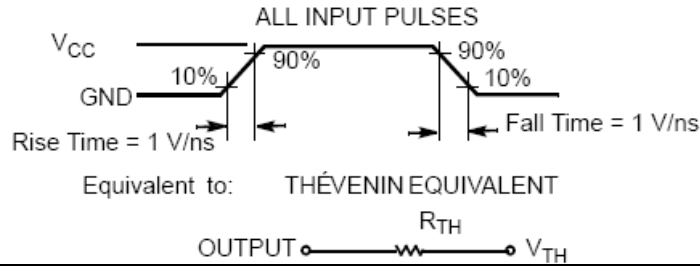
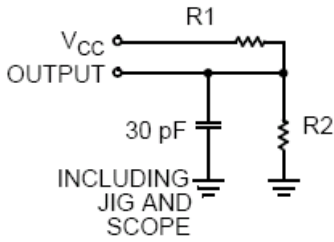
Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	TA = 25°C, f = 1 MHz	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = V <sub>CC(typ)</sub>	8	pF

### Thermal Resistance[9]

Parameter	Description	Test Conditions	BGA	Unit
θJA	Thermal Resistance(Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/ JESD51.	55	°C/W
θJC	Thermal Resistance (Junction to Case)		17	°C/W

- Notes: 6. V<sub>IL(MIN)</sub> = -0.5V for pulse durations less than 20 ns.  
 7. V<sub>IH(Max)</sub> = V<sub>CC</sub> + 0.5V for pulse durations less than 20 ns.  
 8. Overshoot and undershoot specifications are characterized and are not 100% tested.  
 9. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Parameters	3.0V V <sub>CC</sub>	Unit
R1	22000	Ω
R2	22000	Ω
R <sub>TH</sub>	11000	Ω
V <sub>TH</sub>	1.50	V

## Switching Characteristics Over the Operating Range[10]

Parameter	Description	-55 [14]		-70		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
t <sub>RC</sub>	Read Cycle Time	55[14]		70		ns
t <sub>AA</sub>	Address to Data Valid		55		70	ns
t <sub>OHA</sub>	Data Hold from Address Change	5		10		ns
t <sub>ACE</sub>	$\overline{CE}$ LOW to Data Valid		55		70	ns
t <sub>DOE</sub>	$\overline{OE}$ LOW to Data Valid		25		35	ns
t <sub>LZOE</sub>	$\overline{OE}$ LOW to LOW Z[11, 13]	5		5		ns
t <sub>HZOE</sub>	$\overline{OE}$ HIGH to High Z[11, 13]		25		25	ns
t <sub>LZCE</sub>	$\overline{CE}$ LOW to Low Z[11, 13]	2		5		ns
t <sub>HZCE</sub>	$\overline{CE}$ HIGH to High Z[11, 13]		25		25	ns
t <sub>DBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		55		70	ns
t <sub>LZBE</sub>	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[11, 13]	5		5		ns
t <sub>HZBE</sub>	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[11, 13]		10		25	ns
t <sub>SK</sub> [14]	Address Skew		0		10	ns
<b>Write Cycle[12]</b>						
t <sub>WC</sub>	Write Cycle Time	55		70		ns
t <sub>SCE</sub>	$\overline{CE}$ LOW to Write End	45		60		ns
t <sub>AW</sub>	Address Set-Up to Write End	45		60		ns
t <sub>HA</sub>	Address Hold from Write End	0		0		ns
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		ns
t <sub>PWE</sub>	$\overline{WE}$ Pulse Width	40		45		ns

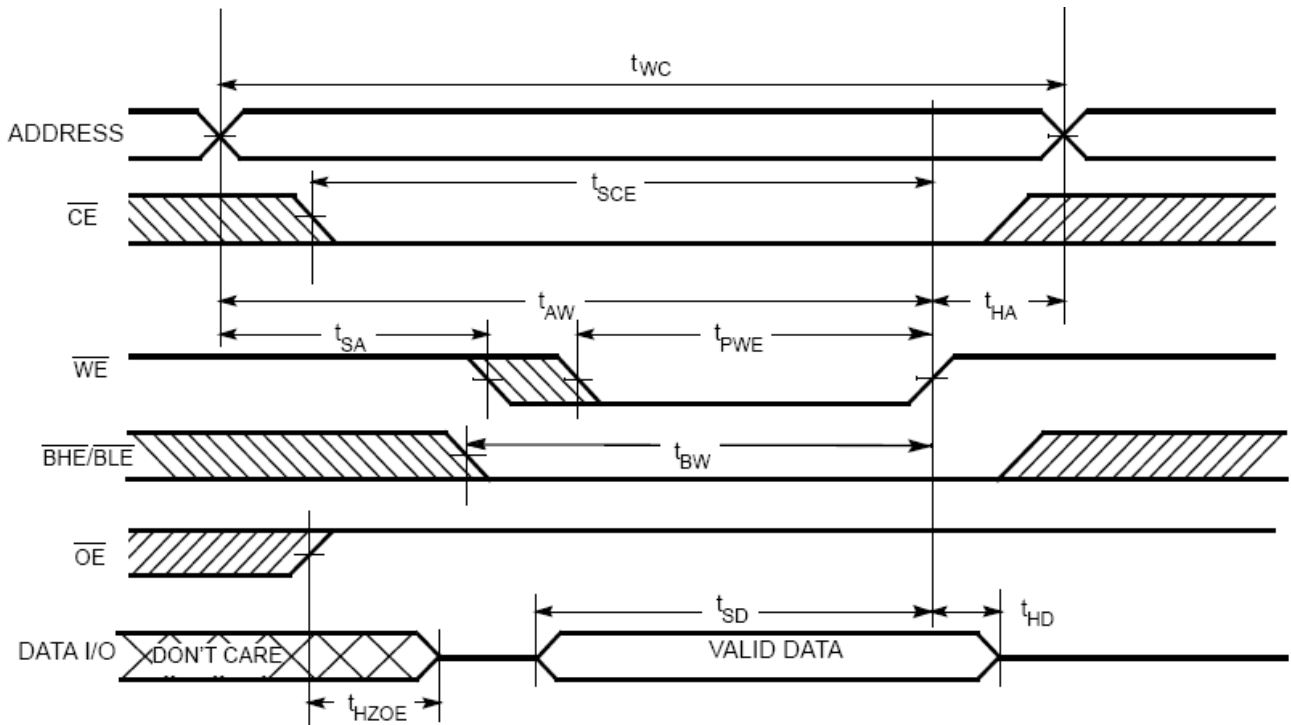
### Notes:

- Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0V to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high impedance state.
- The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  and/or  $\overline{BLE} = V_{IL}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
- High-Z and Low-Z parameters are characterized and are not 100% tested.
- To achieve 55-ns performance, the read access should be  $\overline{CE}$  controlled. In this case  $t_{ACE}$  is the critical parameter and  $t_{SK}$  is satisfied when the addresses are stable prior to chip enable going active. For the 70-ns cycle, the addresses must be stable within 10 ns after the start of the read cycle.

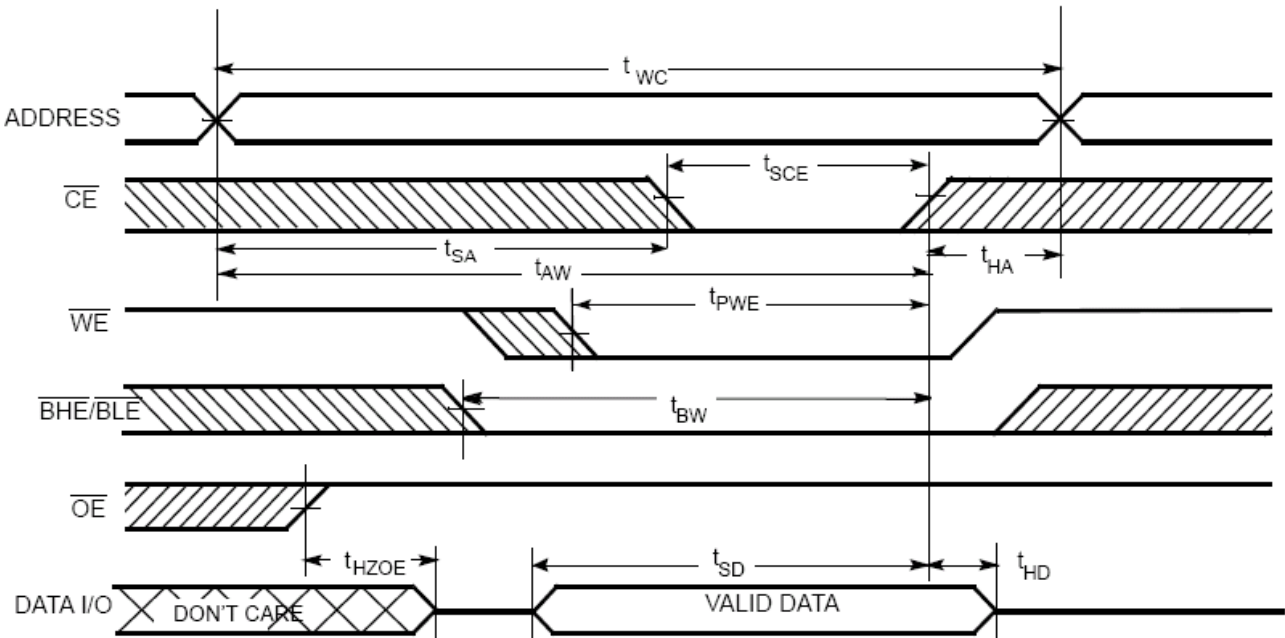


Switching Waveforms (continued)

Write Cycle 1 ( $\overline{WE}$  Controlled)[12, 13, 18, 19, 20]



Write Cycle 2 ( $\overline{CE}$  Controlled)[12, 13, 18, 19, 20]



Notes:

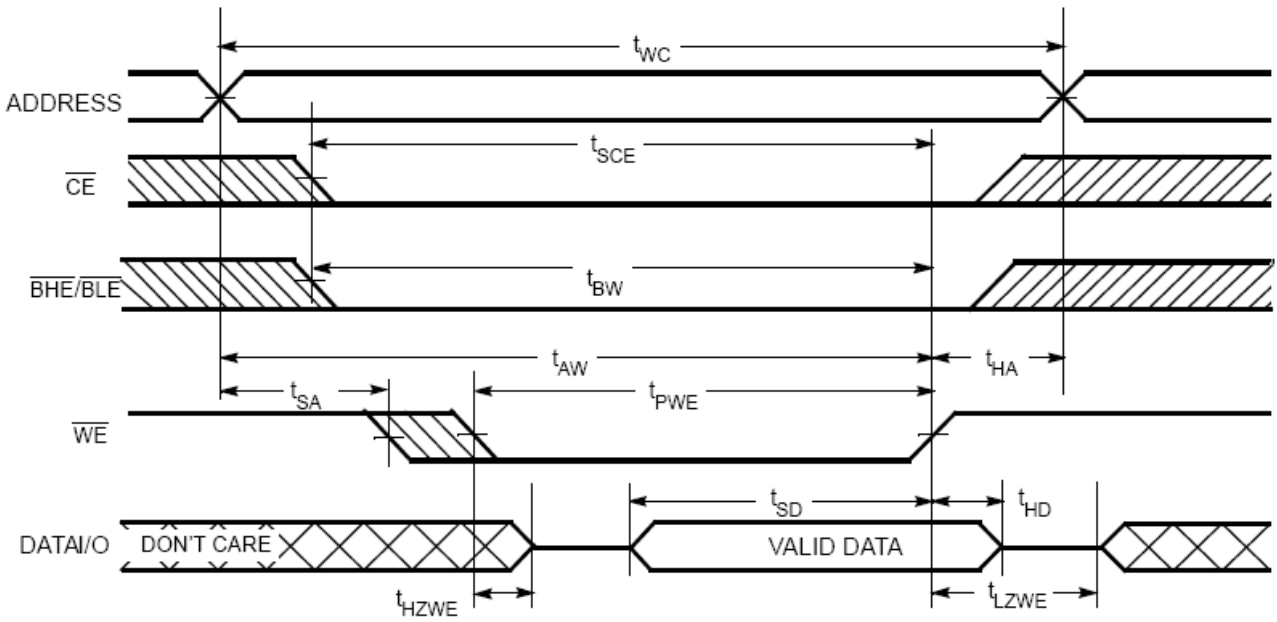
18.Data I/O is high impedance if  $\overline{OE} \geq V_{IH}$ .

19.If Chip Enable goes INACTIVE with  $\overline{WE} = V_{IH}$ , the output remains in a high-impedance state.

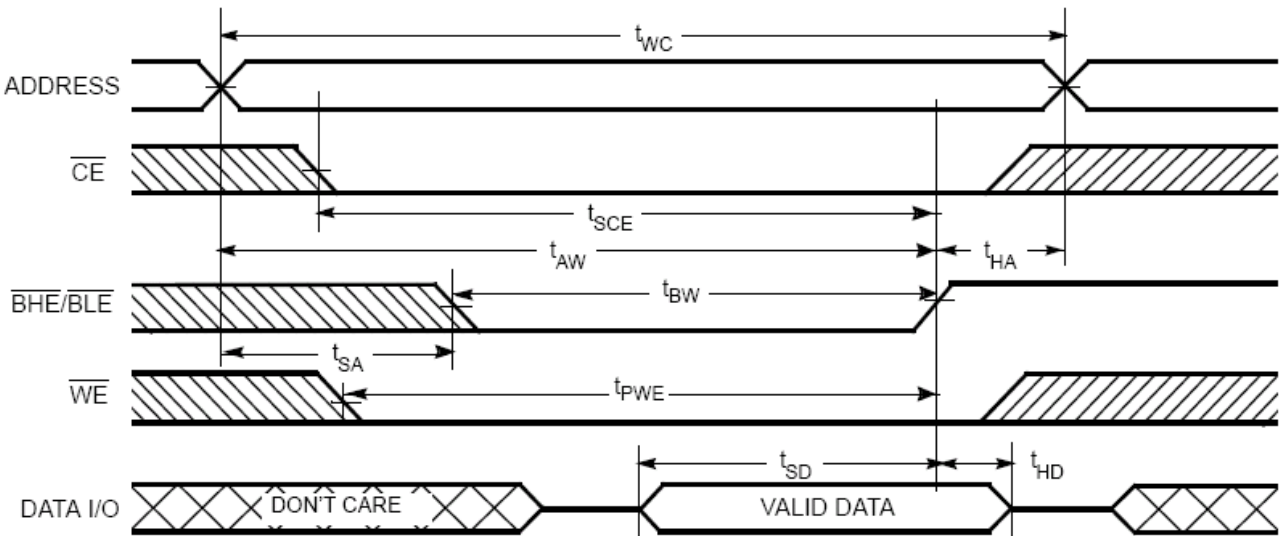
20.During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)[19, 20]



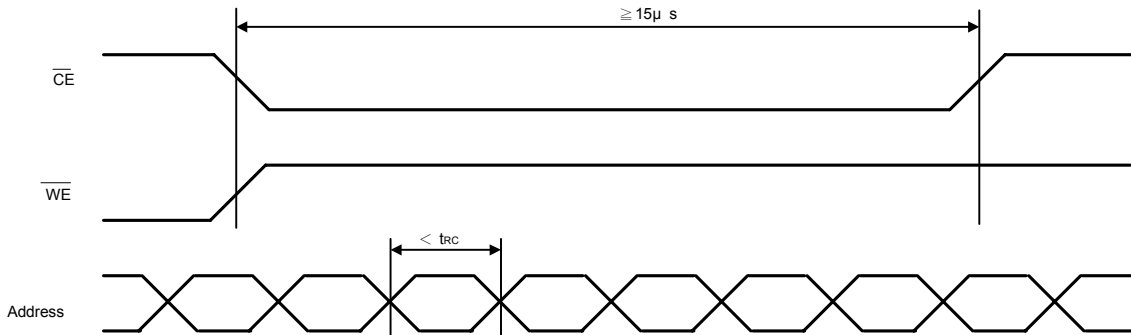
Write Cycle 4 ( $\overline{BHE}/\overline{BLE}$  Controlled,  $\overline{OE}$  LOW)[19, 20]



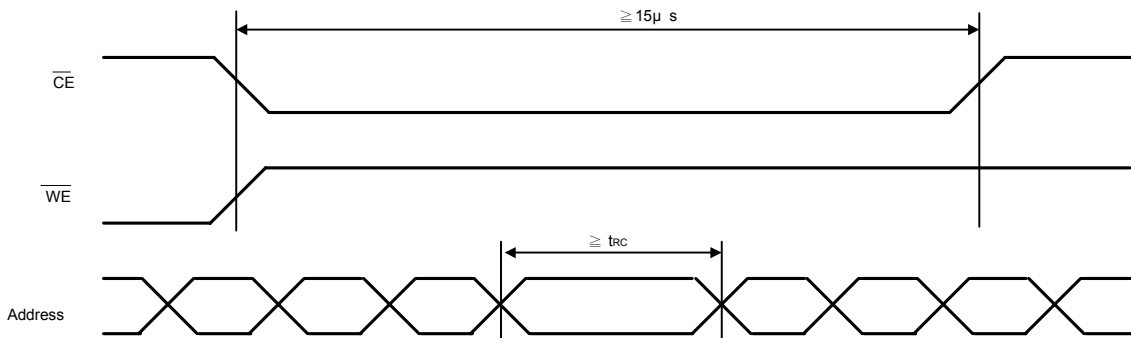
## Avoid Timing

ESMT Pseudo SRAM has a timing which is not supported at read operation, If your system has multiple invalid address signal shorter than  $t_{RC}$  during over  $15\mu s$  at read operation shown as in Abnormal Timing, it requires a normal read timing at least during  $15\mu s$  shown as in Avoidable timing 1 or toggle  $\overline{CE}$  to high ( $\geq t_{RC}$ ) one time at least shown as in Avoidable Timing 2.

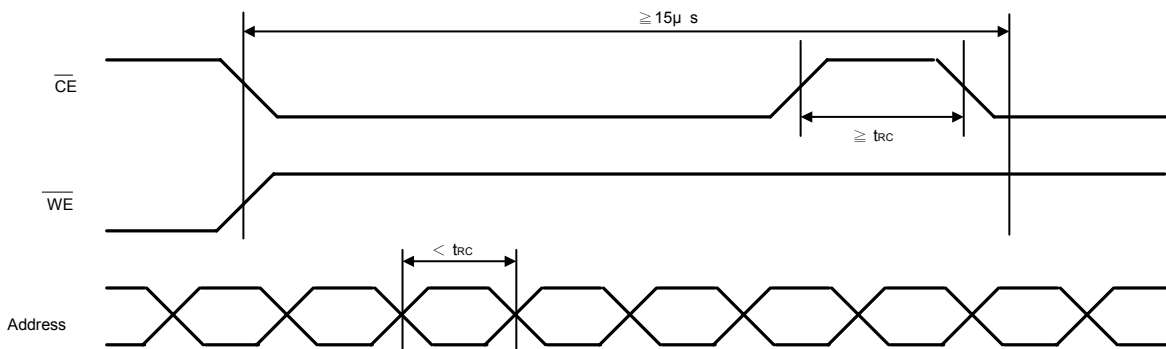
## Abnormal Timing



## Avoidable Timing 1



## Avoidable Timing 2



**Truth Table[21]**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	L	L	Data Out ( $I/O_0-I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	H	L	Data Out ( $I/O_0-I/O_7$ ); High Z ( $I/O_8-I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	L	L	H	High Z ( $I/O_0-I/O_7$ ); Data Out ( $I/O_8-I/O_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	L	X	L	L	Data In ( $I/O_0-I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	H	L	Data In ( $I/O_0-I/O_7$ ); High Z ( $I/O_8-I/O_{15}$ )	Write	Active ( $I_{CC}$ )
L	L	X	L	H	High Z ( $I/O_0-I/O_7$ ); Data In ( $I/O_8-I/O_{15}$ )	Write	Active ( $I_{CC}$ )

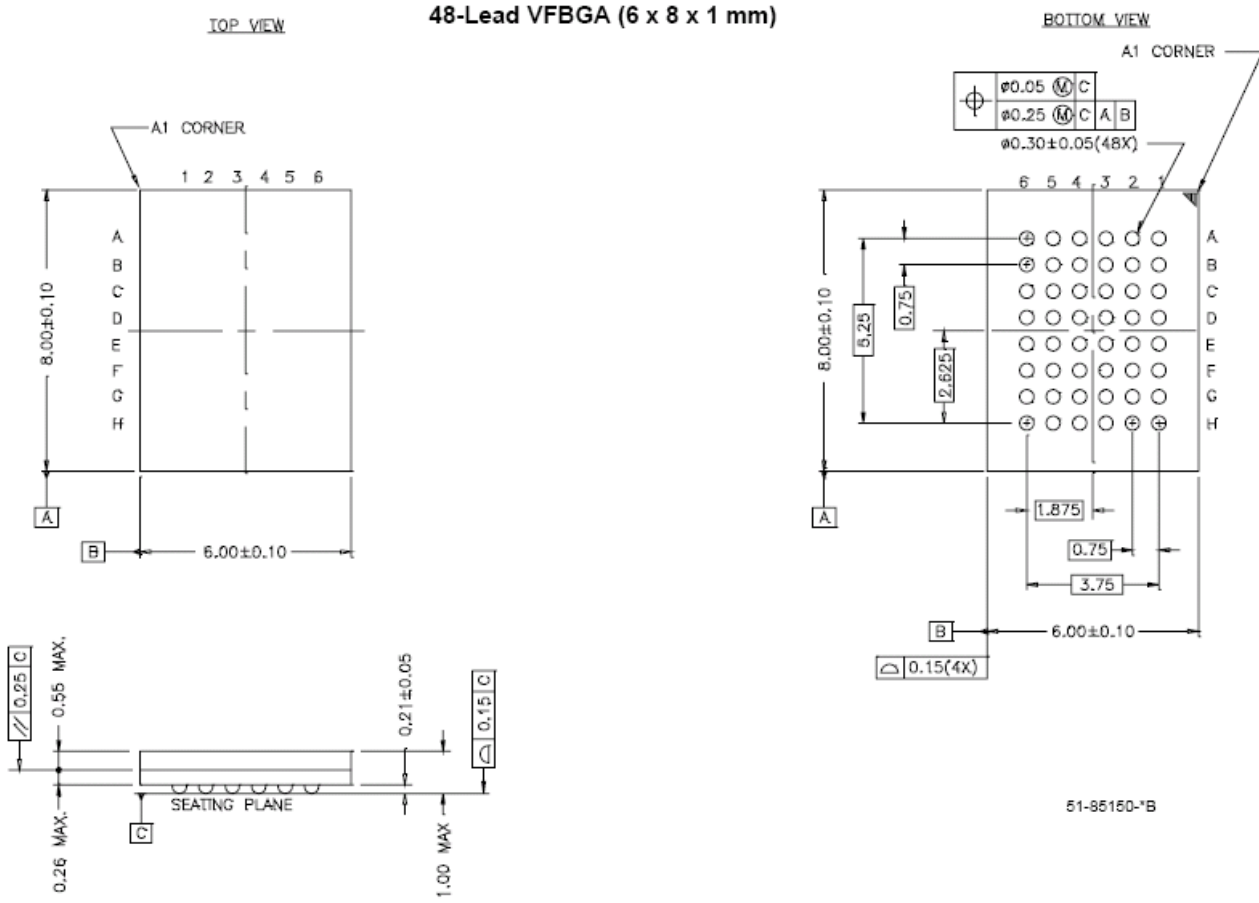
Note:

21.H = Logic HIGH, L = Logic LOW, X = Don't Care.

## Ordering information

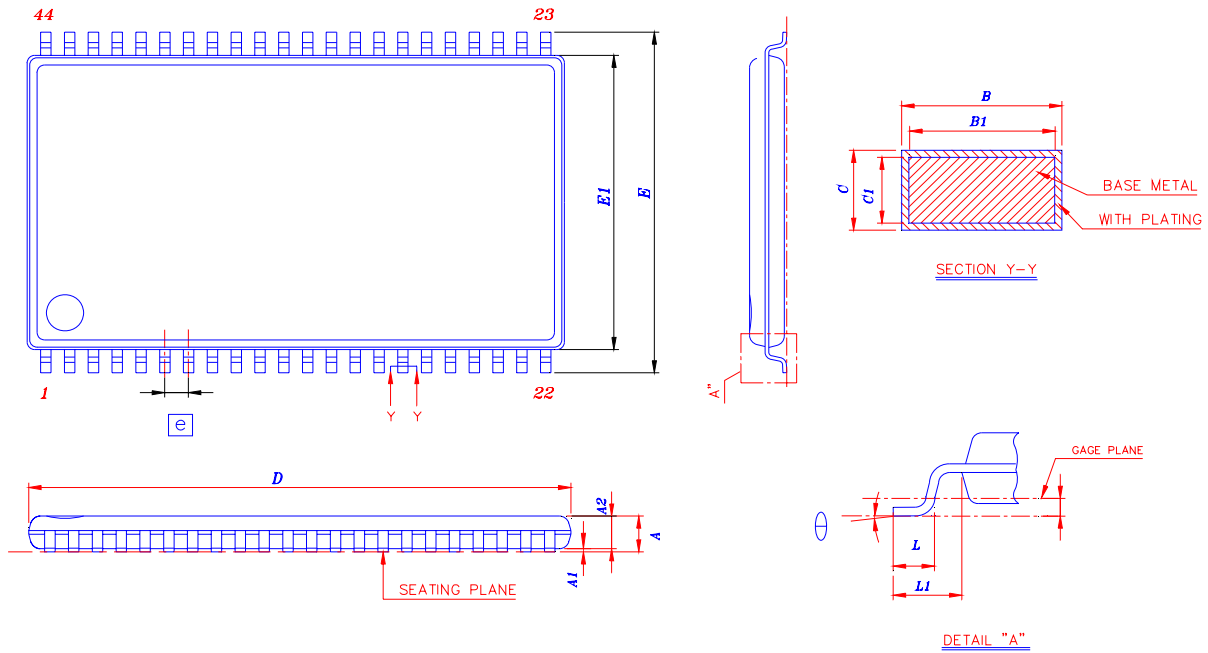
Speed(ns)	Ordering Code	Package Type	Operating Range
55	M24L216128SA-55BEG	48-ball Very Fine Pitch BGA (6.0x8.0x1.0mm) (Pb-free)	Extended
70	M24L216128SA-70BEG	48-ball Very Fine Pitch BGA (6.0x8.0x1.0mm) (Pb-free)	Extended
55	M24L216128SA-55TEG	44-pin TSOPII (Pb-free)	Extended
70	M24L216128SA-70TEG	44-pin TSOPII (Pb-free)	Extended
55	M24L216128SA-55BIG	48-ball Very Fine Pitch BGA (6.0x8.0x1.0mm) (Pb-free)	Industrial
70	M24L216128SA-70BIG	48-ball Very Fine Pitch BGA (6.0x8.0x1.0mm) (Pb-free)	Industrial
55	M24L216128SA-55TIG	44-pin TSOPII (Pb-free)	Industrial
70	M24L216128SA-70TIG	44-pin TSOPII (Pb-free)	Industrial

## Package Diagram



44-LEAD TSOP(II)

PRAM(400mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
B	0.30	—	0.45	0.012	—	0.018
B1	0.30	0.35	0.40	0.012	0.014	0.016
C	0.12	—	0.21	0.005	—	0.008
C1	0.10	—	0.16	0.004	—	0.006
D	18.28	18.41	18.54	0.720	0.725	0.730
ZD	0.805 REF			0.0317 REF		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.4
L	0.40	0.59	0.69	0.016	0.023	0.027
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.0315 BSC		
θ	0°	—	8°	0°	—	8°

**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Description</b>
1.0	2007.05.11	Original
1.1	2008.02.29	1. Add 44-pin TSOPII package 2. Add Avoid timing
1.2	2008.07.04	1. Move Revision History to the last 2. Modify voltage range 2.7V~3.3V to 2.7V~3.6V 3. Add Industrial grade

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