



ECL/TTL/ECL Translator and High-Speed Bus Driver

Features

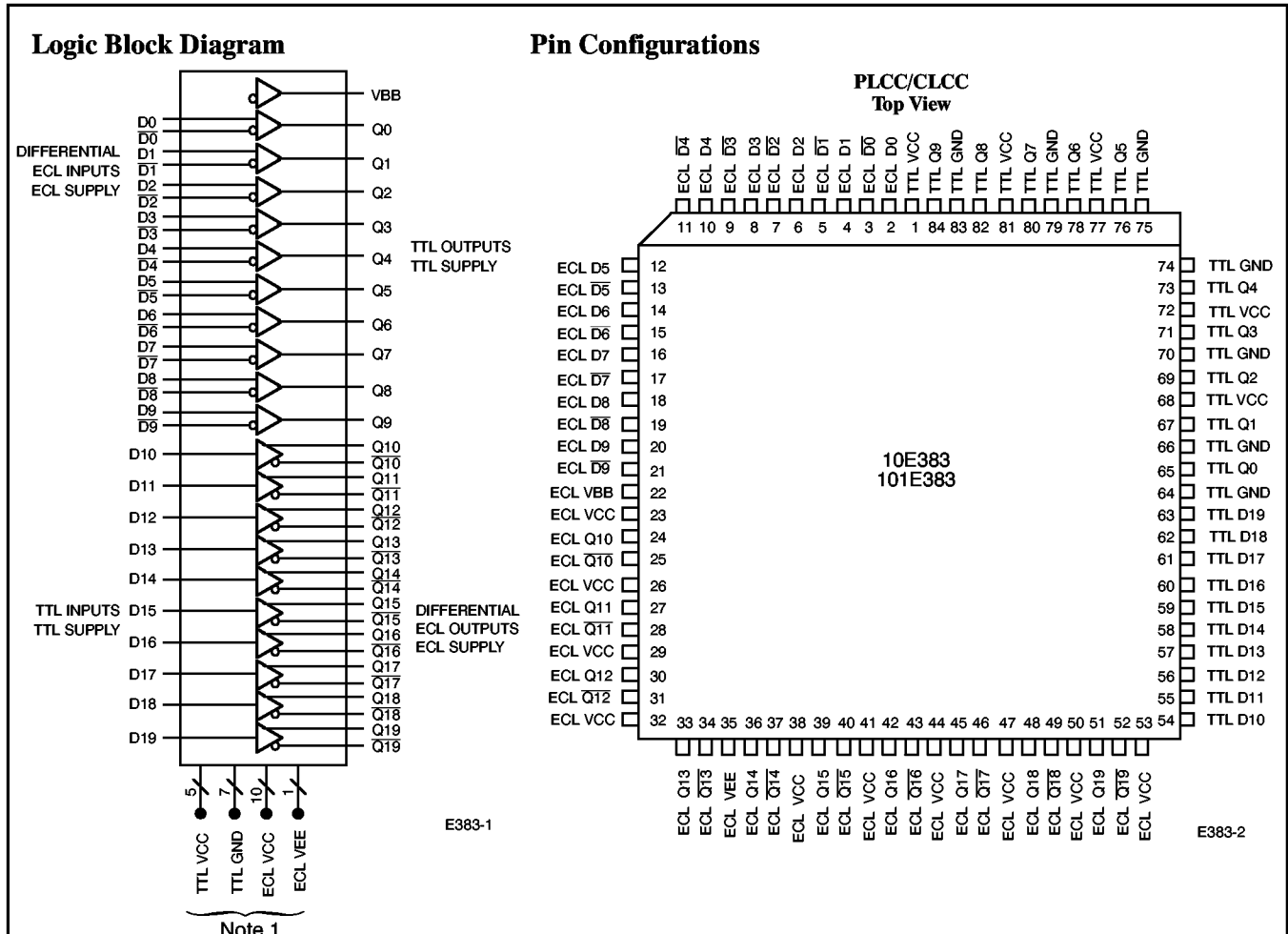
- BiCMOS for optimum speed/power
- High speed (max.)
 - 2.5 ns t_{PD} TTL-to-ECL
 - 3.5 ns t_{PD} ECL-to-TTL
- Low skew $< \pm 1$ ns
- Can operate on single +5V supply
- Full-duplex ECL/TTL data transmission
- Internal 2 k Ω ECL pull-down resistors on each ECL output
- 80-pin PQFP package
- Surface-mount PLCC/CLCC package
- V_{BB} ECL reference voltage output
- Single- or dual-supply operation
- Capable of greater than 2001V ESD
- ECL cable/twisted pair driver

Functional Description

The CY10/101E383 is a new-generation TTL-to-ECL and ECL-to-TTL logic level translator designed for high-performance systems. The device contains ten independent TTL-to-ECL and ten independent ECL-to-TTL translators for high-speed full-duplex data transmission, mixed logic, and bus applications. The CY10/101E383 is especially suited to drive ECL backplanes between TTL boards. The CY10/101E383 is implemented with differential ECL I/O to provide balanced low noise operation over controlled impedance buses between TTL and/or ECL subsystems. In addition, the device has internal output 2 k Ω pull-down resistors tied to V_{EE} to decrease the number of external components. For system testing purposes or for driving light loads, the 2 k Ω is used as the only termination thereby eliminating

up to 20 external resistors. The part meets standard 10K/10KH and 100K logic levels with the internal pull-down while driving 50 Ω to -2V.

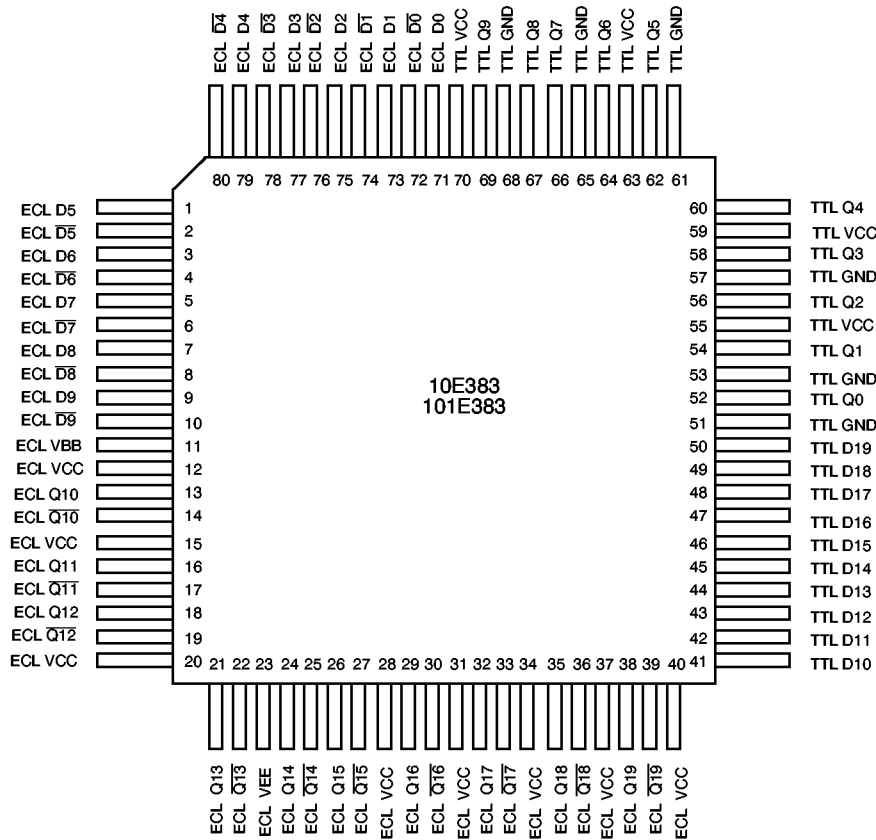
The device is designed with ample ground pins to reduce bounce, and has separate ECL and TTL power/ground pins to reduce noise coupling between logic families. The parts can operate in single- or dual-supply configurations while maintaining absolute 10K/10KH and 100K level swings. The translators are offered in standard 10K/10KH (10E) and 100K (101E) ECL-compatible versions with -5.2V or -4.5V power supply. The TTL I/O is fully TTL compatible. The CY10/101E383 is packaged in 84-pin surface-mountable PLCCs and CLCCs. To save board space, an 80-pin PQFP package with 25-mil-lead pitch is available.





Pin Configurations (continued)

PQFP
Top View



E383-3

Selection Guide

	10E383-2 101E383-2	10E383-3 101E383-3
Maximum Propagation Delay Time (ns) (TTL to ECL)	2.5	3
Maximum Propagation Delay Time (ns) (ECL to TTL)	3.5	4
Maximum Operating Current (mA) Sum of I _{EE} and I _{CC}	270	270

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied -55°C to +125°C
- TTL Supply Voltage to Ground Potential ... -0.5V to +7.0V
- TTL DC Input Voltage -3.0V to +7.0V
- ECL Supply Voltage V_{EE} to ECL V_{CC} -7.0V to +0.5V
- ECL Input Voltage V_{EE} to +0.5V
- ECL Output Current -50 mA
- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-Up Current >200 mA

Operating Range

Range	I/O	Version	Ambient Temperature	ECL V _{EE}	TTL V _{CC}
Commercial	10K 10KH	10E	0°C to +75°C	-5.2V ± 5%	5V ± 5%
Commercial	100K	101E	0°C to +85°C	-4.2V to -5.46V	5V ± 5%
Military	10K 10KH	10E	-55°C to +125°C case	-5.2V ± 5%	5V ± 5%



ECL Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions	Temperature ^[3]	10E383		101E383		Unit
				Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	10E, R _L = 50Ω to -2V V _{IN} = V _{IH} Min. or V _{IL} Max.	T _C = -55°C	-1140	-900			mV
			T _A = 0°C	-1000	-840			mV
			T _A = +25°C	-960	-810			mV
			T _A = +75°C	-900	-735			mV
			T _C = +125°C	-880	-700			mV
		101E, R _L = 50Ω to -2V, V _{IN} = V _{IH} Min. or V _{IL} Max.	T _A = 0°C to 85°C			-1025	-880	mV
V _{OL}	Output LOW Voltage	10E, R _L = 50Ω to -2V V _{IN} = V _{IH} Min. or V _{IL} Max.	T _C = -55°C	-1920	-1670			mV
			T _A = 0°C	-1870	-1665			mV
			T _A = +25°C	-1850	-1650			mV
			T _A = +75°C	-1830	-1625			mV
			T _C = +125°C	-1830	-1610			mV
		101E R _L = 50Ω to -2V, V _{IN} = V _{IH} Min. or V _{IL} Max.	T _A = 0°C to 85°C			-1810	-1620	mV
V _{IH}	Input HIGH Voltage	10E	T _C = -55°C	-1260	-900			mV
			T _A = 0°C	-1170	-840			mV
			T _A = +25°C	-1130	-810			mV
			T _A = +75°C	-1070	-720			mV
			T _C = +125°C	-1030	-700			mV
		101E	T _A = 0°C to 85°C			-1165	-880	mV
V _{IL}	Input LOW Voltage	10E	T _C = -55°C	-1950	-1540			mV
			T _A = 0°C	-1950	-1480			mV
			T _A = +25°C	-1950	-1475			mV
			T _A = +75°C	-1950	-1450			mV
			T _C = +125°C	-1950	-1450			mV
		101E	T _A = 0°C to 85°C			-1810	-1475	mV
V _{BB}	Output Reference Voltage	10E ^[4]	T _A = 0°C to 75°C	-1.37	-1.18			V
			T _C = -55°C	-1.46	-1.32			
			T _C = +125°C	-1.29	-1.14			
		101E ^[4]	T _A = 0°C to 85°C			-1.40	-1.23	
V _{CM} ^[5]	Common Mode Voltage	±V _{CM} with respect to V _{BB}		1.0		1.0	V	
V _{DIFF}	Input Voltage Differential	Required for Full Output Swing		150		150	mV	
I _{IH}	Input HIGH Current	V _{IN} = V _{IH} Max.			220		220	μA
I _{IL}	Input LOW Current	V _{IN} = V _{IL} Min.		-0.5	170	-0.5	170	μA
R _{PD}	Pull-Down Resistor	Connected from All ECL Outputs to V _{EE}	T _A = 0°C to 75°C	1.6	2.4			kΩ
			T _C = -55°C to +125°C	1.6	2.4			
			T _A = 0°C to 85°C			1.6	2.4	
I _{EE}	Supply Current (All inputs and outputs open)				-180		-180	mA

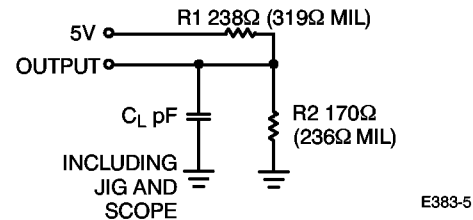
TTL Electrical Characteristics Over the Operating Range^[2]

Parameter	Description	Test Conditions	10E383 101E383		Unit
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -3.2 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Max., I _{OL} = 16.0 mA		0.5	V
V _{IH}	Input HIGH Voltage ^[6]		2.0		V
V _{IL}	Input LOW Voltage ^[5]			0.8	V
V _{CD}	Input Clamp Diode Voltage	I _{IN} = -10 mA	-1.5		V
I _{OS} ^[7]	Output Short-Circuit Current	V _{CC} = Max., V _{OUT} = 0.5V ^[8]	-180	-40	mA
I _{IX}	Input Load Current ^[9]	GND ≤ V _I ≤ V _{CC}	-250	+20	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f max.		90	mA

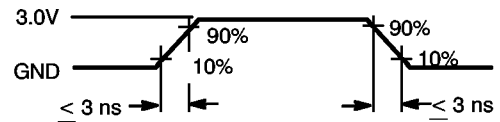
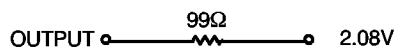
Capacitance^[7]

Parameter	Description	Max.	Unit
C _{IN} ^[7]	Input Capacitance	4	pF
C _{OUT} ^[7]	Output Capacitance	5	pF

TTL AC Test Load and Waveform^[10]

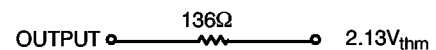


Equivalent to: THÉVENIN EQUIVALENT (Commercial)

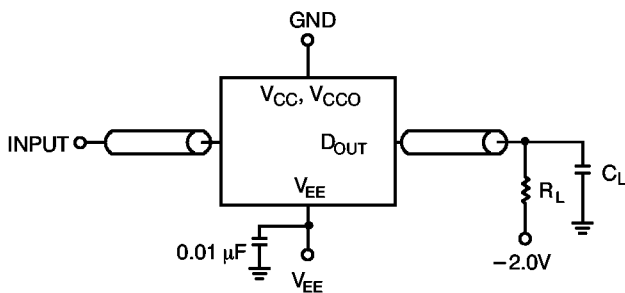


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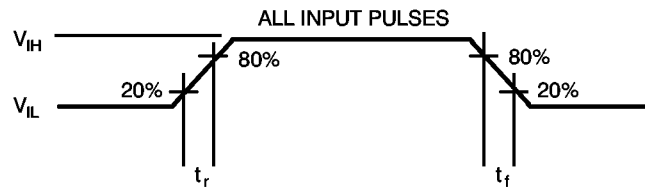
THÉVENIN EQUIVALENT (Military)



ECL AC Test Load and Waveform^[11, 12, 13, 14, 15, 16]



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E383-7

Notes:

- See AC Test Load and Waveform for test conditions.
- Commercial grade is specified as ambient temperature with transverse air flow greater than 500 linear feet per minute. Military grade is specified as case temperature.
- Max. I_{BB} = -1 mA.
- The internal gain of the CY101/10E383 guarantees that the output voltage will not change for common mode signals to ±1V. Therefore, input C_{MRR} is infinite within the common mode range.
- These are absolute values with respect to device ground.
- Characterized initially and after any design or process changes that may affect these parameters.
- Not more than one output should be tested at a time. Duration of the short should not be more than one second.
- I/O pin leakage is the worst case of I_{IX} (where X = H or L).
- TTL test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH}, and C_L = 10 pF.
- V_{IL} = V_{IL} Min., V_{IH} = V_{IH} Max. on 10KH version.
- V_{IL} = -1.7V, V_{IH} = -0.9V on 101E version.
- ECL R_L = 50Ω, C_L < 5 pF (includes fixture and stray capacitance).
- All coaxial cables should be 50Ω with equal lengths. The delay of the coaxial cables should be “nulled” out of the measurement.
- t_r = t_f = 0.7 ns
- All timing measurements are made from the 50% point of all waveforms.



ECL-to-TTL Switching Characteristics Over the Operating Range

Parameter	Description	Test Conditions	10E383-2 101E383-2		10E383-3 101E383-3		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Time	D_n, \overline{D}_n to Q_n	1	3	1	4	ns
t_{PHL}	Propagation Delay Time	D_n, \overline{D}_n to Q_n	1	3	1	4	ns

TTL-to-ECL Switching Characteristics Over the Operating Range

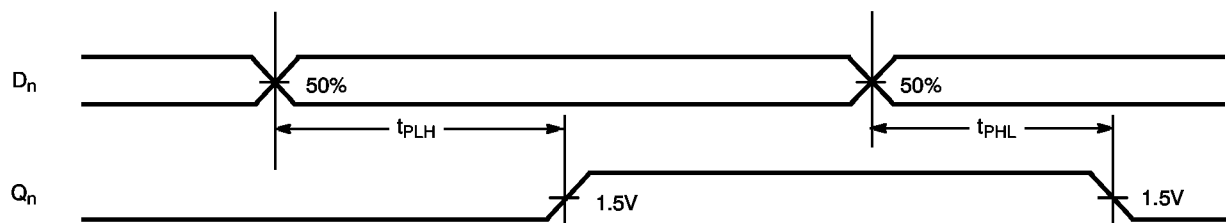
Parameter	Description	Test Conditions	10E383-2 101E383-2		10E383-3 101E383-3		Unit
			Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay Time	D_n to Q_n, \overline{Q}_n	1	2.5	1	3	ns
t_{PHL}	Propagation Delay Time	D_n to Q_n, \overline{Q}_n	1	2.5	1	3	ns
t_R	Output Rise Time	20% to 80%	0.35	1.7	0.35	1.7	ns
t_F	Output Fall Time	20% to 80%	0.35	1.7	0.35	1.7	ns

Skew Time Switching Characteristics^[7] (Same test conditions as TTL-to-ECL and ECL-to-TTL Electrical Characteristics)

Symbol	Characteristic	Test Conditions	Min.	Max.	Unit
$t_{SKT}^{[7]}$	Data Skew Time ECL-to-TTL	$TTLQ_n$ to $TTLQ_{n+m}$		1	ns
$t_{SKE}^{[7]}$	Data Skew Time TTL-to-ECL	$ECLQ_n, \overline{Q}_n$ to $ECLQ_{n+m}, \overline{Q}_{n+m}$		1	ns

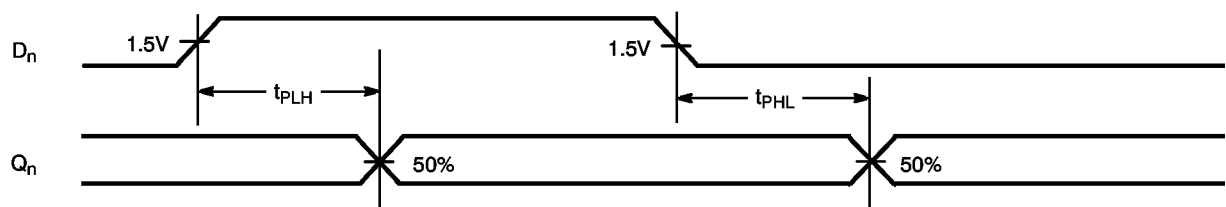
Switching Waveforms

ECL-to-TTL Timing

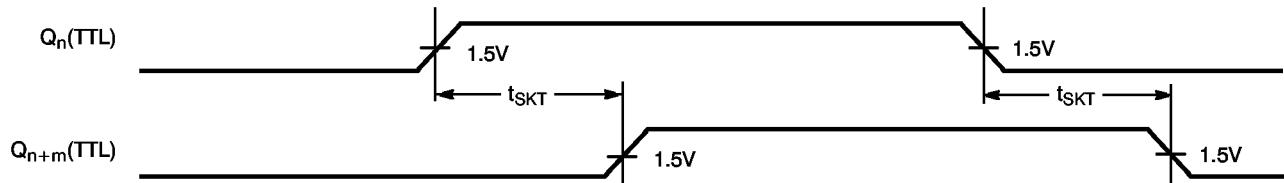


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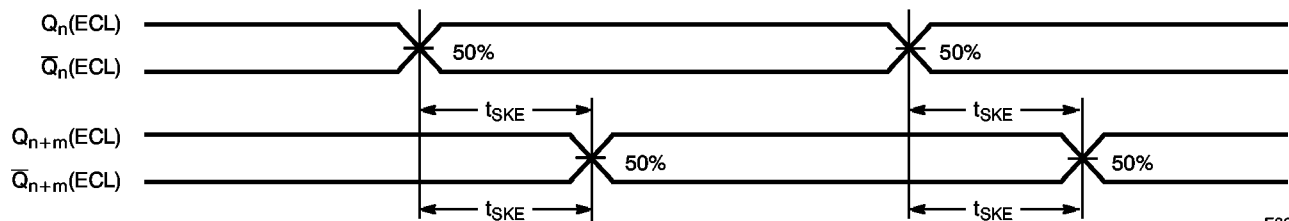
TTL-to-ECL Timing



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Switching Waveforms (continued)
**Skew Test (t_{SKT})
TTL Q_n -to-TTL Q_{n+m}**


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**Skew Test (t_{SKE})
ECL Q_n , \bar{Q}_n -to-ECL Q_{n+m} , \bar{Q}_{n+m}**


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ECL-to-TTL Truth Table

Inputs		Outputs
ECL D_n	ECL \bar{D}_n	TTL Q_n
Open ^[17]	Open ^[17]	L
L	H	L
H	L	H

TTL-to-ECL Truth Table

Inputs	Outputs	
TTL D_n	ECL Q_n	ECL \bar{Q}_n
L	L	H
H	H	L

Nominal Voltages

The CY101/10E383 can be used in dual $\pm 5V$ or single $+5V$ supply systems. The supply pins should be connected as shown in *Tables 1* and *2*. This connection technique involves shifting up all ECL supply pins by $5V$. When operating in single-supply systems, the ECL termination voltage level must also be shifted up by adding $5V$. For example, if the termination is $50\ \Omega$ to $-2V$ in a dual-supply system, the single $+5V$ system should have $50\ \Omega$ to $+3V$. If the termination is a Thévenin type, then the resistor tied to ground is now at $+5V$ and the resistor tied to $-5V$ is now at ground potential. Consideration should be given to the power supply so that adequate bypassing is made to isolate the ECL output switching noise from the supply. Having separate TTL and ECL $+5V$ supply lines will help to reduce the noise. *Table 3* shows the CY10E383 nominal voltages applied in a $10K$ system.

Note:

17. The ECL inputs will pull to a known logic level if left open.

Table 1. CY101E383 Nominal Voltages Applied in 100K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	$+5.0V$	$+5.0V$
TTL GND	$0.0V$	$0.0V$
ECL V_{CC}	$+5.0V$	$0.0V$
ECL V_{EE}	$0.0V$	$-4.5V$

Table 2. CY101E383 Nominal Voltages Applied in 101K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	$+5.0V$	$+5.0V$
TTL GND	$0.0V$	$0.0V$
ECL V_{CC}	$+5.0V$	$0.0V$
ECL V_{EE}	$0.0V$	$-5.2V$

Table 3. CY10E383 Nominal Voltages Applied in 10K System

Supply Pin	Single-Supply System	Dual-Supply System
TTL V_{CC}	$+5.0V$	$+5.0V$
TTL GND	$0.0V$	$0.0V$
ECL V_{CC}	$+5.0V$	$0.0V$
ECL V_{EE}	$0.0V$	$-5.2V$



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
2.5	CY10E383-2JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY10E383-2NC	N80	80-Lead Plastic Quad Flatpack	
3	CY10E383-3JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY10E383-3NC	N80	80-Lead Plastic Quad Flatpack	
	CY10E383-3YMB	Y84	84-Pin Ceramic Leaded Chip Carrier	Military

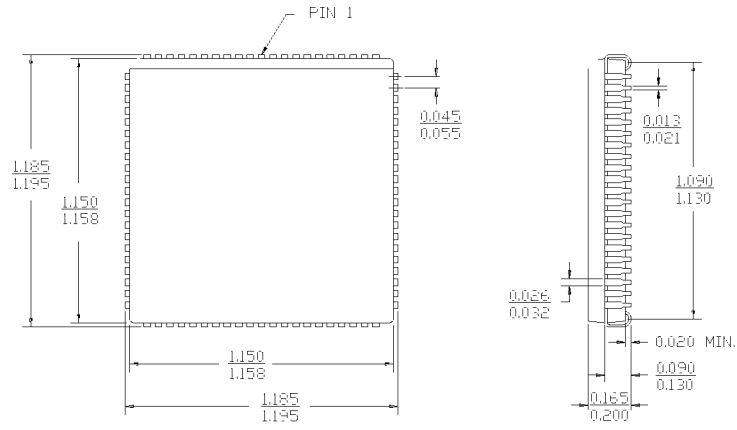
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	CY101E383-2NC	N80	80-Lead Plastic Quad Flatpack	
3	CY101E383-3JC	J83	84-Lead Plastic Leaded Chip Carrier	Commercial
	CY101E383-3NC	N80	80-Lead Plastic Quad Flatpack	

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Package Diagrams

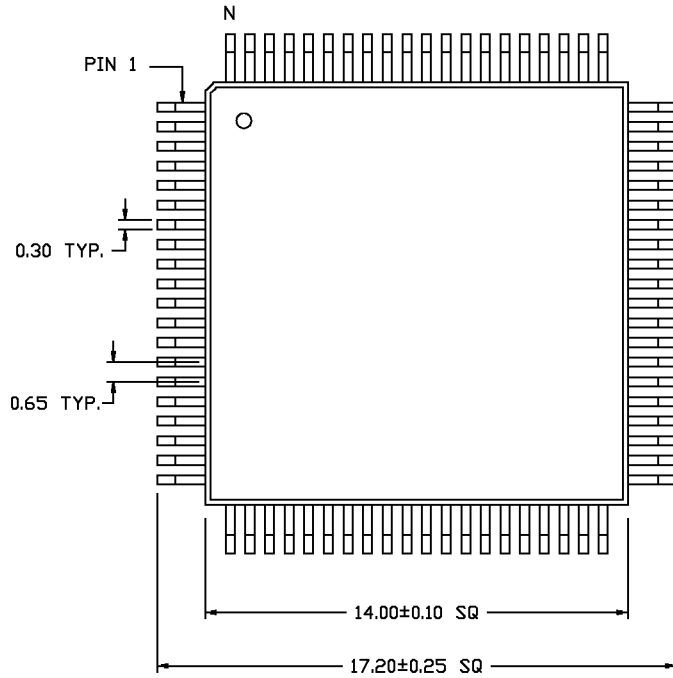
84-Lead Plastic Leaded Chip Carrier J83

DIMENSIONS IN INCHES MIN.
 MAX.

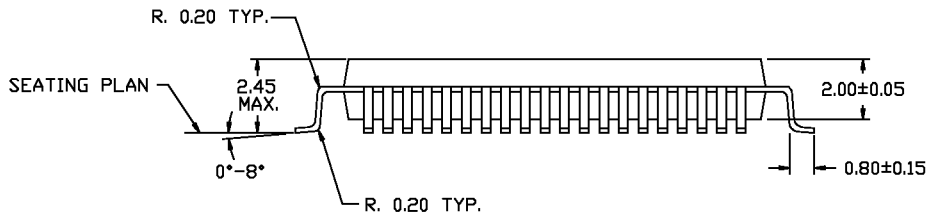


Package Diagrams (continued)

80-Lead Plastic Quad Flatpack N80



DIMENSIONS ARE IN MILLIMETERS
LEAD COPLANARITY 0.102 MAX.



Package Diagrams (continued)
84-Pin Ceramic Leaded Chip Carrier Y84
