GD54/74HC195,GD54/74HCT195

4-BIT PARALLEL-ACCESS SHIFT REGISTER

General Description

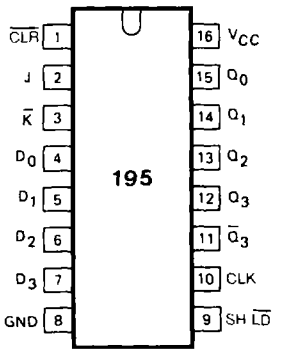
These devices are identical in pinout to the 54/74LS195. This circuit features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. This shift register can operate in two modes:

Parallel (Broadsied) Load

Shift Right (In the direction Q_0 toward Q_3)

Parallel loading is accomplished by applying the four bits of data, and taking the shift/load control input low. Serial shifting occurs synchronously when the shift/load control input is high, where serial data are entered through the J-$\overline{K}$ inputs. These devices are characterized for operation over wide temperature ranges to meet industry and military specifications.

Pin Configuration



Suffix-Blank	Plastic Dual In Line Package
Suffix-J	Ceramic Dual In Line Package
Suffix-D	Small Outline Package

Features

- Low Power consumption characteristic of CMOS devices
- Output drive capability: 10 LS TTL Loads Min.
- Operating speed superior to LS TTL
- Wide operating voltage range: for HC 2 to 6 volts
  for HCT 4.5 to 5.5 volts
- Low input current: 1μA Max.
- Low quiescent current: 80μA Max. (74HC)
- High noise immunity characteristic of CMOS
- Diode protection on all inputs

Function Table

OPERATING MODES	INPUTS						OUTPUTS				
	CLK	$\overline{CLR}$	SH $\overline{LD}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q_3}$
asynchronous reset	L	X	X	X	X	X	L	L	L	L	H
shift, set first stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q_2}$
shift reset first stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q_2}$
shift, toggle first stage	H	↑	h	h	l	X	$\overline{q_0}$	q_0	q_1	q_2	$\overline{q_2}$
shift retain first stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q_2}$
parallel load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d_3}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CLK transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CLK transition
a d = lower case letters indicate the state of the referenced input for output one set-up time prior to the LOW-to-HIGH CLK transition
X = don't care
↑ = LOW-to-Hi · CLK transition

Logic Diagram

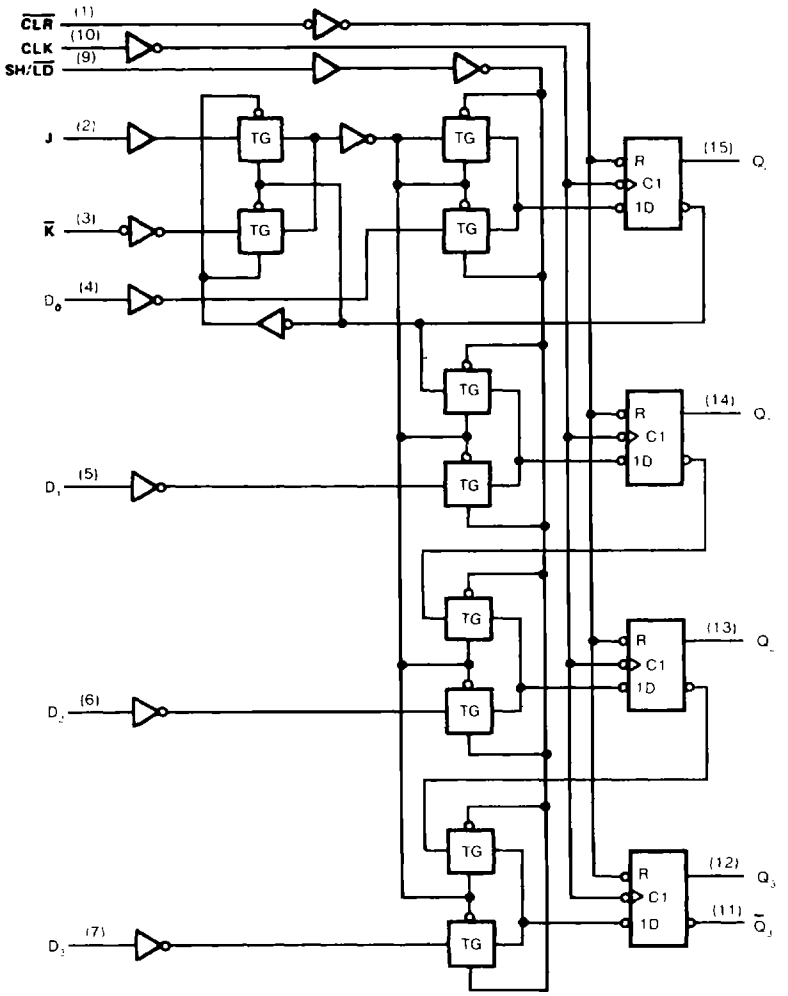


Fig. 1 Logic diagram

Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	DC Supply voltage		−0 5	+7	V
I_{IK} I_{OK}	DC input or output diode current	for V_I<−0 5 or V_I>V_{CC}+0 5V		|20|	mA
I_O	DC output source or sink current	for −0 5V<V_O<V_{CC}+0 5V		|25|	mA
I_{CC}	DC V_{CC} or GND current			50	mA
T_{stg}	Storage temperature range		−65	150	°C
P_D	Power dissipation per package	above +70°C derate linearly with 8mW/K		500	mW
T_L	Lead temperature	At distance 1/16±1/32 in from case for 60 sec(CERAMIC) 10 sec(PLASTIC)		 300 260	°C

Recommended Operating Conditions

CHARACTERISTIC		LIMITS		UNITS
		MIN.	MAX	
Supply-Voltage Range V_{CC}	GD54/74HC Types	2	6	V
	GD54/74HCT Types	4 5	5 5	
DC Input or Output Voltage V_I, V_O		0	V_{CC}	V
Operating Temperature T_A	GD74 Types	−40	+85	°C
	GD54 Types	−55	+125	
Input Rise and Fall times t_r, t_f	GD54/74HC Types at 2V		1000	ns
	at 4 5V		500	
	at 6V		400	
	GD54/74HCT Types at 4 5V		500	

Typical Clear, Shift, and Load Sequences

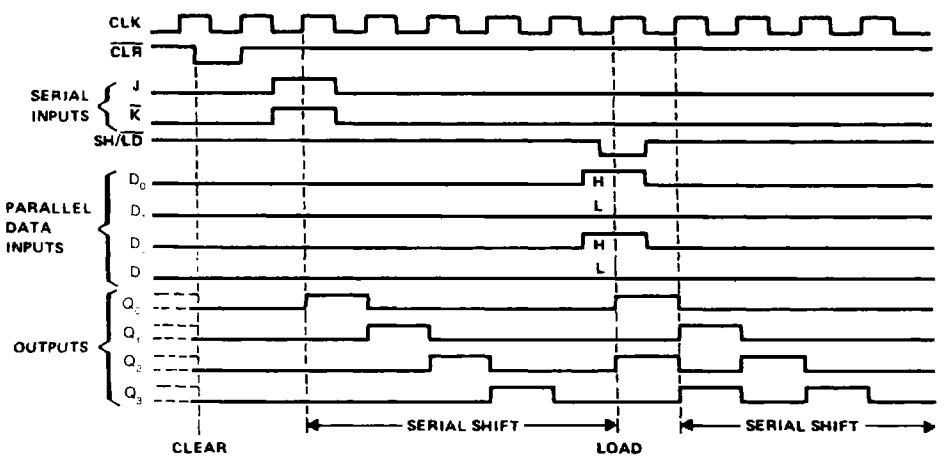


Fig. 2 Typical clear, shift, and load sequences

DC Electrical Characteristics for HC

SYMBOL	PARAMETER	TEST CONDITION		V_{CC}	T_A=25°C			GD74HC195		GD54HC195		UNIT
					MIN	TYP	MAX.	MIN	MAX	MIN	MAX	
V_{IH}	HIGH level input Voltage			2.0 4.5 6.0	1.5 3.15 4.2			1.5 3.15 4.2		1.5 3.15 4.2		V
V_{IL}	LOW level output voltage			2.0 4.5 6.0			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V
			$I_{OH}=-4mA$ $I_{OH}=-5.2mA$	4.5 6.0	3.98 5.48	4.3 5.2		3.84 5.34		3.7 5.2		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	2.0 4.5 6.0			0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
			$I_{OL}=4mA$ $I_{OL}=5.2mA$	4.5 6.0		0.17 0.15	0.26 0.26		0.33 0.33		0.4 0.4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$ or GND		6.0			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		6.0			8		80		160	μA

DC Electrical Characteristics for HCT

SYMBOL	PARAMETER	TEST CONDITION		V_{CC}	T_A=25°C			GD74HCT195		GD54HCT195		UNIT
					MIN.	TYP	MAX.	MIN	MAX	MIN	MAX	
V_{IH}	HIGH level input Voltage			4.5 to 5.5	2.0			2.0		2.0		V
V_{IL}	LOW level output voltage			4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	HIGH level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OH}=-20\mu A$	4.5	4.4	4.5		4.4		4.4		V
			$I_{OH}=-4mA$	4.5	3.98	4.3		3.84		3.7		
V_{OL}	LOW level output voltage	$V_{IN}=V_{IH}$ or V_{IL}	$I_{OL}=20\mu A$	4.5			0.1		0.1		0.1	V
			$I_{OL}=4mA$	4.5		0.17	0.26		0.33		0.4	
$\|I_{IN}\|$	Input leakage Current	$V_{IN}=V_{CC}$or GND		5.5			0.1		1.0		1.0	μA
I_{CC}	Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{out}=0\mu A$		5.5			8		80		160	μA

Timing Requirements for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HC195		GD54HC195		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_w	Pulse width	$\overline{CLR}$ low, CLK	2.0 4.5 6.0	80 16 14			100 20 17		120 24 20		ns
t_{su}	Setup time	SH/$\overline{LD}$, Dn, J, $\overline{K}$	2.0 4.5 6.0	80 16 12			100 20 17		120 24 20		ns
t_{rec}	Recovery time	$\overline{CLR}$ to CLK	2.0 4.5 6.0	80 16 12			100 20 17		120 24 20		ns
t_h	Hold time	SH/$\overline{LD}$, Dn, J, $\overline{K}$ to CLK	2.0 4.5 6.0	0 0 0			0 0 0		0 0 0		ns

AC Characteristics for HC: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HC195		GD54HC195		UNIT
			MIN.	TYP	MAX.	MIN.	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	2.0 4.5 6.0	6 31 36			5 25 29		4.2 21 25		MHz
t_{PLH}/ t_{PHL}	Propagation Delay Time CLK to Qn, $\overline{Q}$n	2.0 4.5 6.0		50 17 13	145 29 25		180 36 31		220 44 36	ns
t_{PLH} t_{PHL}	Propagation Delay Time $\overline{CLR}$ to Qn,$\overline{Q}$n	2.0 4.5 6.0		41 15 12	140 28 24		175 35 30		210 42 35	ns
t_{TLH}· t_{THL}	Output Transition Time	2.0 4.5 6.0		19 7 6	75 15 13		95 19 16		110 22 19	ns

Timing Requirements for HCT: $t_r=t_f=6ns$ $C_L=50$ pF

SYMBOL	PARAMETER		V_{CC} (V)	$T_A=25°C$			GD74HCT195		GD54HCT195		UNIT
				MIN	TYP.	MAX.	MIN	MAX.	MIN	MAX.	
t_w	Pulse width	$\overline{CLR}$ low, CLK	4.5	16			20		24		ns
t_{su}	Setup time	SH/$\overline{LD}$, Dn, J, $\overline{K}$	4.5	16			20		24		ns
t_{rec}	Recovery time	$\overline{CLR}$ to CLK	4.5	16			20		24		ns
t_h	Hold time	SH/$\overline{LD}$, Dn, J, $\overline{K}$ to CLK	4.5	0			0		0		ns

AC Characteristics for HCT: $t_r=t_f=6ns$ CL=50 pF

SYMBOL	PARAMETER	V_{CC} (V)	$T_A=25°C$			GD74HCT195		GD54HCT195		UNIT
			MIN.	TYP.	MAX.	MIN	MAX.	MIN.	MAX.	
f_{max}	Maximum Clock Pulse Frequency	4.5	30			23		20		MHz
t_{PLH}, t_{PHL}	Propagation Delay Time CLK to Qn,$\overline{Q}$n	4 5		19	32		40		48	ns
t_{PLH}, t_{PHL}	Propagation Delay Time $\overline{CLR}$ to Qn,$\overline{Q}$n	4 5		16	31		40		46	ns
t_{TLH} t_{THL}	Output Transition Time	4 5		7	15		19		22	ns

AC Waveforms

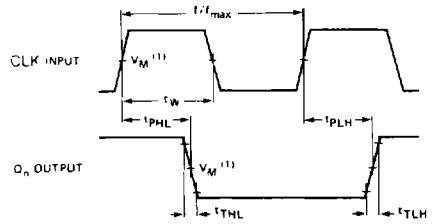


Fig. 3 Waveforms showing the clock (CLK) to output (Q_n) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.

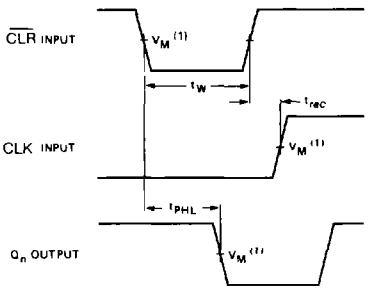


Fig. 4 Waveofrms showing the master clear ($\overline{CLR}$) pulse width, the master clear to output (Q_n) propagation delays and the master clear to clock (CLK) recovery time

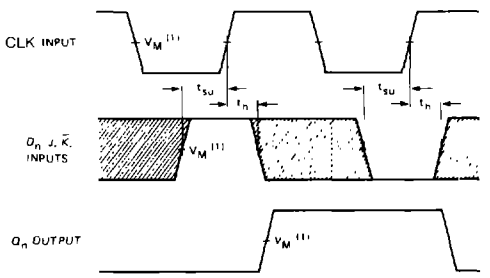


Fig. 5 Waveforms showing the data set-up and hold times for J, $\overline{K}$ and D_n inputs.

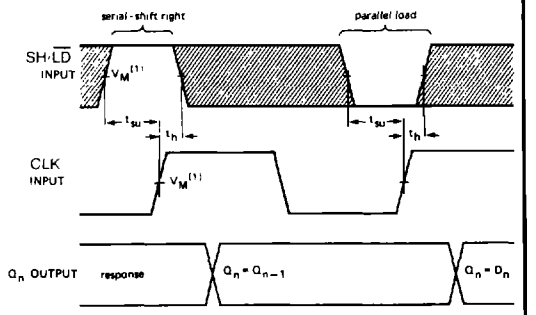


Fig. 6 Waveoforms showing the set-up and hold times from the parallel enable input (SH/$\overline{LD}$) to the clock (CLK).

Note to Figs. 5 and 6
The shaded areas indicate when the input is permitted to change for predictable output performance.

Note to AC waveforms

(1) HC : V_M=50% V =GND to V_{CC}
HCT V_M=1.3V V_I=GND to 3V