Signetics

8X372/8X376
Addressable/Bidirectional I/O Ports

Product Specification

Military
Customer Specific Products

FEATURES
- **Two bidirectional 8-bit busses**
- **Independent bus operation (user-bus priority for data entry)**
- **User data input synchronous (8X372) or asynchronous (8X376) with respect to MCLK**
- **Programmed Microcontroller port address**
- **3-State TTL outputs with high-drive capabilities**
- **Power-up to predetermined logic state**
- **Directly compatible with 8X305**
- **Single +5V supply**
- **0.4", 24-pin Dip**

PRODUCT IDENTITY
8X372 Synchronous 3–State bidirectional I/O port with programmed address

8X376 Asynchronous, 3–State, bidirectional I/O port with programmed address.

PRODUCT DESCRIPTION
Each of these I/O ports is an addressable device designed for use as a bidirectional interface element in systems that use TTL–compatible busses. Typically, these I/O ports are used with the 8X305 Microcontroller and its associated Interface Vector ($\overline{IV}$) bus; however, either port can also be used with the 8X300 Microcontroller or an equivalent microprocessor.

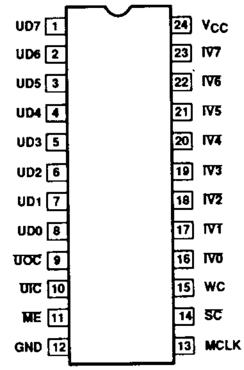
As shown in the logic diagram of Figure 1, each I/O port consists of eight identical data latches — bits 0 through 7. These latches are accessed through either of two 8-bit busses — one connected to the Microcontroller ($\overline{IV}$ bus) and the other to the user system (UD bus). Separate controls are provided for each bus and both busses operate independently, except when both attempt to input data at the same time. In such situations, the user bus always has priority. The data latches are transparent, in that, while either bus is enabled for input, all transitions in input data are propagated to the other bus, if enabled for output.

Both the 8X372 and 8X376 are available with preprogrammed addresses (0_{10} through 255_{10}); either device can be field-programmed over the same address range. Input/output operations can begin once the I/O port is selected and appropriate control signals are generated. Port selection is implemented by putting the I/O port address (0_{10} – 255_{10}) on the $\overline{IV}$ bus; once selected, the I/O port remains selected until a different "port address" is put on the bus. Thus, software overhead is minimized. Data is accessible on the UD bus at all times. A Master Enable ($\overline{ME}$) input, which is typically connected to the Left Bank ($\overline{LB}$) or Right Bank ($\overline{RB}$) output of the Microcontroller, provides the capability of organizing the $\overline{IV}$ bus into two separate and independent banks of I/O devices.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
24–Pin DIP	8X372/BXA 8X376/BXA

PIN CONFIGURATION



PIN NO.	IDENTIFIER	FUNCTION
1–8	UD7–UD0	3–State, bidirectional User Data (UD) bus; UD0 and corresponds to $\overline{IV0}$.
9	$\overline{UOC}$	User Output Control – active low input to enable data output to UD0 – UD7.
10	$\overline{UIC}$	User Input Control – active low input to enable data input from UD0 – UD7.
11	$\overline{ME}$	Master Enable – active low input to enable the $\overline{IV}$ bus for data input, data output; or $\overline{IV}$ address selection/deselection; UD–bus operations are unaffected.
12	GND	Ground.
13	MCLK	Master Clock – active high input (from Microcontroller used to strobe data into data latches from the $\overline{IV}$ bus and, for the synchronous 8X372, from the UD bus; MCLK also synchronizes $\overline{IV}$ address selection.
14	$\overline{SC}$	Select Command – active high input from Microcontroller to enable $\overline{IV}$ address input from the $\overline{IV}$ bus for device selection.
15	WC	Write Command – active high input from Micontroller to enable the writing of data into the data latches from the $\overline{IV}$ bus, provided $\overline{UIC}$ is not low.
16–23	$\overline{IV0}$–$\overline{IV7}$	Interface Vector (Input/Output Bus) – 3–State, bidirectional, Microcontroller data bus; $\overline{IV0}$ corresponds to UD0.
24	V_{CC}	+5V power supply.

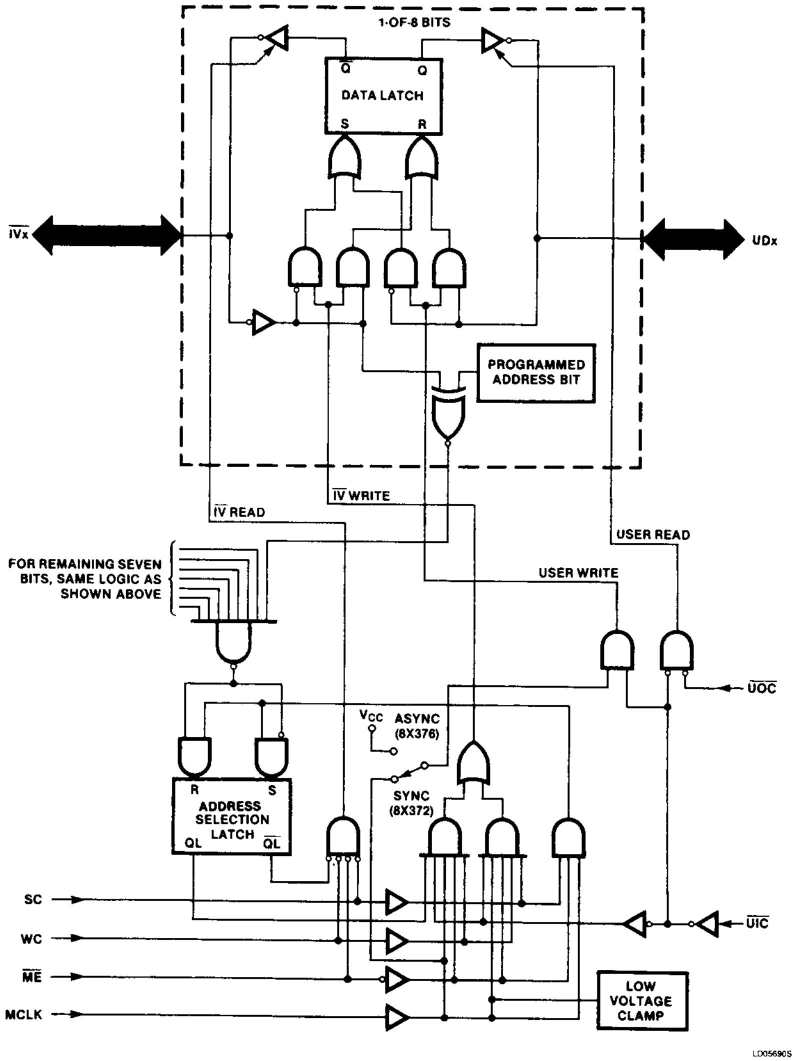


Figure 1. Logic Diagram for 8X372/8X376 I/O Ports

FUNCTIONAL OPERATION

UD Bus Control

As shown in Table 1, the User Data (UD) bus interface is controlled by the $\overline{\text{UIC}}$ and $\overline{\text{UOC}}$ inputs. For the 8X372, data input from the UD bus is written synchronously with MCLK, that is, with $\overline{\text{UIC}}$ low, information is written into the data latches only when MCLK is high. In the case of the 8X376, data input is asynchronous, in that, with $\overline{\text{UIC}}$ low, data is latched in without regard to the level of MCLK. (Note: *To avoid the possibility of processor error when using the asynchronous 8X376, the $\overline{\text{IV}}$ bus should not be read during the time the data latches are changing due to user input.*.) Output drivers on the UD bus are enabled when UOC is low and $\overline{\text{UIC}}$ is high.

$\overline{\text{IV}}$ Bus Control

Input/output control of the $\overline{\text{IV}}$ bus is shown in Table 2; this bus is controlled by SC, WC, $\overline{\text{ME}}$, MCLK and the current state of the internal address selection latch. As shown in Table 2, $\overline{\text{UIC}}$ is required to indicate priority of the UD bus for data input operations. The selection latch in the I/O port stores the result of the most recent $\overline{\text{IV}}$ address selection. The latch is set when the internally preprogrammed address of the port matches the address on the $\overline{\text{IV}}$ bus during an address–selection operation (SC = MCLK = High/WC = Low). The latch is cleared when the two 8–bit address patterns are in disagreement. The $\overline{\text{IV}}$ bus can transfer data only when the selection latch is set. As shown in the APPLICATION DIAGRAM, the Microcontroller Left Bank ($\overline{\text{LB}}$) and Right Bank ($\overline{\text{RB}}$) outputs can control the $\overline{\text{ME}}$ inputs for two banks of I/O devices, thus, acting as a ninth address bit.

Data is written into the data latches of a selected device from the $\overline{\text{IV}}$ bus when WC, MCLK, and $\overline{\text{UIC}}$ are all high and $\overline{\text{ME}}$ is low. To prevent data–input conflicts, inputs from the $\overline{\text{IV}}$ bus are inhibited when $\overline{\text{UIC}}$ is low; under all other conditions, the $\overline{\text{IV}}$ and UD busses operate independently. Output drivers on the $\overline{\text{IV}}$ bus of a selected device are enabled when $\overline{\text{ME}}$, WC, and SC are all low and the address selection latch is set. With SC and WC both high (Shaded entry of Table 2), the bit pattern present on $\overline{\text{IV0}}$ – $\overline{\text{IV7}}$ is interpreted as both input data and $\overline{\text{IV}}$ address. Provided $\overline{\text{UIC}}$ is high, the data is latched into the data latches whether or not the I/O port has been previously selected. If the preprogrammed address of the I/O port matches the bit pattern on $\overline{\text{IV0}}$ = $\overline{\text{IV7}}$ when SC and WC are both high, the selection latch is set; otherwise, it is reset. (Note: *The Microcontroller never drives both SC and WC high at the same time.*)

Table 1. Input/Output Control of UD Bus

$\overline{\text{UIC}}$	$\overline{\text{UOC}}$	MCLK	FUNCTION OF UD BUS	
			8X372	8X376
H	L	X	Output data	Output data
L	X	H	Input data	Input data
L	X	L	Inactive	Input data
H	H	X	Inactive	Inactive

NOTE:
X = Don't care

Table 2. Input/Output Control Of IV Bus

$\overline{\text{ME}}$	SC	WC	MCLK	$\overline{\text{UIC}}$	SELECTION LATCH	FUNCTION $\overline{\text{IV}}$ BUS
L	L	L	X	X	Set	Output Data
L	L	H	H	H	Set	Input Data
L	H	L	H	X	X	Input Address*
L	H	H	H	H	X	Input data and Address*
L	H	H	H	L	X	Input Address*
L	X	H	L	X	X	Inactive
L	H	X	L	X	X	Inactive
L	L	H	H	L	X	Inactive
L	L	X	X	X	Not Set	Inactive
H	X	X	X	X	X	Inactive

NOTE:
X = Don't care
* Selection latch is updated

Bus Logic Levels

Data written into the I/O port from either bus will appear inverted when read from the other bus. Data written into either bus will not be inverted when read from the same bus. (Note: *A logic "1" in Microcontroller software corresponds to a high level on the UD bus even though the $\overline{\text{IV}}$ bus is inverted.*) Both the 8X372 and 8X376 wickiup with the address selection latch in the unselected state and all data bits latched at the "logic 1" level (UD bus outputs high if enabled).

ADDRESS PROGRAMMING AND ADDRESS PROTECT

Programming Procedures

Both 8X372 and 8X376 can be programmed to respond to any address within a range of 0_{10} through 255_{10}. In an unprogrammed state, low level ($\leq$0.8V) inputs on all $\overline{IV}$ bus lines (address 255_{10}) will select the device. To program a given address bit to match a high level ($\geq$ 2.0V) input on the corresponding $\overline{IV}$ pin (a logical "0" to the Microcontroller), the counterpart UD–bus pin must be pulsed according to Table 3 and the following procedures:

Step 1: Set all control inputs to the inactive state— $\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = V_{CC} and SC = WC = MCLK = GND; leave the UD and $\overline{IV}$ bus pins open.

Step 2: Increase V_{CC} to V_{CCP}.

Step 3: After V_{CC} has stabilized, apply a single programming pulse (Figure 2) to the user–bus bit that corresponds to the desired high–level $\overline{IV}$ address bit. The I/O port is programmed from the user bus (UD0 – UD7) for addressing from the Microcontroller bus ($\overline{IV0}$ – $\overline{IV7}$).

Step 4: Return V_{CC} to 0–V. (Note: *If the programming of all address bits is completed in less than 1–second V_{CC} can remain at 90–V for the required interval of time.*)

Step 5: Steps 1 through 3 are applicable to the programming of each address bit that requires a high–level $\overline{IV}$ match.

Step 6: To verify that the address is properly programmed, return V_{CC} to +5V, set $\overline{IV0}$ – $\overline{IV7}$ to the desired (inverted) binary address pattern, set $\overline{ME}$ = WC = Low and SC = MCLK = High. If there are no programming errors, subsequent data written from $\overline{IV0}$ – $\overline{IV7}$ (WC = High) will appear inverted on UD0 – UD7.

Address Protect

After programming the I/O Port, steps should be taken to isolate the address circuits and make these circuits permanently immune to further change.

Step 1: Set V_{CC} and all control inputs to 0V V_{CC} = $\overline{UIC}$ = $\overline{UOC}$ = $\overline{ME}$ = SC = WC = MCLK = 0V; $\overline{IV0}$ – $\overline{IV7}$ = open circuit.

Step 2: Taking one pin at a time, apply a protect programming pulse (Figure 3) to each user–bus bit (UD0 – UD7) — refer to Table 3 for Min/Max specifications pertaining to voltage and current.

Step 3: Verify that the address circuits for each bit is isolated by applying 9V, in turn, to each user–bus pin (UD0 – UD7) and measuring less than 200 microamperes of input current. (Note: *Setup conditions are the same as those in Step 1.*)

Table 3. Programming Specification

PARAMETERS	LIMITS Min	Typ	Max	UNITS
V_{CCP} — Programming supply voltage: Address	8.75	9.0	9.25	V
Protect		0		V
Maximum time V_{CCP} > 5.25V			1.0	Sec
Programming voltage: Address	8.75	9.0	9.25	V
Protect	8.75		9.25	V
Programming current: Address			5	mA
Protect			50	mA
t_r — Programming pulse rise time: Address	10		100	µS
Protect	10		100	µS
$t\omega$ — Programming pulse width	0.5		1.0	mS

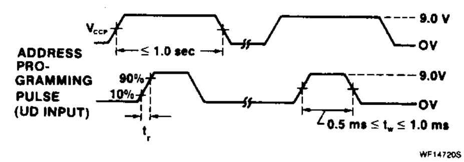


Figure 2. Address Programming Pulse

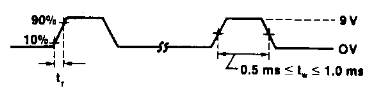


Figure 3. Protect Programming Pulse

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage[3]	+7	V_{DC}
V_I	Input voltage[3]	+5.5	V_{DC}
T_{STG}	Storage temperature range	–65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $4.5V \leq V_{CC} \leq 5.5V, -55°C \leq T_C \leq +125°C$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
V_{IK}	Input clamp voltage	V_{CC} = Min; I_I = –10mA			–1.5	V
I_{IH}	High level input current[1]	V_{CC} = Max; V_{IH} = 2.7V			100	µA
I_{IL}	Low level input current[1]	V_{CC} = Max; V_{II} = 0.5V			–550	µA
V_{OL}	Low level output voltage $\overline{IV}$ Bus ($\overline{IV0}$ – $\overline{IV7}$)	V_{CC} = Min; I_{OL} = 16mA			0.55	V
	User Bus (UD0 – UD7)	V_{CC} = Min; I_{OL} = 24mA			0.55	V
V_{OH}	High level output voltage	V_{CC} = Min; I_{OH} = –3.2mA	2.4			V
I_{OS}	Short circuit output current[2] $\overline{IV}$ bus ($\overline{IV0}$ – $\overline{IV7}$)	V_{CC} = Max	–20			mA
	UD bus (UD0 – UD7)	V_{CC} = Max	–10			mA
I_{CC}	Supply current	V_{CC} = Max; $\overline{ME}$, $\overline{UOC} \geq 4.0V$			150	mA

NOTES:
1. The input current includes the 3–State leakage current of the output driver on the data lines.
2. Only one output may be shorted at a time.
3. These limits do not apply during address programming.

AC ELECTRICAL CHARACTERISTICS $4.5V \le V_{CC} \le 5.5V$, $-55^{\circ}C \le T_C \le +125^{\circ}C$

SYMBOL	PARAMETER	REFERENCES From	REFERENCES To	TEST CONDITIONS	LIMITS Min	LIMITS Typ	LIMITS Max	UNIT
Pulse Widths:								
t_{W1}	Clock high	↑MCLK	↓MCLK		30			ns
t_{W2}	User input control	↓$\overline{\text{UIC}}$	↑$\overline{\text{UIC}}$	MCLK = High	35			ns
Propagation Delays:								
t_{PD1}	UD propagation delay	UD	IV	MCLK = High SC = WC = $\overline{\text{ME}}$ = $\overline{\text{UIC}}$ = Low			45	ns
t_{PD2}	UD clock delay (8X732 only)	↑MCLK	IV	UD = Stable; SC = WC = $\overline{\text{ME}}$ = $\overline{\text{UIC}}$ = Low			55	ns
t_{PD3}	UD input delay	↓$\overline{\text{UIC}}$	IV	UD = Stable; MCLK = High; SC = WC = $\overline{\text{ME}}$ = Low			55	ns
t_{PD4}	IV data propagation delay	IV	UD	MCLK = WC = $\overline{\text{UIC}}$ = High $\overline{\text{ME}}$ = $\overline{\text{UOC}}$ = SC = Low			45	ns
t_{PD5}	IV data clock delay	↑MCLK	UD	WC = $\overline{\text{UIC}}$ = High; IV = Stable; $\overline{\text{ME}}$ = $\overline{\text{UOC}}$ = SC = Low			55	ns
Output Enable Timing:								
t_{OE1}	UD output enable	↓UOC	UD	$\overline{\text{UIC}}$ = High			45	ns
t_{OE2}	UD input recovery	↑$\overline{\text{UIC}}$	UD	$\overline{\text{UOC}}$ = Low			45	ns
t_{OE3}	IV data master enable	↓$\overline{\text{ME}}$	IV	WC = SC = Low			45	ns
t_{OE4}	IV data write recovery	↓WC	IV	SC = $\overline{\text{ME}}$ = Low			45	ns
t_{OE5}	IV data select recovery	↓SC	IV	SC = $\overline{\text{ME}}$ = Low			45	ns
Output Disable Timing:								
t_{OD1}	UD output disable	↑$\overline{\text{UOC}}$	UD	$\overline{\text{UIC}}$ = High			40	ns
t_{OD2}	UD input override	↓$\overline{\text{WC}}$	UD	$\overline{\text{UOC}}$ = Low — 8X372			45	ns
				8X376			55	
t_{OD3}[2]	IV data master disable	↑$\overline{\text{ME}}$	IV	WC = SC = Low			40	ns
t_{OD4}[2]	IV data write override	↑WC	IV	SC = $\overline{\text{ME}}$ = Low			40	ns
t_{OD5}[2]	IV data select override	↑SC	IV	WC = $\overline{\text{ME}}$ = Low			40	ns
Setup Times:								
t_{S1}	UD clock setup time (8X372 only)	UD	↓MCLK	$\overline{\text{UIC}}$ = Low	15			ns
t_{S2}	UD control setup time	UD	↑$\overline{\text{UIC}}$	MCLK = High	25			ns
t_{S3}	User input control setup time (8X372 only)	↓$\overline{\text{UIC}}$	↓MCLK		25			ns
t_{S4}	IV data setup time	IV	↓MCLK	WC = High or SC = High; $\overline{\text{ME}}$ = Low; $\overline{\text{UIC}}$ = High	15			ns
t_{S5}[3]	IV master enable setup time	↓ME	↓MCLK	WC = High or SC = High; $\overline{\text{UIC}}$ = High	21			ns
t_{S6}	IV write control setup time	↑WC	↓MCLK	SC = $\overline{\text{ME}}$ = Low; $\overline{\text{UIC}}$ = High	40			ns
t_{S7}	IV select control setup time	↑SC	↓MCLK	WC = $\overline{\text{ME}}$ = Low	30			ns

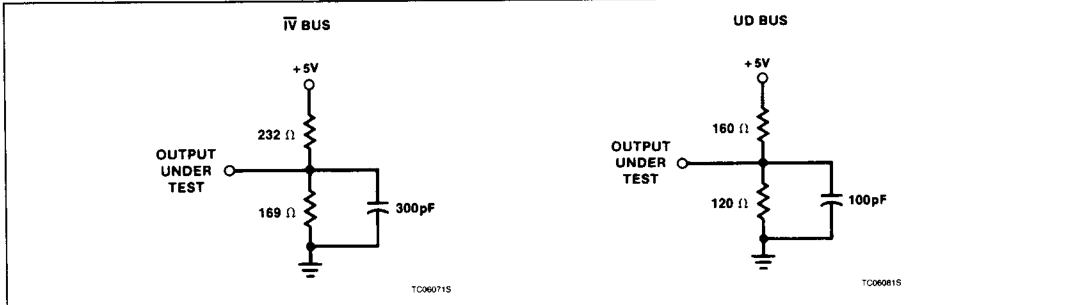
AC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	REFERENCES		TEST CONDITIONS		LIMITS			UNIT
		From	To			Min	Typ	Max	
Hold Times:									
t_{H1}	UD clock hold time (8X372 only)	↓MCLK	UD	$\overline{UIC}$ = Low		20			ns
t_{H2}	UD control hold time	↑$\overline{UIC}$	UD	MCLK = High		10			ns
t_{H3}	User input control hold time (8X372 only)	↓MCLK	↑$\overline{UIC}$			0			ns
t_{H4}	$\overline{IV}$ data hold time	↓MCLK	$\overline{IV}$	WC = High or SC = High;	25°C	5			ns
				$\overline{ME}$ = Low, $\overline{UIC}$ = High	Temp	20			
t_{H5}[3]	$\overline{IV}$ master enable hold time	↓MCLK	↑$\overline{ME}$	WC = High or SC = High; $\overline{UIC}$ = High		0			ns
t_{H6}	$\overline{IV}$ write control hold time	↓MCLK	↓WC	SC = $\overline{ME}$ = Low; $\overline{UIC}$ = High		0			ns
t_{H7}	$\overline{IV}$ select control	↓MCLK	↓SC	WC = $\overline{ME}$ = Low		0			ns

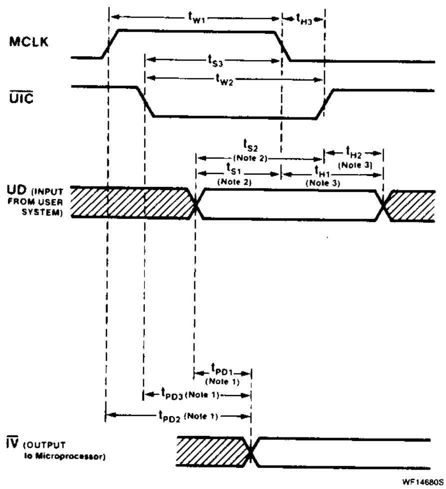
NOTES:

1. All measurements to the $\overline{IV}$ bus assumes the address selection latch is set.
2. These parameters are measured with a capacitive loading of 50pf and represent the output drive turn–off time.
3. If $\overline{ME}$ is to be high (inactive) it must be setup before the rising edge and held after the falling edge of MCLK to avoid unintended writing into or selection of the I/O port.

AC TEST LOADING CIRCUITS



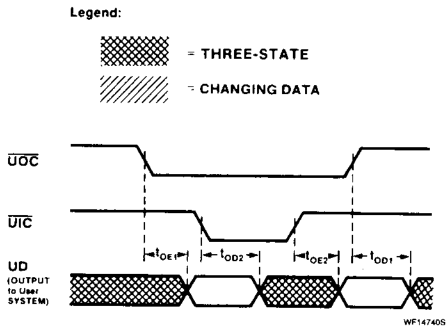
TIMING DIAGRAMS



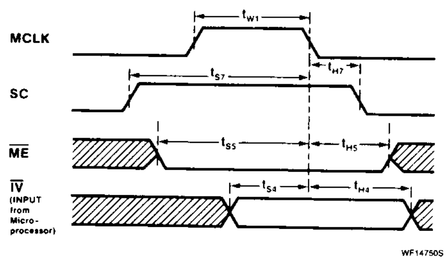
STATIC CONDITIONS:
SC WC $\overline{ME}$ Low
$\overline{UOC}$ High

NOTES:
1. The actual time for stable data on the $\overline{IV}$ bus is the latest propagation from t_{PD1}, t_{PD2} and t_{PD3}.
2. The UD input must satisfy the setup-time requirements for both t_{S1} and t_{S2}.
3. Minimum hold-time required for the UD input is the earlier of the times specified by t_{H1} and t_{H2}.

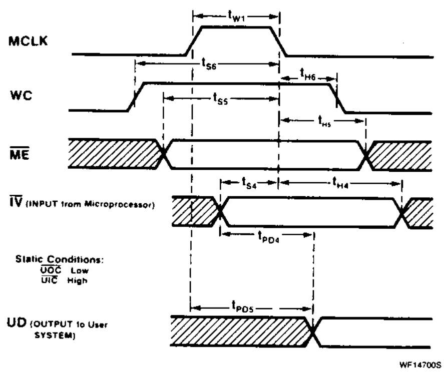
a. User Data Input Timing



b. User Data Output Enable

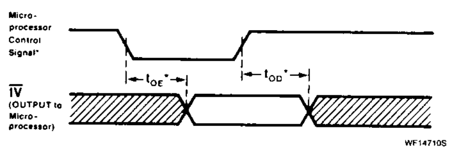


d. Microcontroller Select Cycle Timing



STATIC CONDITIONS:
$\overline{UOC}$ Low
$\overline{UIC}$ High

c. Microcontroller Write Cycle Timing



*PARAMETER KEY

MICROPROCESSOR CONTROL SIGNAL	AC TIMING PARAMETERS	STATIC CONDITIONS
$\overline{ME}$	t_{OE3} t_{OD3}	SC = WC = LOW
WC	t_{OE4} t_{OD4}	SC = $\overline{ME}$ = LOW
SC	t_{OE5} t_{OD5}	WC = $\overline{ME}$ = LOW

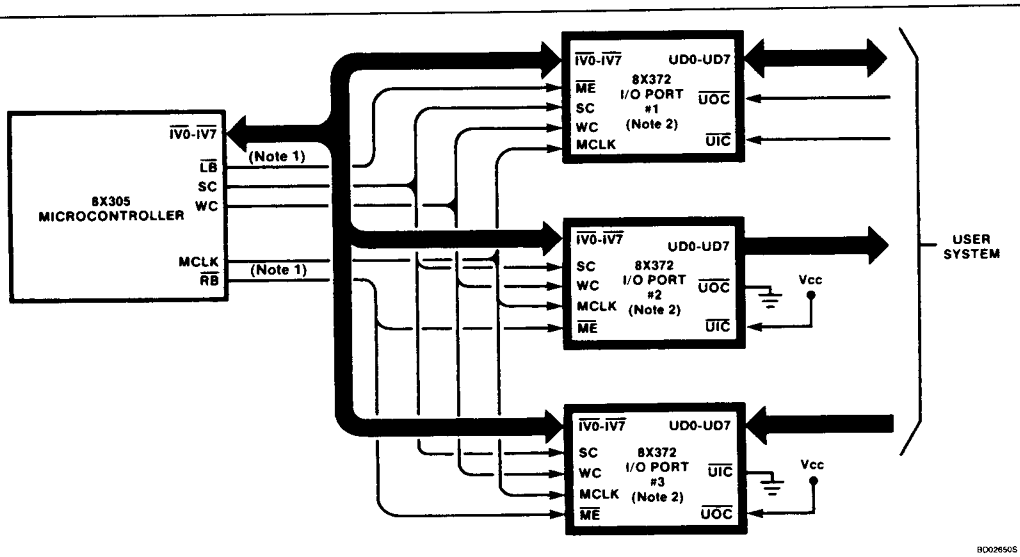
e. Microcontroller Output Enable Timing

Addressable/Bidirectional I/O Ports

8X372/8X376

APPLICATIONS

One way of using I/O Ports in a microprocessor–based system is shown in the following application diagram; there are many other ways of implementing I/O functions with these parts, both singularly and in combination. By proper control the $\overline{UIC}$ and $\overline{UOC}$ lines, the user can implement bidirectional data transfers, exercise system control, and/or read system status. In the concept shown here, I/O Port #1 is setup for bidirectional data transfers and I/O Ports #2 and #3, respectively, serve as dedicated output and input devices.



NOTES:

1. Up to 256 discrete addresses can be assigned to each bank ($\overline{LB}$ or $\overline{RB}$).
2. The 8X376 can be implemented in an identical manner.

Signetics

Packaging Information

T-90-20

Military Products

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

U: Leadless chip carriers
X: Dual-in-line packages
Y: Flat packages
Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

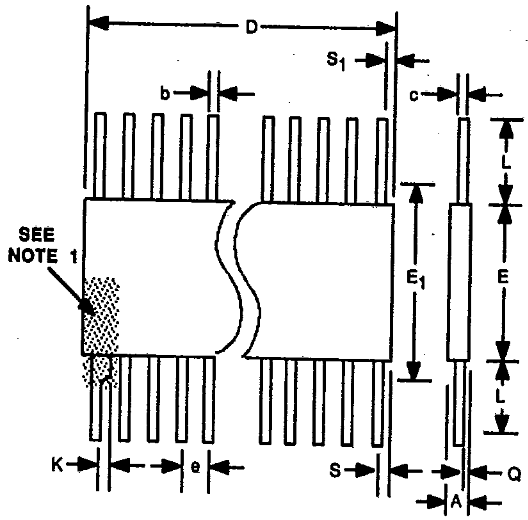
Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

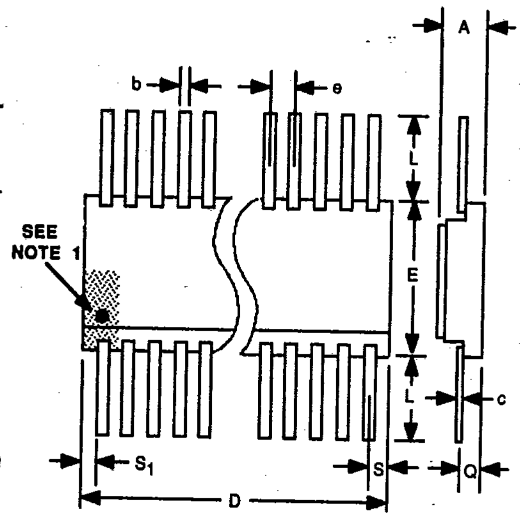
T-90-20

Packaging Information

CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1



Configuration 2

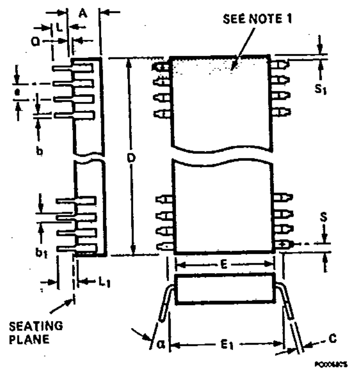
NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ± 0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

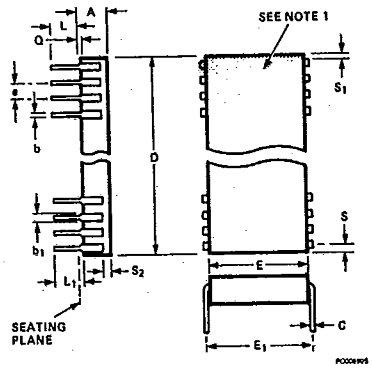
OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	- -	1.330	2
E	0.620	0.660	
e	0.050 BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	-	0.045	5
S1	0.005	-	5

Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1

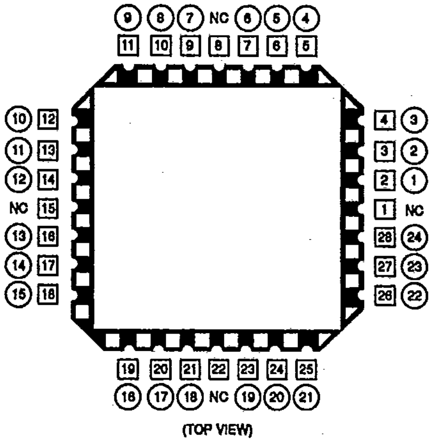


Configuration 2

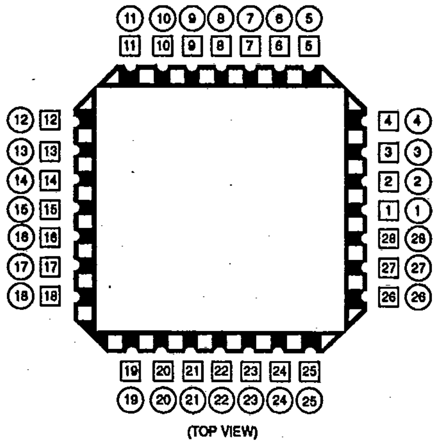
1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

Packaging Information

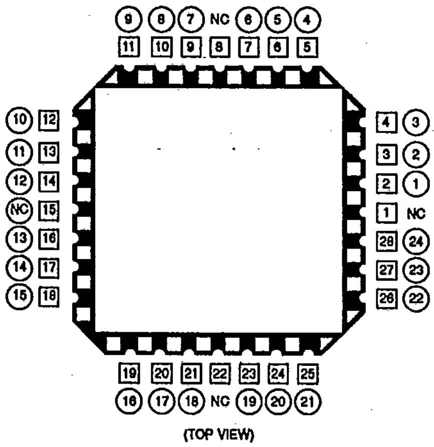
LEADLESS CHIP CARRIER (LLCC) PINOUTS



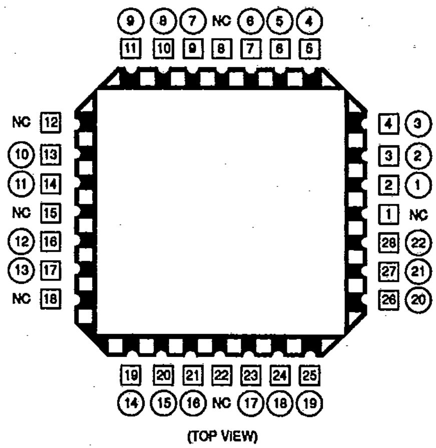
24–Lead Logic Pinout for 28 Terminal Chip Carrier



28–Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24–Lead Memory Pinout for 28 Terminal Chip Carrier



22–Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect