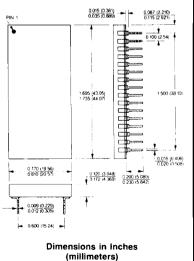
## **FEATURES**

- Complete DAS Front End: 2 8-Channel Multiplexers Instrumentation Amp Track-Hold Amp
- Small 32-Pin DIP
- 12-Bit Linearity
- 16 Single-Ended or 8 Differential Input Channels
- 10usec Maximum Acquisition Time to ±0.01% (20V Step)
- Low Droop Rate +7µV/µsec Maximum
- Full Mil Operation -55°C to +125°C
- MIL-H-38534 Screening Optional, MIL-STD-1772 **Qualified Facility**

### 32 PIN DIP



### DESCRIPTION

MN7130 is a thin-film hybrid circuit containing two 8-channel multiplexers, a true instrumentation amplifier and a track-hold amplifier. This unique circuit is extremely versatile and can be used in conjunction with any of Micro Networks analog-to-digital converters to configure a complete, 16-channel (8 full differential) data acquisition system in as few as 2 dual-in-line packages occupying as little as 4 square inches of board space. Additionally, MN7130 can be used in any analog system for applications requiring the analog acquisition of multiple channels.

MN7130 has a maximum acquisition time of  $10\mu$ sec (20V step to ±0.01%FSR) when the multiplexer, instrumentation amplifier and track-hold are serially connected, and a typical droop rate of +4µV/usec. The internal multiplexer may be connected for single-ended or 8 full differential input channels and is directly addressable in binary. The digital inputs are CMOS compatible. and analog inputs up to ±10V can be accommodated. For additional flexibility, all inputs and outputs of the internal subsections are available at the device pins. The standard device is ful-Iv specified for either 0°C to +70°C or -55°C to +125°C (H model) operation. The MN7130H/B is available with Environmental Stress Screening while the MN7130H/B CH is fully screened in accordance with MIL-H-38534.

MN7130 was specifically designed to fill the need for a small. low-cost data acquisition system that was physically and electrically compatible with current microprocessor technology. When used with a 12-bit A/D, the approach eliminates the need for special mountings and connectors, saves space, facilitates maintenance, and reduces costs. In addition, MN7130 allows standard board spacing, improves reliability and offers significant weight savings in aerospace and avionics applications.



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# MN7130 MULTIPLEXED TRACK-HOLD AMPLIFIER

#### **ABSOLUTE MAXIMUM RATINGS**

T/H Amplifier Output (Pin 18)

Operating Temperature Range
Specified Temperature Range:
MN7130
MN7130H, H/B
Storage Temperature Range
Positive Supply (+ V<sub>CC</sub>, Pin 24)
Negative Supply (- V<sub>CC</sub>, Pin 23)
Multiplexer Inputs (Pins 1-16)
Instrumentation Amp Inputs (Pins 21, 22)
T/H Amplifier Input (Pin 19)
Address Inputs (Pins 27-31)
T/H Command (Pin 17)
Multiplexer Outputs (Pins 26, 32)
Instrumentation Amp Output (Pin 20)

-55°C to +125°C

0°C to +70°C

-55°C to +125°C

-65°C to +150°C

0 to +16 Volts

0 to -16 Volts

- Vcc to + Vcc

±15 Volts

0 to ± Vcc Volts

-0.3 to + Vcc Volts

±25mA

S.C. Protected to Ground

#### ORDERING INFORMATION

PART NUMBER	H/B C
Standard part is specified for	111
0°C to +70°C operation.	IIII
Add "H" for specified -55°C to +125°C	111
operation.	וונ
Add "/B" to "H" models for	- [ ]
Environmental Stress Screening.	<b>-</b>
Add "CH" to "B" models for 100%	- 1
screening according to MIL-H-38534.	

#### SYSTEM SPECIFICATIONS (TA = +25°C, ±Vcc = ±15V, unless otherwise indicated) (Note 1)

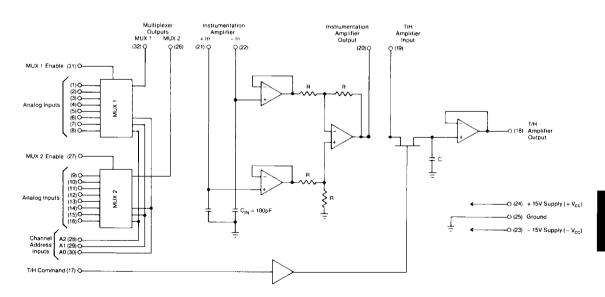
ANALOG INPUT (Multiplexer Inputs)	MIN.	TYP.	MAX.	UNITS
Voltage Range: Single-Ended Differential Common Mode	± 10	± 10 ± 10 ± 12		Volts Volts Volts
Input Impedance		250//100		MΩ//pF
Input Current		± 15	± 30	nA
Common Mode Rejection Ratio	70	80		dB
DIGITAL INPUTS (Mux Address, T/H Command)				
Logic Levels: Mux Address: Logic "1" Logic "0" T/H Command: Logic "1" Logic "0"	+4.0 +2.4		+ 0.8	Volts Volts Volts Volts
Logic Currents: Mux Address (Note 2):		±10 ±10 ±10 ±10		μΑ μΑ μΑ μΑ
ANALOG OUTPUT (T/H Amplifier)				
Output Voltage	± 10			Volts
Output Current	± 2			mA
Output Load Capacitance			50	pF
TRANSFER CHARACTERISTICS				
Gain		+1		V/V
Gain Error (Note 3): Initial ( + 25 °C) Over Temperature (Note 4)		± 0.1 ± 0.1	± 0.2	% %
Gain Linearity Error (Note 5)		±0.002		%FSR
Offset Voltage (Track Mode): Initial (+25°C) Over Temperature (Note 4)		±2 ±4	± 6	mV mV
Offset Change (Pedestal, Hold Mode) Over Temperature (Note 4)		± 15		mV
Droop Rate: +25°C 0°C to +70°C -55°C to +125°C		±4	±7 ±10 ±40	μV/μsec μV/μsec μV/μsec

DYNAMIC CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS
Large Signal Bandwidth		250		kHz
Output Slew Rate		± 20		V/µsec
Acquisition Time (20V step to ± 0.01%)		6.5	10	μSec
Aperture Delay		200	400	nsec
Settling Time, Track-to-Hold to ± 1.0mV		0.5	2	μsec
Feedthrough (Hold Mode) @ 1kHz		± 0.01		%
Transients Peak Amplitude: Track-to-Hold Hold-to-Track		90 100		mV mV
POWER SUPPLIES		1	† · · · · · · · · · · · · · · · · · · ·	
Power Supply Range: + 15V Supply - 15V Supply	+ 14.55 - 14.55	+ 15 - 15	+ 15.45 - 15.45	Volts Volts
Current Drains: + 15V Supply - 15V Supply		+ 30 - 30	+ 40 - 40	mA mA
Power Consumption		900	1200	mW

#### SPECIFICATION NOTES:

- System specifications listed reflect system performance with all elements serially connected.
- If the multiplexer inputs are to be driven from standard TTL logic, 1kΩ pullup resistors to +5V should be connected.
- Gain error is defined as the error in the slope of the systems input-output transfer function and is expressed in percent.
- MN7130 is specified for 0°C to +70°C operation. MN7130H and MN7130H/B are specified for ~55°C to +125°C operation.
- Gain linearity error is defined as the maximum deviation from the best-fit straight line approximation to the system's input-output transfer function and is expressed as a percentage of the system's full scale voltage swing (FSR).

# **BLOCK DIAGRAM**



## **PIN DESIGNATIONS**



1	Channel 0	32	Mux 1 Output
2	Channel 1	31	Mux 1 Enable
3	Channel 2	30	A <sub>0</sub> Mux Address
4	Channel 3	29	A <sub>1</sub> Mux Address
5	Channel 4	28	A <sub>2</sub> Mux Address
6	Channel 5	27	Mux 2 Enable
7	Channel 6	26	Mux 2 Output
8	Channel 7	25	Ground
9	Channel 8	24	+ 15V Supply ( + Vcc)
10	Channel 9	23	– 15V Supply ( – V <sub>cc</sub> )
11	Channel 10	22	<ul> <li>In (Instrumentation Amplifier)</li> </ul>
12	Channel 11	21	+ In (Instrumentation Amplifier)
13	Channel 12	20	Instrumentation Amplifier Output
14	Channel 13	19	T/H Amplifier Input
15	Channel 14	18	T/H Amplifier Output
16	Channel 15	17	T/H Command

### APPLICATIONS INFORMATION

**DESCRIPTION OF OPERATION**—MN7130 is a complete data acquisition system front end containing user-configurable components (multiplexers, instrumentation amplifier and track-hold amplifier).

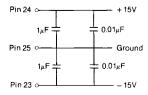
In order to preserve maximum flexibility, all inputs and outputs of the subsections are available at the device pins. The internal 8-channel multiplexers can be connected for 16 single-ended or 8 fully differential input operation and may be directly addressed via three address lines and two mux enable lines. The internal instrumentation amplifier offers high input impedance (250M $\Omega$ /100pF) and 70dB common mode rejection ratio. The internal track-hold amplifier completes this analog front-end function allowing dynamic input signals to be acquired and then held for analog-to-digital conversion.

MN7130 can be used in conjunction with MN574A  $\mu P\text{-}compatible 12\text{-}bit A/D converters to configure a complete and inexpensive, 16-channel, 12-bit <math display="inline">\mu P\text{-}compatible DAS$  capable of 28,000 channels/sec throughput rates in a minimum of board space. Substituting MN5240 for MN574A increases throughput to 60,000 channels/sec.

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified performance from the MN7130. The unit's ground pin (pin 25) should be tied to system analog ground as close to the unit as possible, preferably through a large analog ground plane underneath the package.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground.  $1_\mu F$  tantalum capacitors in parallel with  $0.01_\mu F$  ceramic capacitors are the most effective combination. Single  $1_\mu F$  ceramic capacitors can be used if necessary to save board space.



MULTIPLEXER-INSTRUMENTATION AMPLIFIER—The multiplexer section of the MN7130 is addressed with a three or four bit binary word and can be configured for 8 full differential inputs or 16 single-ended inputs. The use of differential inputs provides high rejection of common mode noise and elimination of ground return offsets. Differential inputs must be used when both sides of the input signal are off ground. Connections and truth tables for both modes of operation are shown on the following pages.

Approximately  $1\mu sec$  access time should be allowed after addressing before the analog outputs of the multiplexer are used. A particular point to note is the minimum logic "1" for the multiplexer inputs is +4.0V. If the multiplexer inputs are to be driven from standard TTL logic,  $1k\Omega$  pullup resistors to +5V should be used.

The following diagrams show typical connections for both full differential and single-ended applications along with truth tables which demonstrate multiplexer address  $(A_0, A_1, A_2)$  and enable  $(Mux_1 \text{ Enable})$ ,  $Mux_2 \text{ Enable})$  line functions.

MN7130 is specified and tested as a system (all elements serially connected). Typical specifications for the multiplexer and instrumentation amplifier appear below.

Typical Mux Performance Specifications				
Numbers of Channels	16 Single-Ended 8 Full Differential			
Input Voltage Range	± 10V			
Input Impedance	250MΩ/100pF			
Logic Levels: Logic "1" (min.) Logic "0" (max.)	+ 4.0V + 0.8V			
Logic Currents: Logic "1" Logic "0"	± 10μA ± 10μA			
Access Time	500nsec			
On Resistance	2kΩ			
Cross Talk (1kΩ Source, 1kHz, 20vp-p)	- 68dB			

Typical Instrumentation Amplifier Performance Specifications	
Voltage Range	± 10V
Input Impedance	250MΩ/100pF
Input Current (max.)	± 30nA
Common Mode Rejection Ratio (min.)	70dB
Gain	+ 1V/V
Gain Error: Initial ( + 25 °C) Over Temperature	±0.02% ±0.05%
Gain Nonlinearity	±0.002%
Large Signal Bandwidth	250kHz
Output Slew Rate	± 20V/μsec
Settling Time (20V Step to ±0.01%)	4μsec
Output Voltage Swing (min.)	± 10V
Output Current (min.)	± 2mA
Output Load Capacitance (max.)	50pF

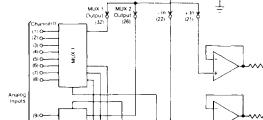
TRACK-HOLD AMPLIFIER—The track-hold amplifier is in the hold mode when the T/H command is a logic "1" and in the sample mode when the T/H command is a logic "0". A total of 10μsec should be allowed after addressing the multiplexer before the T/H is commanded to the hold mode to allow for full scale (20V) changes. Maximum acquisition times for changes less than full scale are shown on the following page.

In data acquisition applications, the T/H command input can usually be driven directly from the A/D converter Status (E.O.C.) output.

As stated earlier, the MN7130 is specified and tested as a system (all elements serially connected). Typical T/H amplifier specifications are listed below.

Typical T/H Amplifier Performance Specifications	
Voltage Range	± 10V
Input Impedance	1010Ω
Input Bias Current	± 15nA
Logic Levels: Logic "1" (min.) Logic "0" (max.)	+2.4V +0.8V
Logic Currents: Logic "1" Logic "0"	± 10μΑ ± 10μΑ
Gain	+ 1V/V
Gain Nonlinearity: Initial (+25°C) Over Temperature	± 0.002% ± 0.005%
Offset Voltage (Track Mode): Initial ( + 25 °C) Over Temperature	± 2mV ± 4mV
Offset Change (Pedestal, Hold Mode) Over Temperature	± 15mV
Droop Rate: Initial (25 °C) (max.) 0 °C to + 70 °C (max.) - 55 °C to + 125 °C (max.)	$\pm 7\mu V/\mu sec$ $\pm 10\mu V/\mu sec$ $\pm 40\mu V/\mu sec$
Acquisition Time (20V Step to ± 0.01%) (max.)	10μsec
Aperture Time (max.)	400nsec
Feedthrough (Hold Mode) @ 1kHz	± 0.01%
Transients Peak Amplitude: Track-to-Hold Hold-to-Track	90mV 100mV

# MULTIPLEXER CONNECTIONS and ADDRESSING



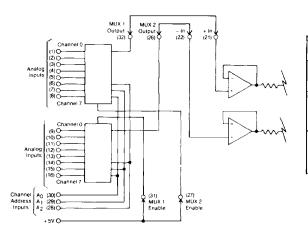
16 Single Ended Input Channels

	Output & Output &	- in * + In *	=
(Channel I)	(32)		
(2) 0			
(3) O			
(5) O X			4-000
(7) 0			
(8) 0	<u>.</u>		
Analog		<b>¬</b> !	
Inputs			4
(9)0	<del>                                      </del>		_ >+~~~ <i>\</i>
(11)0			1
(13)O			
(14)0	<del>         </del>		
(15)0	<b>41</b>		
Channel 15		1	
Channel A <sub>1</sub> (30)0	☐ (27) MUX 2	(31) <b>Q</b> MUX 1	
Address A2 (28)	Enable	Enable	
A3 O		<u> </u>	
	740	4	

A	Address Inputs			Enable Inputs	
A <sub>2</sub>	Α1	A <sub>0</sub>	MUX 1	MUX 2	
X	X	X	1	1 0	ILLEGAL NONE
0	0	0	1 1	0	0
0	1 1	1	1	0	3
1	0	0	1	0	4
1	0	1	1	0	5
1	1	0	1	0	6
1	1	_ 1	1	0	7
0	0	0	0	1	8
0	0	1	0	1	9
0	1	0	0	1	10
0	1	1	0	1	11
1	0	0	0	1	12
1	0	1	0	1	13
1	1	0	0	1	14
1	1	_ 1	0	1	15

Logic "1" > +4.0V Logic "0" < +0.8V

## 8 Differential Input Channels



A	Address Inputs			Enable Inputs	
$A_2$	A <sub>1</sub>	$A_0$	MUX 1	MUX 2	
X	X	x		1	ILLEGAL
X	X	Х	1	0	ILLEGAL
X	X	Χ	0	0	NONE
0	0	0	1	1	0
0	0	1	1	1	1
0	1	0	1	1	2
0	1	1	1	1	3
1	0	0	1	1	4
1	0	1	1	1	5
1	1	0	1	1	6
1	1	1	1	1	7

Logic "1" > +4.0V Logic "0" < +0.8V

