NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT
μPD6130

MSK REMOTE CONTROL SENDER/RECEIVER IC
CMOS IC

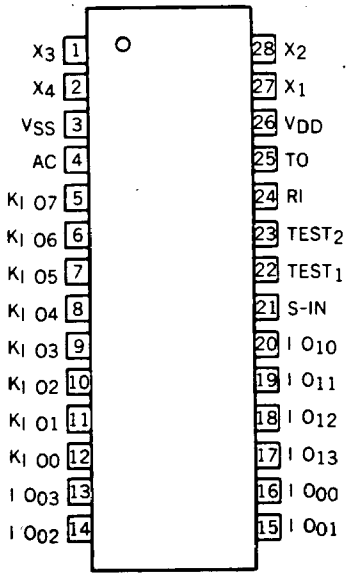
The μPD6130 is a remote control IC that implements sending and receiving the Minimum Shift Keying (MSK) signal.

The μPD6130 is composed of 1 K steps of ROM (10 bits/step), 32 words of RAM (5 bits/word), 4-bit parallel processing ALU, MSK signal generator circuit, receiver circuit, key I/O port, sender output port, receiver and input port. Functions can be further developed by programming.

FEATURES

- MSK signaling two-way remote control IC
- 19 instructions
- Instruction cycle: 17.4 μs/460.8 kHz (ceramic oscillation)
- Program memory (ROM) capacity: 1 024 x 10 bits
- Data memory (RAM) capacity: 32 x 5 bits
- MSK signal generator circuit and receiver circuit incorporated
- I/O: 16 ports
  Serial input pin: 1
- Sending data output format (MSK signaling)
  9-level D/A output
- SCF circuit incorporated (low pass filter)
- Stand-by operation (HALT)
- Ceramic oscillator circuit incorporated for system clock
- CMOS
- Low power consumption
- Low voltage operation guaranteed (2.2 to 6.0 V)

PIN CONNECTION DIAGRAM (Top View)

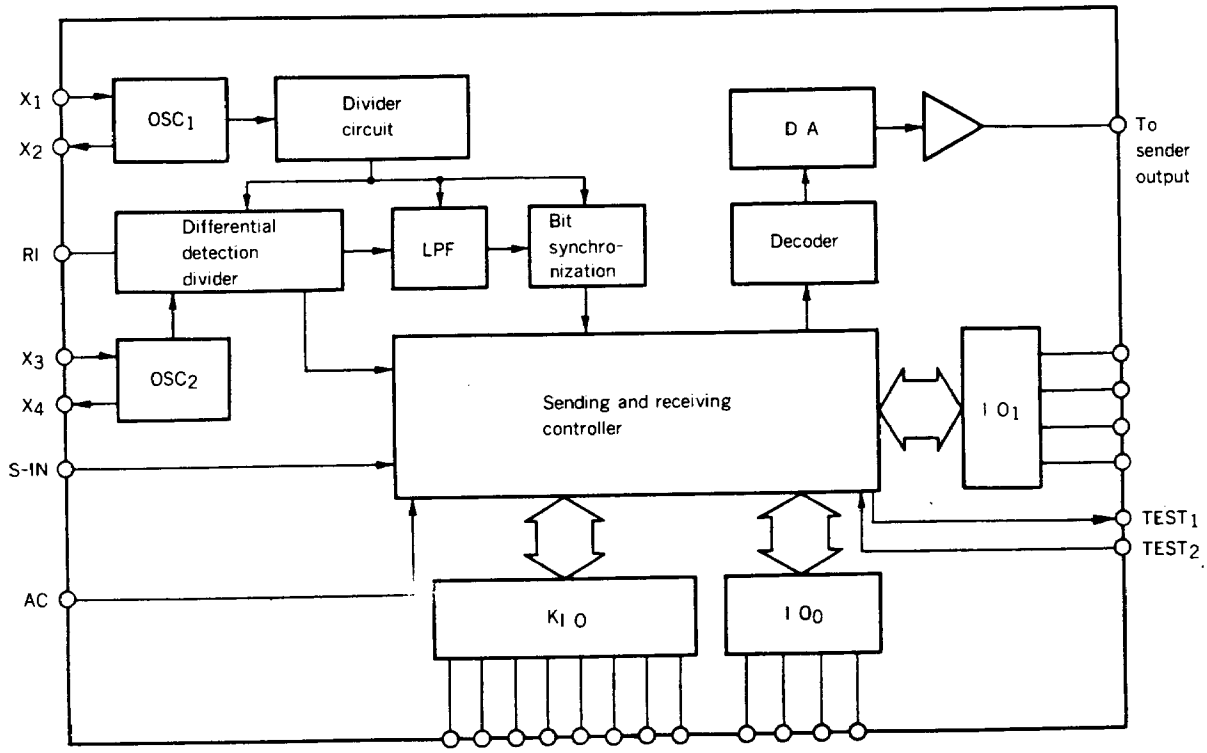


ORDERING INFORMATION

Order Code	Package
μPD6130G	28-pin plastic SOP (375 mil)
μPD6130CA	28-pin shrink DIP (400 mil)

Document No. IC-2515
(O.D.No. IC-7216)
Date Published September 1989 M
Printed in Japan

BLOCK DIAGRAM



1. INTERNAL BLOCK FUNCTIONS

1.1 Program Counter (PC): 10 bits

This is a 10-bit binary counter that retains the 10-bit address data of the program memory.

Fig. 1-1 Configuration of Program Counter

PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	PC

Normally, the program counter is automatically incremented according to the number of bytes of an instruction when the instruction is executed.

When a jump instruction (JMP0, JC, or JF) is executed, the program counter points the destination of the jump.

Immediate data or contents of the data memory are loaded to all or part of the bits of the PC.

When a call instruction (CALL0) is to be executed, the contents of the PC before the execution are incremented and saved in the stack memory, and then the necessary value for each jump instruction is loaded.

When a return instruction (RET) is executed, the contents of the stack memory are incremented by 2 and loaded to the PC. When "all clear" is entered, the PC is initialized to "000".

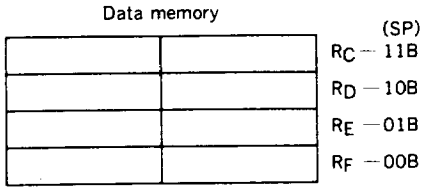
1.2 Stack Pointer (SP): 2 bits

This is a 2-bit register that retains the leading address data of the stack area when data memory is used as the stack memory.

The stack pointer is incremented when the call instruction (CALL0) is executed, and decremented when the return instruction (RET) is executed.

The stack pointer is initialized to 00B when "all clear" is entered. When initialized, the SP points FH, the highest order address of the data memory, as the stack area.

The stack pointer corresponds to the data memory areas as shown below:



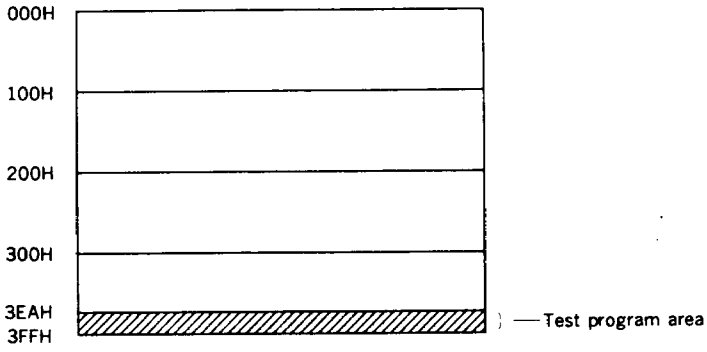
When an overflow occurs in the stack pointer, it is determined that the CPU has run away, and the PC is initialized to "000".

1.3 Program Memory (ROM): 1 024 steps x 10 bits

This is a mask programmable ROM with a configuration of 1 024 steps x 10 bits. The program memory is addressed by the program counter.

The program memory is used to store program and table data.

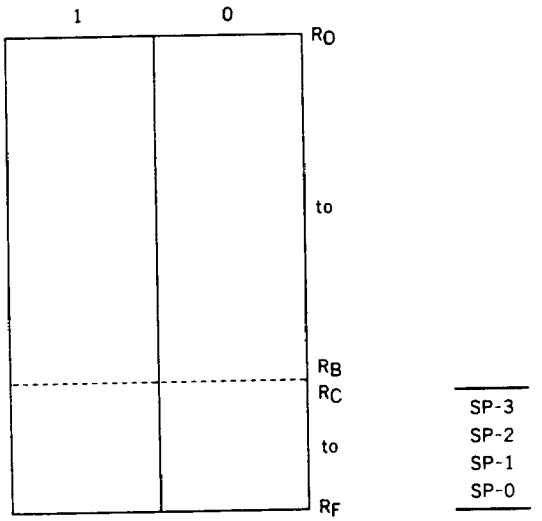
Fig. 1-2 Program Memory Map



1.4 Data Memory (RAM): 32 words x 5 bits

The data memory is static RAM having a configuration of 32 words x 5 bits. The data memory is used to store processed data. The data memory can be processed in units of 8 bits. R_0 can be used as the data pointer of ROM.

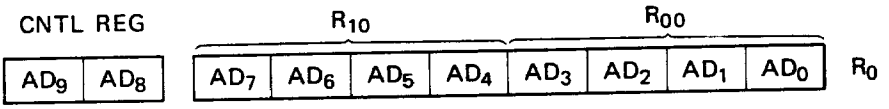
Fig. 1-3 Configuration of Data Memory



1.5 Data Pointer (R_0)

R_0 (R_{10}, R_{00}) of the data memory functions as a data pointer of ROM.
R_0 specifies the lower 8 bits of the ROM address, while the higher 2 bits are specified by the control register.
ROM data tables can be referred readily by setting the ROM address in the data pointer and by calling the contents of ROM.

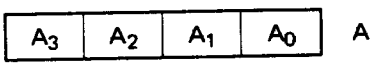
Fig. 1-4 Configuration of Data Pointer



1.6 Accumulator (A): 4 bits

The accumulator is a 4-bit register that plays the central role in arithmetic operations.

Fig. 1-5 Configuration of Accumulator



1.7 Arithmetic and Logic Unit (ALU): 4 bits

The arithmetic and logic unit is a 4-bit operation circuit that implements simple processing, mainly logical operations.

1.8 Flags

(1) Status flag

When the condition of each port is polled by the STTS instruction, if it matches the condition specified by the instruction the status flag (F) is set to 1.

(2) Carry flag

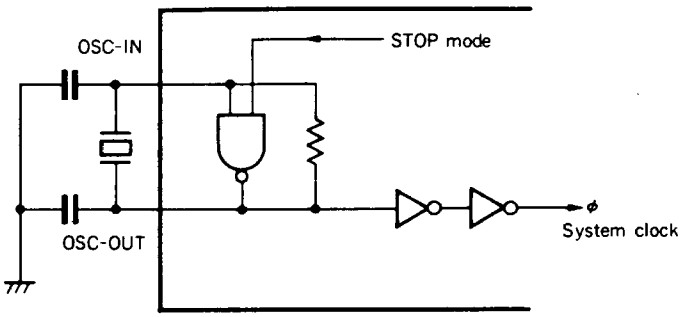
After an increment (INC) or rotate left (RL) instruction is executed, if a carry is produced in the MSB of the accumulator the carry flag (C) is set to 1.

When the SCAF instruction is executed and if the contents of the accumulator are "FH", the carry flag (C) is also set to 1.

1.9 System Clock Generator Circuit

The system clock generator circuit consists of an oscillator circuit for a ceramic oscillator (400 to 500 kHz).

Fig. 1-6 System Clock Generator Circuit

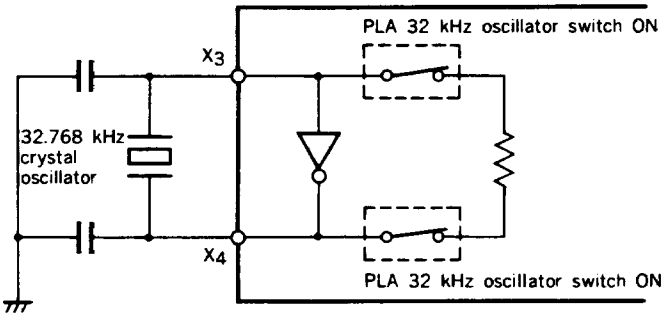


In the STOP mode (HALT in the state of oscillation stop), the system clock generator circuit stops its oscillator circuit, and thus the system clock ϕ also stops.

1.10 Sub-clock Generator Circuit

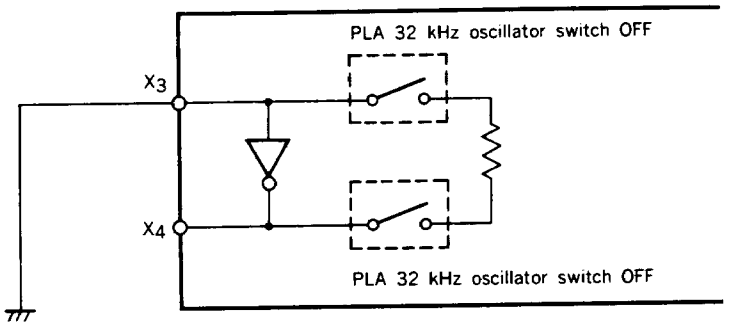
The sub-clock generator circuit consists of a 32.768 kHz crystal oscillator circuit.

Fig. 1-7 Sub-clock Generator Circuit



With the sub-clock generator circuit, the 32.768 kHz oscillator can either be used or not used, selected by the PLA data. When the 32.768 kHz oscillator is not to be used, set the PLA data so that X_3 pin (OSC-IN) is fixed to V_{DD} or V_{SS}.

Fig. 1-8 Sub-clock Generator Circuit



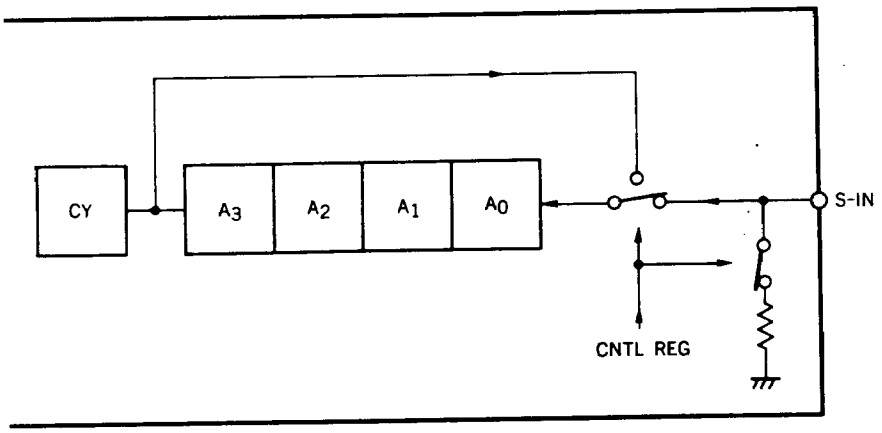
1.11 Serial Input Port

Serial data is entered using the serial input port. When the control register (P_1) is set to the serial input mode, the serial input port is connected as the input to the LSB of the accumulator. At the same time, the serial input port is pulled down to the V_{SS} level inside the LSI. If the accumulator left shift instruction is executed in this state, the data from the serial input port is fetched to the LSB of the accumulator.

When the control register is released from the serial input mode, the serial input pin becomes high impedance.

When the accumulator left shift instruction is executed, data in the MSB is input to the LSB.

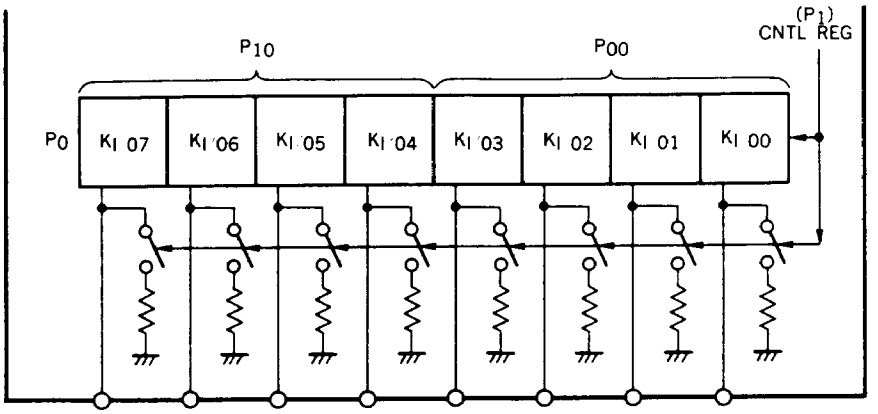
Fig. 1-9 Configuration for Serial Input Port



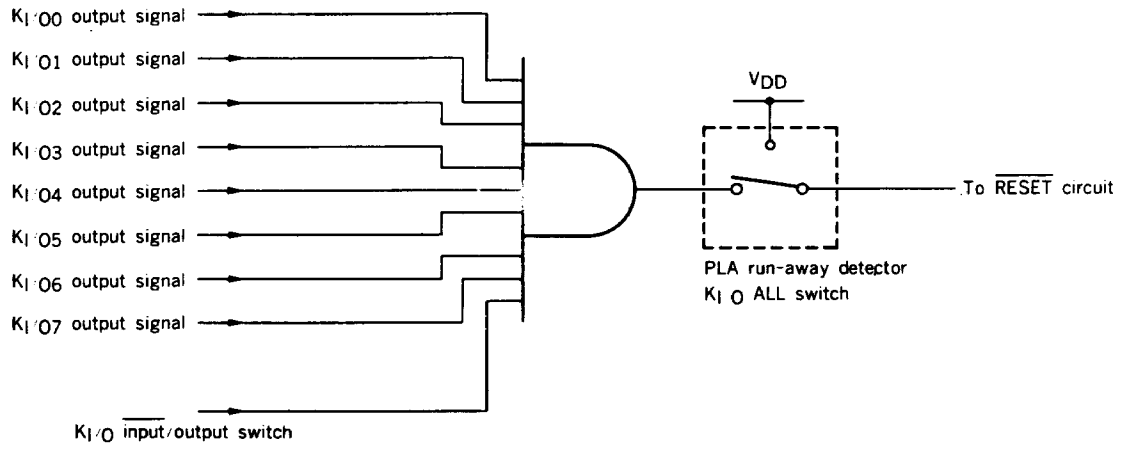
1.12 $K_{I/O}$ Port (P_0)

The $K_{I/O}$ port is an 8-bit port for key scan output. When the control register (P_1) is set to the input mode, the port becomes available as the 8-bit input port. In the input mode, all the pins in the LSI are pulled down to the V_{SS} level.

Fig. 1-10 Configuration of $K_{I/O}$ Port



1.13 Configuration for Run-away Detector $K_{I/O}$ ALL



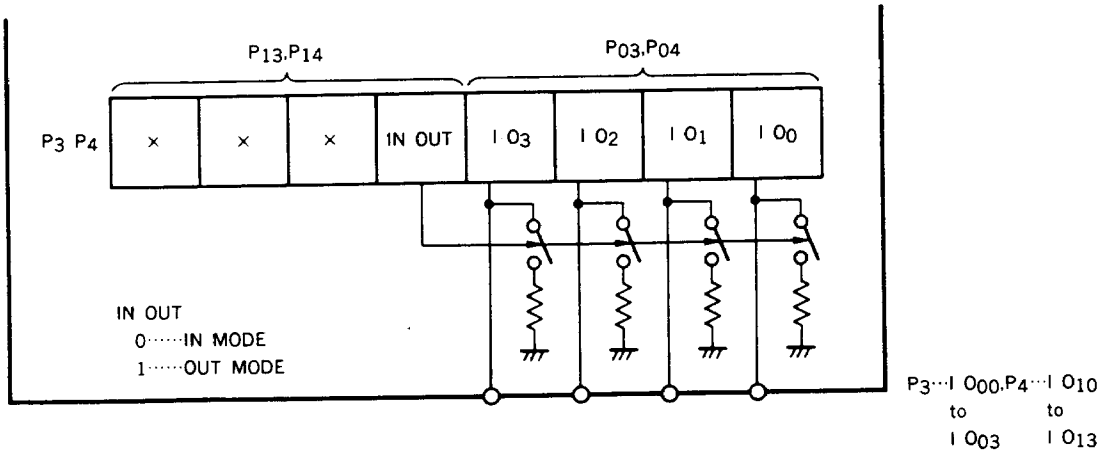
If the run-away detector $K_{I/O}$ ALL switch has been turned on (set to 1) using the PLA data, the CPU is reset under the following conditions: the $K_{I/O}$ pins are in the input mode while the CPU is in the oscillation stop HALT mode, or, one or more of the $K_{I/O}$ pins is at the L level.

If the pin is to be used as the source of the switch, turn on the switch using the PLA data.

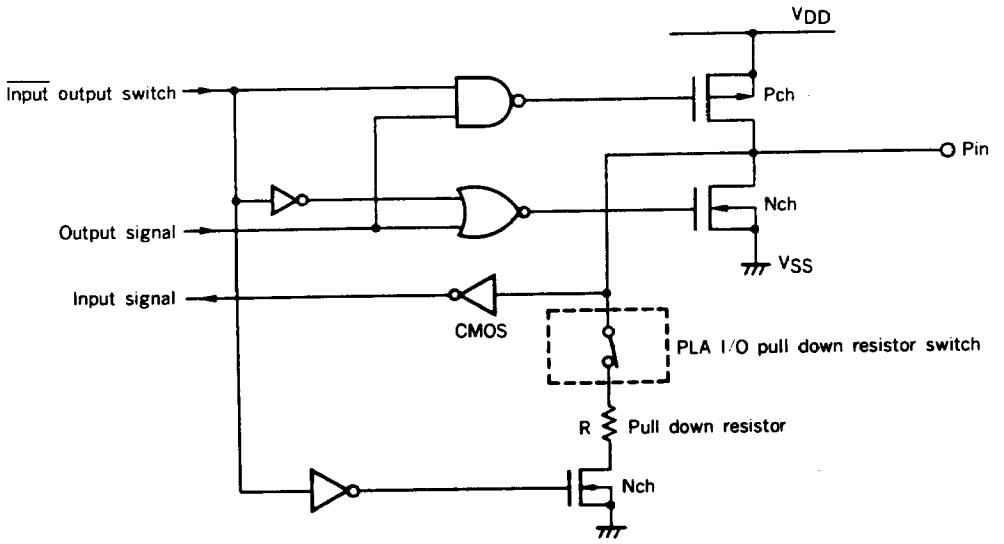
1.14 I/O Ports (P_3, P_4)

P_3 and P_4 are the I/O ports for key matrix expansion. The input and output modes are switched by the LSBs in P_{13} and P_{14}. In the output mode, the pull down resistor in the LSI is disconnected.

Fig. 1-11 Configuration of I/O ports



1.15 Configuration for $K_{I/O}$ and I/O Pull Down Resistor



The pull down resistor can either be connected or not connected to I/O, selected by the PLA data.

When the pull down resistor switch is turned on (set to 1) by the PLA data, pull down resistor R is turned on only in the input mode.

When the pin is to be used as the switch, turn on the pull down resistor switch using the PLA data.

Connection of the pull down resistor to $K_{I/O}$ cannot be switched using the PLA data.

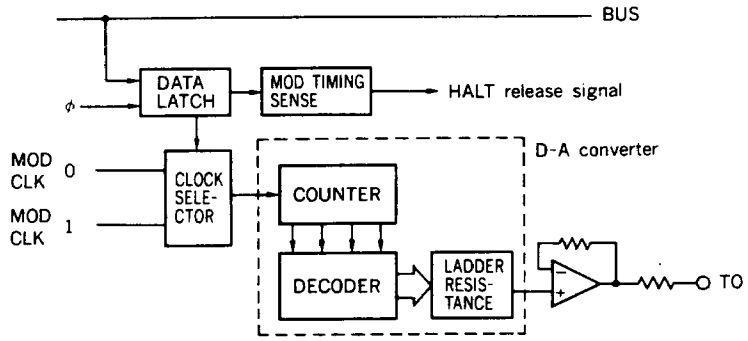
When $K_{I/O}$ is in the input mode, all the pins are pulled down to the V_{SS} level.

1.16 TO Port (P_{16})

The Minimum Shift Keying (MSK) signal is output via the TO port (The TO port is a MOD port). When D_6 of the control register P_1 is set to 1 and the CPU enters the HALT mode, the analog circuit is powered off. While the analog circuit is powered off, the state of the TO port can be selected from pull up resistor, pull down resistor, and high impedance, using the PLA data.

Fig. 1-12 shows the configuration of the transmitter:

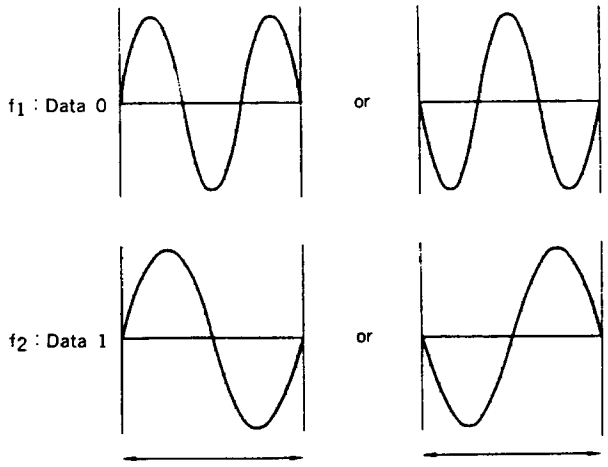
Fig. 1-12 Transmitter Block Diagram



Data is transmitted bit by bit. Clock to be supplied to the D–A converter is selected according to the data written in the data latch. Whether data 1 or data 0 is to be transmitted depends on the selection of the clock supplied to the D–A converter.

Fig. 1-13 shows the transmitted waveforms of data 0 and data 1:

Fig. 1-13 Transmitted Waveforms of Data 0 and Data 1



The baud rate is selected using the PLA data.

The baud rate corresponds with the original oscillation as specified in the formulas in the following table:

PLA Data	Correspondence between f_1 or f_2 and f_{OSC}	f_1/f_2 (Hz) when f_{OSC} = 460.8 kHz
C_4	$f_1 = f_{OSC}/2^9 \times 3$ $f_2 = 1.5\ f_1$	300/450
C_3	$f_1 = f_{OSC}/2^8 \times 3$ $f_2 = 1.5\ f_1$	600/900
C_2	$f_1 = f_{OSC}/2^7 \times 3$ $f_2 = 1.5\ f_1$	1.2 k/1.8 k
C_1	$f_1 = f_{OSC}/2^6 \times 3$ $f_2 = 1.5\ f_1$	2.4 k/3.6 k
C_0	$f_1 = f_{OSC}/2^5 \times 3$ $f_2 = 1.5\ f_1$	4.8 k/7.2 k

When f_{OSC} = 460.8 kHz, f_1 and f_2 are respectively 300 and 450, 600 and 900, 1.2 k and 1.8 k, 2.4 k and 3.6 k, or 4.8 k and 7.2 k, according to the PLA data.

The transmitted data is determined by D_3 and D_2 of port P_{16} and is transmitted bit by bit. While bit data is being transmitted, the CPU waits for the completion of the transmission in the HALT mode.

The OUT P_{16}, A instruction resets the HALT release signal and sends data to P_{15}.

The HALT MODE instruction sets the HALT release signal.

The output from the low pass filter is used as the differential-detected input data. This output is latched and timed by the clock output from the bit synchronization circuit, to be used as the received data. The bit synchronization circuit compensates the output clock synchronization, by comparing the data 0/1 change points to the timing of the clock output from the circuit itself.

To synchronize the operation of the bit synchronization circuit with the input signal timing, input the repetitive signal "01" for 12 bits or more as the bit synchronization signal.

The receiving operation of the CPU is basically the same as for transmission. The CPU waits the completion of one-bit data receiving in the HALT mode.

The IN A, P_{06} instruction resets the HALT release signal, and sends P_{06} data to the accumulator.

The HALT DEM instruction sets the HALT release signal.

When data is sent from port P_{06} to the accumulator, the data is received at the same time as when the next HALT release signal is set. Thus, data receiving is accomplished by repetitively issuing the IN A, P_{06} instruction and the HALT DEM instruction.

When data is sent from the accumulator to port P_{16}, the data is sent simultaneously when the next HALT release signal is set. Thus, data transmission is accomplished by repetitively issuing the OUT P_{16}, A instruction and the HALT MOD instruction.

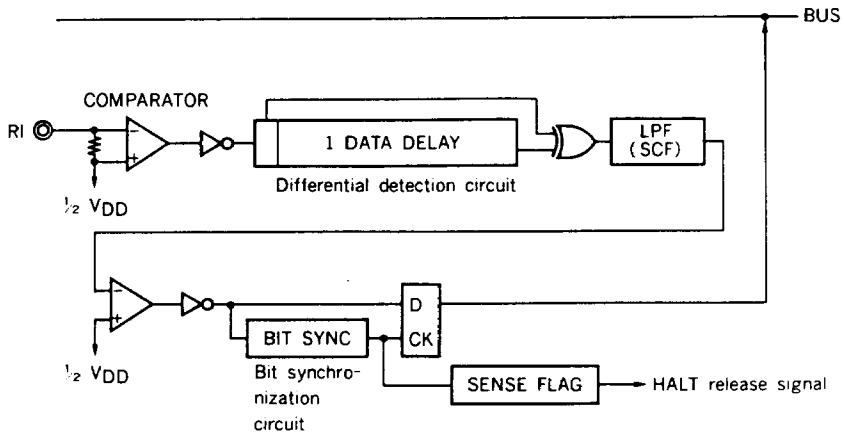
1.17 RI Port (P_{06})

The MSK signal is input via the RI port. (The RI port is a DEM port). When D_6 of the control register P_1 is set to 1 and the CPU enters the HALT mode, the analog circuit is powered off. While the analog circuit is powered off, the state of the RI port can be selected from pull up resistor, pull down resistor, and high impedance, using the PLA data.

Fig. 1-14 shows the configuration of the receiver.

The input MSK signal is checked for retardation by the differential detector circuit which consists of 48-stage shift register. The detector outputs the exclusive OR of the input data and the data delayed by one set of input data behind the input data. The output from the differential detector contains high frequency; the low pass filter removes this. The low pass filter is a switched capacitor filter (SCF).

Fig. 1-14 Receiver Block Diagram



1.18 Control Register (P_1)

The control register supports 8 bits. The following items can be controlled:

Table 1-1

D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
TEST MODE		*	HALT	D.P. AD_9	D.P. AD_8			$K_{I/O}$	RL A_{CC} A_0 ←	
Must be set to 0		NOP	NOP	*	*	DEM	NOP	IN	A_3	0
		NOP	OSC STOP	*	*	Timer	NOP	OUT	S-IN	1

D_0 : Specifies data to be input to A_0, when the accumulator is to be shifted to the left. "0" = A_3, "1" = S–IN

D_1 : Specifies the state of $K_{I/O}$. "0" = IN MODE, "1" = OUT MODE

D_3 : Specifies the DEM or interval timer mode. "0" = DEM mode, "1" = Timer mode

D_4, D_5 : Specifies the higher 2 bits of the ROM data pointer.

D_6 : Specifies the oscillating circuit when the HALT instruction is executed. Also specifies power-on or power-off of the analog circuit.

"0" : Oscillation continues. The analog circuit is powered on.

"1" : Oscillation stops. The analog circuit is powered off. (STOP mode)

D_7 : NOP

D_8, D_9 : These are test mode setting registers. Set both D_8 and D_9 to "0".

2. STAND-BY FUNCTION (HALT)

The μPD6130 provides the stand-by mode (HALT) to save power consumption while the program is in the stand-by condition. Oscillation can be stopped in the stand-by mode by use of the control register. (STOP mode)

When the CPU enters the stand-by mode, the program stops and the contents of all the incorporated registers and data memory are retained.

2.1 STOP Mode (Oscillation Stop HALT)

In the STOP mode, the system clock generator circuit (ceramic oscillator oscillation circuit) stops, and the analog circuit is powered off. Thus, all operations that require the system clock are stopped.

2.2 HALT Mode (Oscillation Continued HALT)

The CPU stops its operation until a HALT release condition occurs.

The system clock generator circuit and the analog circuit are operational in this mode.

2.3 Stand-by Release Conditions

(1) S–IN input
(2) $K_{I/O}$ input
(3) MOD/DEM
(4) I/O input
(5) I/O, INTVL input
(6) S–IN, INTVL input

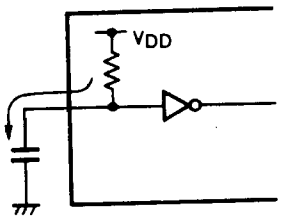
3. AC PIN

The program counter is reset by placing the AC pin at the V_{SS} level.

Watchdog timer function

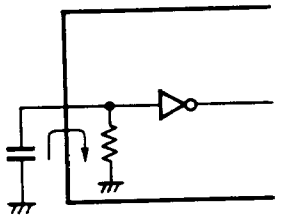
A 0.1 μF capacitor added between the AC pin and V_{SS} serves as a CR watchdog timer controlled by the power-on reset function and program.

Charge mode



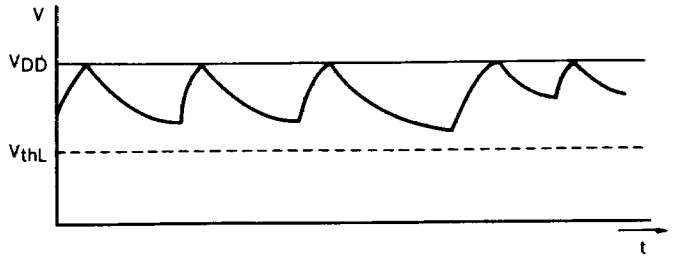
Charging start instruction
Execute the HALT instruction immediately after NOP.

Discharge mode



Discharging start instruction
Discharge starts after the NOP instruction is executed.

Repetitive pattern of charging and discharging



Use program control to keep charge C above V_{thL}.

4. MASK OPTION

The following items can be selected by switching mask options.

(1) Presence or absence of pull down resistors across ports S–IN, I/O_0, and I/O_1.
(2) Selection of status of ports RI and TO; pull down resistor, pull up resistor, or high impedance
(3) Selection of port TO 1/2 V_{DD} or floating
(4) Presence or absence of 32.768 kHz crystal oscillator
(5) Selection of baud rate
(6) Selection of timer time for interval receiving
(7) Selection of run-away detection

The PLA data is registered at the end of the object code.

Switch Setting Bit Assignments

Address	Corresponding Section	MSB 7	6	5	4	3	2	1	LSB 0
0	S–IN	0	0	0	0	0	0	S–IN pull down resistor	0
1	Run-away detection	$K_{I/O}$ ALL	HALT S–IN	HALT $K_{I/O}$	HALT INTVL	HALT I/O_0	HALT I/O_1	HALT MOD	HALT DEM
2	Baud rate	0	0	0	C_4	C_3	C_2	C_1	C_0
3	OSC, RI, TO	0	32 K OSC	RI pull up resistor	RI pull down resistor	0	TO 1/2 V_{DD}/ floating	TO pull up resistor	TO pull down resistor
4	Timer	0	0	0	T_{20}	T_{16}	T_{12}	T_{10}	T_2
5	I/O_0	I/O_0 pull down resistor				0	0	0	0
6	I/O_1	I/O_1 pull down resistor				0	0	0	0

Switch corresponding to data

1. Pull down resistor (S–IN, I/O_0, I/O_1)
   - 0 ⇒ Not provided
   - 1 ⇒ Provided
2. Pull up resistor/pull down resistor/high impedance (RI, TO)
   - 0 ⇒ Not provided
   - 1 ⇒ Provided

Only the following combinations can be selected:

Pull Up	Pull Down	Status
0	0	High impedance
0	1	Pull down resistor provided
1	0	Pull up resistor provided

3. TO 1/2 V_{DD}/floating
   - 0 ⇒ 1/2 V_{DD} output
   - 1 ⇒ Floating
4. 32.768 kHz oscillator
   - 0 ⇒ Not provided
   - 1 ⇒ Provided . . . 32.768 kHz crystal oscillators are used for X_3 and X_4.
5. Baud rate selection
   - 0 ⇒ Not selected
   - 1 ⇒ Selected

LSB

C_4	C_3	C_2	C_1	C_0	Baud Rate (f_{OSC} = 460.8 kHz)
1	0	0	0	0	300/450
0	1	0	0	0	600/900
0	0	1	0	0	1.2 k/1.8 k
0	0	0	1	0	2.4 k/3.6 k
0	0	0	0	1	4.8 k/7.2 k

⑥ Timer selection

0 ⇒ Not selected
1 ⇒ Selected

LSB

T_{20}	T_{16}	T_{12}	T_{10}	T_2	Set Time
1	0	0	0	0	20 s
0	1	0	0	0	16 s
0	0	1	0	0	12 s
0	0	0	1	0	10 s
0	0	0	0	1	2 s

⑦ Run-away detection

(1) $K_{I/O}$ ALL

In the oscillation stopped HALT mode, if the $K_{I/O}$ pins are in the input mode, or any $K_{I/O}$ pin is at the L level, the system is reset.

0 ⇒ Reset function not provided
1 ⇒ Reset function provided

(2) HALT release condition specification

In the HALT mode, if there is any condition that is specified as "not used" by the PLA data, the system is reset.

0 ⇒ Used
1 ⇒ Not used

When

HALT #00EH instruction (I/O_0, I/O_1, INTVL)
#006H

Or, HALT #00F instruction (S–IN, INTVL)
#007

is used, HALT S–IN, HALT I/O_0, HALT I/O_1 are all specified as "not used".

Data Setting Form

(HEX)

Address	μPD6130	
0	0	0 or 2
1	0 to F	0 to F
2	0 or 1	0, 1, 2, 4, 8
3	0, 1, 2, 4, 5, 6	0, 1, 2, 4, 5, 6
4	0 or 1	0, 1, 2, 4, 8
5	0 to F	0
6	0 to F	0

Mnemonic ⟷ Machine Language Correspondence Table

Accumulator Operation Instructions

R_r	–	R_{10}	R_{11}	R_{12}	----	R_{1F}	R_{00}	R_{01}	----	R_{0F}
ANL A, R_r		D00	D01	D02		D0F	D20	D21		D2F
ANL A, @R_0H	D10									
ANL A, @R_0L	D30									
ANL A, #data	D31									
ORL A, R_r		E00	E01	E02		E0F	E20	E21		E2F
ORL A, @R_0H	E10									
ORL A, @R_0L	E30									
ORL A, #data	E31									
XRL A, R_r		A00	A01	A02		A0F	A20	A21		A2F
XRL A, @R_0H	A10									
XRL A, @R_0L	A30									
XRL A, #data	A31									
INC A	A13									
RL A	F13									

I/O Instructions

P_P	P_{10}	P_{11}	P_{13}	P_{14}	P_{16}	P_{00}	P_{01}	P_{03}	P_{04}	P_{06}
IN A, P_P	F18	F19	F1B	F1C	F1E	F38	F39	F3B	F3C	F3E
OUT P_P, A	218	219	21B	21C	21E	238	239	23B	23C	23E
ANL A, P_P	D18	D19	D1B	D1C	D1E	D38	D39	D3B	D3C	D3E
ORL A, P_P	E18	E19	E1B	E1C	E1E	E38	E39	E3B	E3C	E3E
XRL A, P_P	A18	A19	A1B	A1C	A1E	A38	A39	A3B	A3C	A3E

P_P	P_0	P_1	P_3	P_4	P_6
OUT P_P, #data	318	319	31B	31C	31E

P_{1P} and P_{0P} act as a pair.

Data Transfer Instructions

R_r		R_{10}	R_{11}	R_{12}	----	R_{1F}	R_{00}	R_{01}	----	R_{0F}
MOV A, R_r		F00	F01	F02		F0F	F20	F21		F2F
MOV A, @R_0H	F10									
MOV A, @R_0L	F30									
MOV A, #data	F31									
MOV R_r, A		200	201	202		20F	220	221		22F

R_r		R_0	R_1	R_2	----	R_F
MOV R_r, #data		300	301	302		3F
MOV R_r, @R_0		320	321	322		2F

R_{1r} and R_{0r} act as a pair resistor.

Branch Instruction

R_r	–	R_0	R_1	R_2		R_F
JMP0 addr	411					
JMP0 R_r	–	400	401	402		40F
JC addr	611					
JC R_r	–	600	601	602		60F
JNC addr	631					
JNC R_r	–	620	621	622		62F
JF addr	711					
JF R_r	–	700	701	702		70F
JNF addr	731					
JNF R_r	–	720	721	722		72F

← Pair resistor

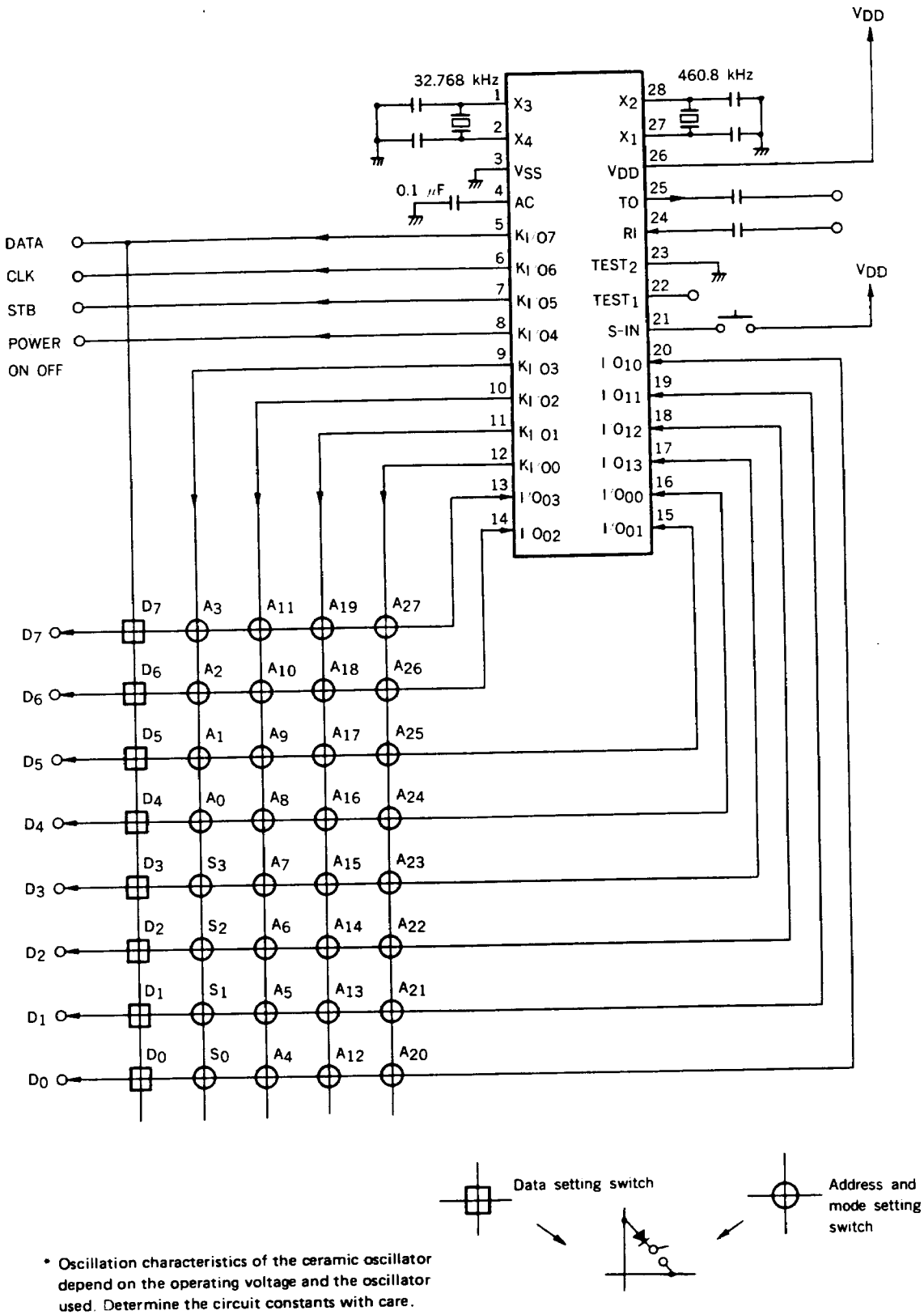
Sub-routine Instructions

CALL0 addr	312	411
RET	412	

Other Instructions

		R_{00}	R_{01}	R_{02}		R_{0F}
HALT #data	111					
STTS R_{0r}		120	121	122		12F
STTS #data	131					
SCAF	D13					
NOP	000					

APPLICATION CIRCUIT DIAGRAM



* Oscillation characteristics of the ceramic oscillator depend on the operating voltage and the oscillator used. Determine the circuit constants with care.

Before μPD6130 is used, the effect of the operating frequency deviation between the sender and receiver upon the transferred bit pattern must be taken into consideration.

Figs. 1 and 2 show the relationship between the transmittable bit pattern and operating frequency fluctuations between the sender and the receiver.

Fig. 1

Frequency allowable fluctuation ratio vs.
number of identical code repeated bits (maximum)

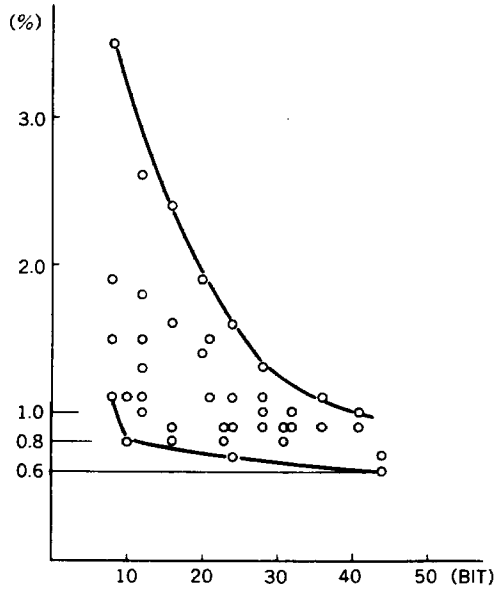
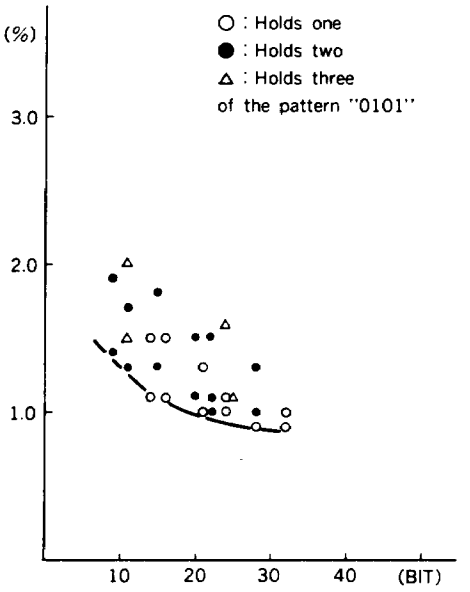


Fig. 2

Frequency allowable fluctuation ratio vs.
number of identical code repeated bits (maximum)



As seen in the figures above, if the transmission pattern contains many repetitions of the same code, the receiver cannot trace the frequency shift at the sender.

Hence, in μPD6130 applications, bit strings having the same code must not be repeated many times in a row.

When the operating frequency fluctuations between the sender and the receiver are within ±1 %, set the transmitted bit pattern as follows:

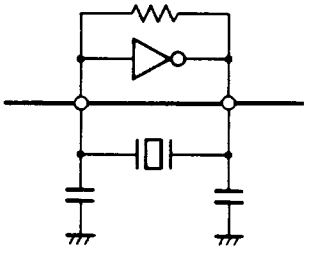
(1) Repetition of the same code containing no "0101" pattern is permitted only within 8 bits.
(2) Repetition of the same code containing one "0101" pattern is permitted only within 15 bits.
(3) Repetition of the same code containing two "0101" patterns is permitted only within 19 bits.
(4) Repetition of the same code containing three "0101" patterns is permitted only within 24 bits.

To settle the operating frequency fluctuations within ±1 %, use either of the ceramic oscillators specified below for the μPD6130.

For details of the oscillating characteristics, contact the manufacturer of the oscillator.

Manufacturer	Type number by the manufacturer
Murata	CSB460E930
Toko	P11ACRK460-M31

Application circuit



ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Power Voltage	V_{DD}	7.0	V
Input Voltage	V_{IN}	−0.3 to V_{DD} +0.3	V
Operating Temperature	T_{opt}	−40 to +85	°C
Storage Temperature	T_{stg}	−40 to +125	°C

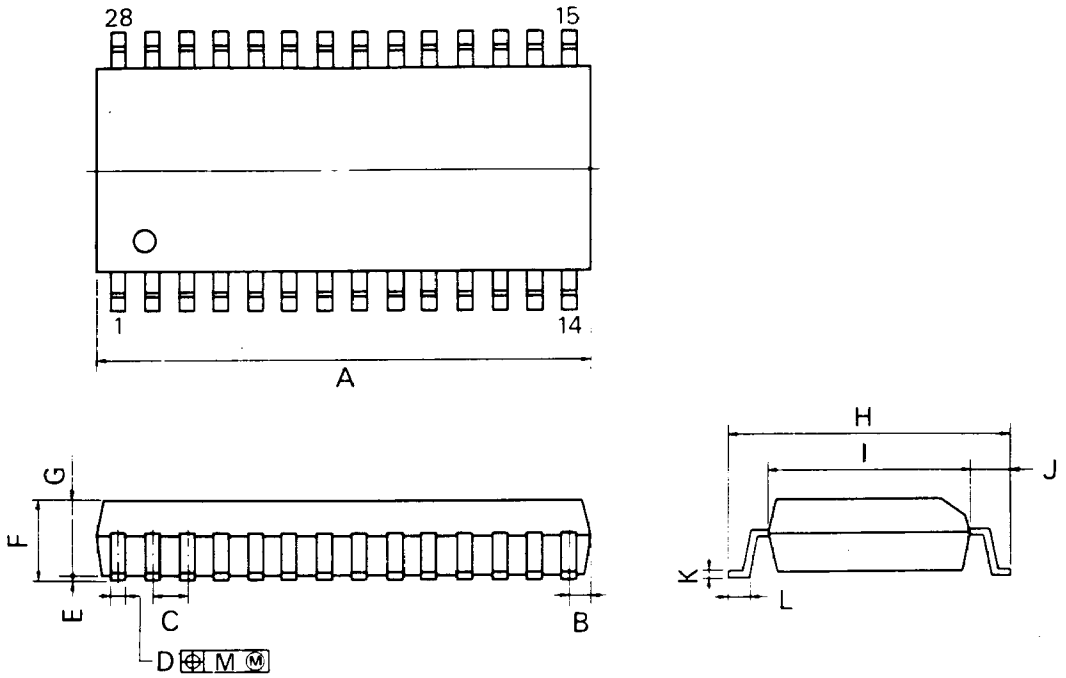
RECOMMENDED OPERATING RANGE (T_a = −40 to +85 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Operating Power Voltage Range	V_{DD}	2.2	3.0	6.0	V
Oscillating Frequency 1 (X_1, X_2)	f_1	400	460.8	500	kHz
Oscillating Frequency 2 (X_3, X_4)	f_2		32.768		kHz
Receiving (RI) Input Signal	V_{in}	0.05	0.2	1.0	V_{p-p}

ELECTRIC CHARACTERISTICS (V_{DD} = 3.0 V, f_1 = 460.8 kHz, f_2 = 32.768 kHz, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Current Consumption 1	I_{DD1}	0.5	1	2	mA	f_1 = 460.8 kHz, f_2 = 32 kHz
Current Consumption 2	I_{DD2}		2.5	5.0	μA	f_1 = STOP, f_2 = 32 kHz
$K_{I/O}$, I/O High Level Input Current	I_{IH1}	10		35	μA	$V_I = V_{DD}$
$K_{I/O}$, I/O Low Level Input Current	I_{IL1}			−0.2	μA	$V_I = V_{SS}$
$K_{I/O}$, I/O High Level Output Current	I_{OH1}	−0.8		−3	mA	V_O = 2.7 V
$K_{I/O}$, I/O Low Level Output Current	I_{OL1}	25		110	μA	V_O = 2.1 V
S−IN High Level Output Current	I_{IH2}	6		20	μA	$V_I = V_{DD}$
S−IN Low Level Output Current	I_{IL2}			−0.2	μA	$V_I = V_{SS}$
S−IN High Level Output Current	I_{IH2}			0.2	μA	$V_I = V_{DD}$ (no pull down resistor)
Transmission Output Voltage (TO)	V_O	0.5	0.6	0.7	V_{p-p}	$R_L = \infty$
Reception Input Voltage (RI)	V_i	0.05		1.0	V_{p-p}	
Reception Input Impedance (RI)	R_i	120	200	350	kΩ	

28PIN PLASTIC SOP (375 mil)



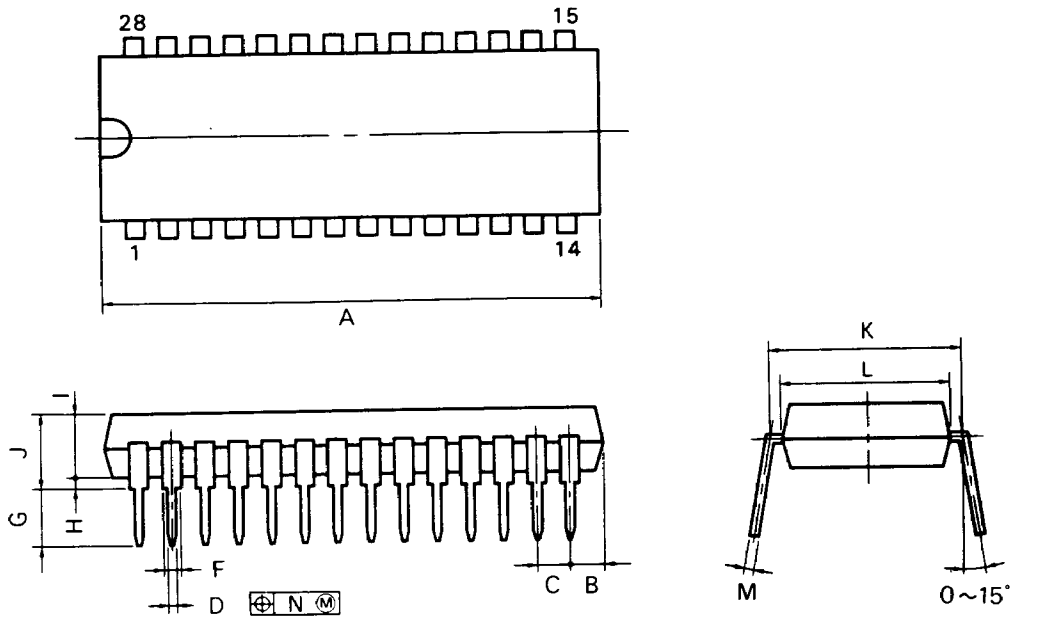
P28GM-50-375B-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1 ± 0.1	0.004 ± 0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3 ± 0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8 ± 0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005

28PIN PLASTIC SHRINK DIP (400 mil)



S28C-70-400B

NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{+0.3}$	$0.126^{+0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product. Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SMT MANUAL" (IEI-1207).

μPD6130G

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature : 230 °C or below, Reflow time : 30 seconds or below (210 °C or higher), Number of reflow process : 1, Exposure limit* : None	IR30-00
VPS	Peak package's surface temperature : 215 °C or below, Reflow time : 40 seconds or below (200 °C or higher), Number of reflow process : 1, Exposure limit* : None	VP15-00
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below, Number of flow process : 1, Exposure limit* : None	WS60-00
Partial heating method	Terminal temperature : 300 °C or below, Flow time : 10 seconds or below, Exposure limit* : None	

*: Exposure limit before soldering after dry-pack package is opened.
Storage conditions : 25 °C and relative humidity a 65 % or less.

Note : Do not apply more than a single process at once, except for "Partial heating method".

TYPES OF THROUGH HOLE MOUNT DEVICE

μPD6130CA

Soldering Process	Soldering Conditions
Wave soldering	Solder temperature : 260 °C or below, Flow time : 10 seconds or below

[MEMO]