

TM4161EP5 65,536 BY 5-BIT MULTI-PORT VIDEO RAM MODULE

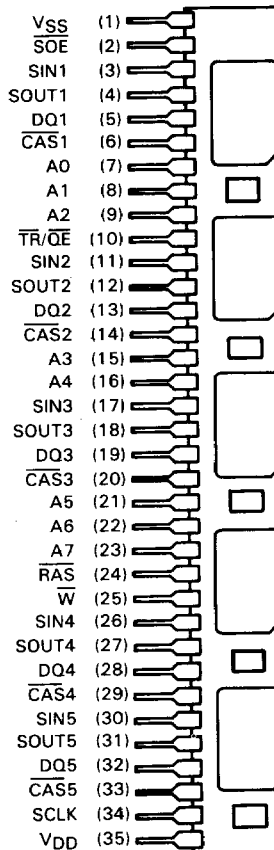
JULY 1984 — REVISED NOVEMBER 1985

- 65,536 X 5 Organization
- Single 5-V Supply (10% Tolerance)
- 35-Pin Single-in-Line Package (SIP)
- Utilizes Five Multiport Video RAMs in Plastic Chip Carriers
- Serial In/Serial Out Capability
- Dual Accessibility — One Port Sequential Access, One Port Random Access
- Five Serial Shift Registers for Sequential Access Applications, Each Comprised of Four Cascaded 64-Bit Segments
- Designed for both Video and Non-Video Applications
- Fast Serial Port . . . Can Be Configured for Video Data Rates in Excess of 150 MHz
- $\overline{TR}/\overline{OE}$ as Output Enable Allows Direct Connection of DQ and Address Lines to Simplify System Design
- Separate Serial In and Serial Out to Allow Simultaneous Shift In and Out
- Supported by TI's TMS34061 Video System Controller (VSC)
- \overline{SOE} Simplifies Multiplexing of Serial Data Streams
- Long Refresh Period . . . 4 ms (256 Cycles)
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Outputs
- Performance Ranges:

| | ACCESS TIME ROW ADDRESS (MAX) | ACCESS TIME COLUMN ADDRESS (MAX) | READ OR WRITE CYCLE (MIN) |
|--------------|---|--|---------------------------------------|
| TM4161EP5-15 | 150 ns | 100 ns | 240 ns |
| TM4161EP5-20 | 200 ns | 135 ns | 315 ns |

- Separate \overline{CAS} Control with Common Data-In and Data-Out Lines
- Low Power Dissipation:
 - Operating . . . 1250 mW (Typ)
 - Standby . . . 400 mW (Typ)
- Operating Free-Air Temperature . . . 0°C to 70°C

**P SINGLE-IN-LINE PACKAGE
(TOP VIEW)**



5
Dynamic RAM Modules

| PIN NOMENCLATURE | |
|-----------------------------------|-----------------------------------|
| A0-A7 | Address Inputs |
| $\overline{CAS1}-\overline{CAS5}$ | Column-Address Strobes |
| $\overline{DQ1}-\overline{DQ5}$ | Random-Access Data In/Data Out |
| \overline{RAS} | Row-Address Strobe |
| SCLK | Serial Data Clock |
| SIN1-SIN5 | Serial Data In |
| \overline{SOE} | Serial Output Enable |
| SOUT1-SOUT5 | Serial Data Out |
| $\overline{TR}/\overline{OE}$ | Register Transfer/Q Output Enable |
| \overline{VDD} | 5-V Supply |
| \overline{VSS} | Ground |
| \overline{W} | Write Enable |

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



TM4161EP5 65,536 BY 5-BIT MULTIPOINT VIDEO RAM MODULE

description

The TM4161EP5 is a 320K dual-access dynamic random-access memory module organized as 65,536 \times 5-bits in a 35-pin single-in-line package comprising five TMS4161FML, 65,536 \times 1-bit Multipoint Video RAMs in 22-lead plastic chip carriers mounted on top of a substrate together with five decoupling capacitors. The random-access port makes the module look like it is organized as 65,536 words of five bits each. The sequential-access port is interfaced to five internal 256-bit dynamic shift registers each organized as four cascaded 64-bit shift register segments which are accessed serially. One, two, three, or four 64-bit shift register segments can be sequentially read out after a transfer cycle depending on a two-bit code applied to the two most significant column address inputs.

The TM4161EP5 features full asynchronous dual access capability except when transferring data between the shift registers and the memory array.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{\text{RAS}}$ in order to retain data. $\overline{\text{CAS}}$ can remain high during the refresh sequence to conserve power. Note that the transfer of a row of data from the memory array to the shift registers also refreshes that row.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data in are latched on chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TM4161EP5 is guaranteed for operation from 0°C to 70°C.

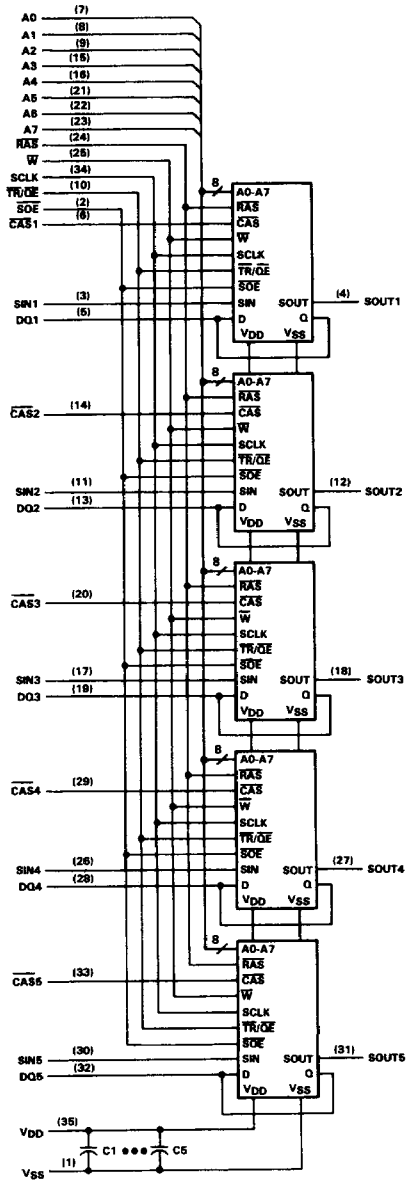
5

Dynamic RAM Modules



TM4161EP5
65,536 BY 5-BIT MULTI-PORT VIDEO RAM MODULE

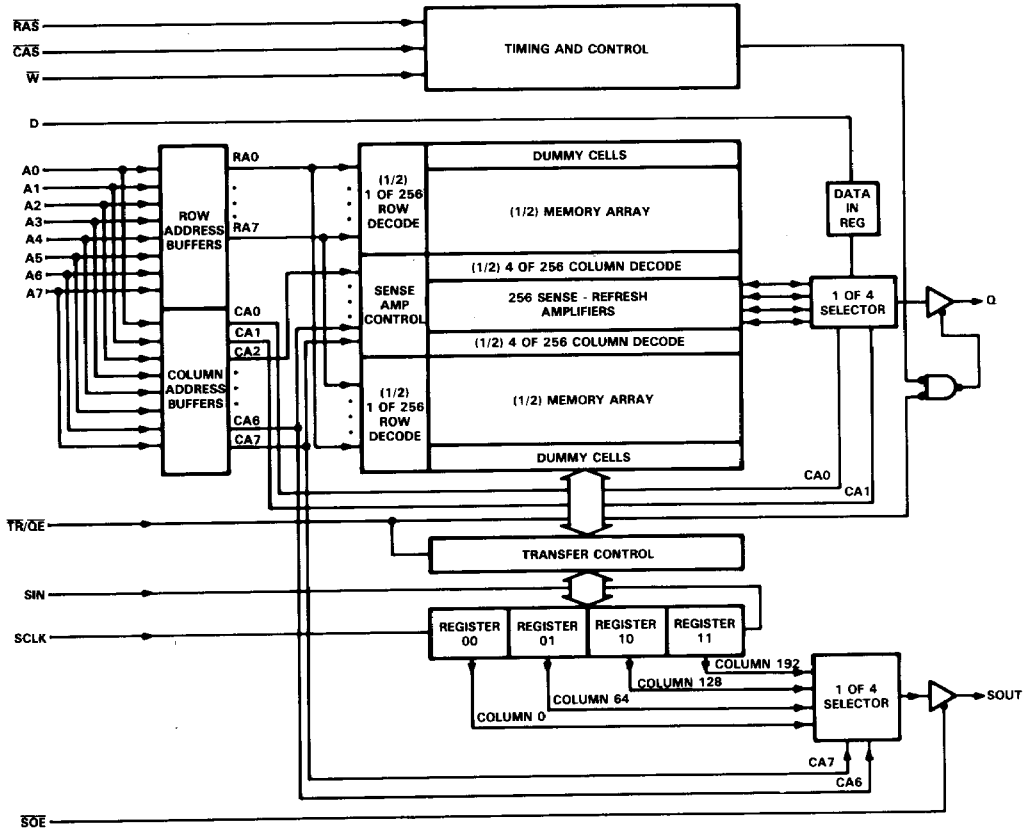
functional block diagram



5
Dynamic RAM Modules

TM4161EP5
65,536 BY 5-BIT MULTI-PORT VIDEO RAM MODULE

TMS4161 functional block diagram



5

Dynamic RAM Modules

random-access address space to sequential address space mapping

The TM4161EP5 is designed with each row divided into four, 64-column sections which map directly onto the four segments of each shift register (see TMS4161 functional block diagram). The first column section to be shifted out is selected by the two most-significant column-address bits. If the two bits represent binary 00, then one to four register segments can be shifted out in order. If the two bits represent binary 01, then only 1 to 3 (the most significant) register segments can be shifted out in order. If the two bits represent 10, then one to two of the most-significant register segments can be shifted out in order. Finally, if the two bits represent 11 only the most-significant register segment can be shifted out in order. All register segments are shifted out with the least-significant bit (bit 0) first and the most-significant bit (bit 63) last. Note that if the two column-address bits equal 00 during the last register transfer cycle ($\overline{\text{TR}}/\overline{\text{QE}}$ at logic level "0" as $\overline{\text{RAS}}$ falls) a total of 256 bits can be sequentially read out of each serial output pin.

random-access operation

$\overline{\text{TR}}/\overline{\text{QE}}$

The $\overline{\text{TR}}/\overline{\text{QE}}$ pin has two functions. First, it selects either register transfer or random-access operation as $\overline{\text{RAS}}$ falls, and second, during a random-access operation, it functions as an output enable after $\overline{\text{CAS}}$ falls.

To use the TM4161EP5 in the random-access mode, $\overline{\text{TR}}/\overline{\text{QE}}$ must be high as $\overline{\text{RAS}}$ falls. Holding $\overline{\text{TR}}/\overline{\text{QE}}$ high as $\overline{\text{RAS}}$ falls keeps the 256 elements of the shift registers disconnected from the corresponding 256 bit lines of the memory array. If data is to be shifted, the shift registers must be disconnected from the bit lines. Holding $\overline{\text{TR}}/\overline{\text{QE}}$ low as $\overline{\text{RAS}}$ falls enables the 256 switches that connect the shift registers to the bit lines and indicates that a transfer will occur between the shift registers and one of the memory rows.

During random-access operation, once $\overline{\text{CAS}}$ has been pulled low, $\overline{\text{TR}}/\overline{\text{QE}}$ controls when the data will appear at the Q output (if this is a read cycle). Whenever $\overline{\text{TR}}/\overline{\text{QE}}$ is held high during random-access operation, the Q output will be in the high-impedance state. This feature removes the possibility of an overlap between data on the address lines and data appearing on the Q output making it possible to connect the address lines to the Q and D lines (Use of this organization prohibits the use of the early write cycle.).

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{\text{RAS}}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{\text{CAS}}$). All addresses must be stable on or before the falling edges of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. $\overline{\text{RAS}}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{\text{CAS}}$ is used as a chip select activating the column decoder and the input and outputs buffers.

write enable ($\overline{\text{W}}$)

The read or write mode is selected through the write-enable ($\overline{\text{W}}$) input. A logic high on the $\overline{\text{W}}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data inputs are disabled when the read mode is selected. The common I/O feature of the TM4161EP5 dictates the use of early write cycles to prevent contention on DQ. When $\overline{\text{W}}$ goes low prior to $\overline{\text{CAS}}$, the data outputs will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data in (DQ1-DQ5)

Data is written during a write or read-modify-write cycle. The falling edge of $\overline{\text{CAS}}$ or $\overline{\text{W}}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{\text{W}}$ is brought low prior to $\overline{\text{CAS}}$ and the data is strobed in by $\overline{\text{CAS}}$ with setup and hold times referenced to this signal.

data out (DQ1-DQ5)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan out of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state as long as $\overline{\text{CAS}}$ or $\overline{\text{TR}}/\overline{\text{QE}}$ is held high. Data will not appear on the output until after both $\overline{\text{CAS}}$ and $\overline{\text{TR}}/\overline{\text{QE}}$ have been brought low. In a read cycle, the guaranteed maximum output enable access time is valid only if t_{CQE} is greater than $t_{\text{CQE MAX}}$, and t_{RLCL} is greater than $t_{\text{RLCL MAX}}$. Likewise, $t_{\text{a(C) MAX}}$ is valid only if t_{RLCL} is greater than $t_{\text{RLCL MAX}}$. Once the output is valid, it will remain valid while $\overline{\text{CAS}}$ and $\overline{\text{TR}}/\overline{\text{QE}}$ are both low; $\overline{\text{CAS}}$ or $\overline{\text{TR}}/\overline{\text{QE}}$ going high will return the output to a high-impedance state. In an early write cycle, the output is always in a high-impedance state. In a register transfer cycle, the output will always be in a high-impedance state.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in high-impedance state unless $\overline{\text{CAS}}$ is applied, the $\overline{\text{RAS}}$ -only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{\text{RAS}}$ causes all bits in each row to be refreshed. $\overline{\text{CAS}}$ can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the module. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on M1-M5, the row address and $\overline{\text{RAS}}$ are applied to multiple modules. $\overline{\text{CAS}}$ is then decoded to select the proper module.

power up

After power up, the power supply must remain at its steady-state value for 1 ms. In addition, $\overline{\text{RAS}}$ must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{\text{RAS}}$ cycles before proper device operation is achieved.

sequential-access operation

5

Dynamic RAM Modules

$\overline{\text{TR}}/\overline{\text{QE}}$

Memory transfer operations involving parallel use of the shift registers are first indicated by bringing $\overline{\text{TR}}/\overline{\text{QE}}$ low before $\overline{\text{RAS}}$ falls low. This enables the switches connecting the 256 elements of the shift registers to the 256 bit lines of the memory array. The $\overline{\text{W}}$ line determines whether the data will be transferred from or to the shift registers.

write enable ($\overline{\text{W}}$)

In the sequential-access mode, $\overline{\text{W}}$ determines whether a transfer will occur from the shift registers to the memory array, or from the memory array to the shift registers. To transfer from the shift registers to the memory array, $\overline{\text{W}}$ is held low as $\overline{\text{RAS}}$ falls, and, to transfer from the memory array to the shift registers, $\overline{\text{W}}$ is held high as $\overline{\text{RAS}}$ falls. Thus, reads and writes are always with respect to the memory array. The write setup and hold times are referenced to the falling edge of $\overline{\text{RAS}}$ for this mode of operation.

row address (A0 through A7)

Eight address bits are required to select one of the 256 possible rows involved in the transfer of data to or from the shift registers. A0-A7, $\overline{\text{W}}$, and $\overline{\text{TR}}/\overline{\text{QE}}$ are latched on the falling edge of $\overline{\text{RAS}}$.

register column address (A7, A6)

To select one of the four shift register segments within each shift register (transfer from memory to register only), the appropriate 2-bit column address (A7, A6) must be valid when $\overline{\text{CAS}}$ falls. However, the $\overline{\text{CAS}}$ and segment address signals need not be supplied every transfer cycle, only when it is desired to change or select a new segment.

SCLK

Data is shifted in and out on the rising edge of SCLK. This makes it possible to view each shift register as though it were made of 256 rising edge D flip-flops connected D to Q. The TM4161EP5 is designed to work with a wide range duty cycle clock to simplify system design. Note that data will appear at the SOUT pins not only on the rising edge of SCLK but also after an access time of $t_{a}(\text{RSO})$ from $\overline{\text{RAS}}$ high during a parallel load of the shift registers.

SIN and SOUT

Data is shifted in through the SIN pins and is shifted out through the SOUT pins. The TM4161EP5 is designed such that it requires 3 ns hold time on SIN as SCLK rises. SOUT is guaranteed not to change for at least

8 ns after SCLK rises. When loading data into the shift registers from the serial inputs in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times. To guarantee proper serial clock sequence after power up, a transfer cycle must be initiated before a serial data stream is applied at SIN.

SOE

The serial output enable pin controls the impedance of the serial outputs, allowing multiplexing of more than one bank of TM4161EP5 memories into the same external video circuitry. When SOE is at a logic low level, the SOUTs will be enabled and the proper data read out. When SOE is at a logic high level, the SOUTs will be disabled and be in the high-impedance state.

refresh

The shift registers are also dynamic storage elements. The data held in the registers will be lost unless SCLK goes high to shift the data one bit position, a transfer write operation is invoked, or the data is reloaded from the memory array. See specifications for maximum register data retention times. Important: If the shift registers have remained idle for a time period which exceeds the maximum SCLK high or SCLK low time, the dynamic clock circuits will lose charge. Under these conditions, the shift register clocks must be re-enabled by performing any transfer cycle before data can be shifted into or out of the shift registers.

single-in-line package and components

- PC substrate: 0.79 mm (0.031 inch) minimum thickness
- Bypass capacitors: Multilayer ceramic
- Leads: Tin/lead solder coated over phosphor-bronze

absolute maximum ratings over operating free-air temperature range (unless otherwise noted) †

| | |
|--|----------------|
| Voltage range on any pin except V _{DD} and data out (see Note 1) | -1.5 V to 10 V |
| Voltage range on V _{DD} supply and data out with respect to V _{SS} | -1 V to 6 V |
| Short circuit output current | 50 mA |
| Power dissipation | 5 W |
| Operating free-air temperature | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---|------|-----|----------------------|------|
| V _{DD} Supply voltage | 4.5 | 5 | 5.5 | V |
| V _{SS} Supply voltage | | 0 | | V |
| V _{IH} High-level input voltage | | 2.4 | V _{DD} +0.3 | V |
| V _{IL} Low-level input voltage (see Notes 2 and 3) | -0.6 | | 0.8 | V |
| T _A Operating free-air temperature | 0 | | 70 | °C |

- NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at -0.6 V; test conditions must comprehend this occurrence.
4. See application report entitled "TMS4164A and TMS4416 Input Protection Diode" on page 9-5.

TM4161EP5
65,536 BY 5-BIT MULTIPOINT VIDEO RAM MODULE

electrical characteristics over full range of recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TM4161EP5-15 | | | TM4161EP5-20 | | | UNIT | |
|-------------------------------|---|---|------|-----|--------------|------|-----|------|----|
| | | MIN | TYP† | MAX | MIN | TYP† | MAX | | |
| V _{OH} | High-level output voltage (DQ1-DQ5, SOUT1-SOUT5) | I _{OH} = -5 mA | | | 2.4 | | | V | |
| V _{OL} | Low-level output voltage (DQ1-DQ5, SOUT1-SOUT5) | I _{OL} = 4.2 mA | | | 0.4 | | | V | |
| I _I | Input current (leakage) | V _I = 0 V to 5.8 V, V _{DD} = 5 V, All other pins = 0 V | | | ± 10 | | | µA | |
| I _O | Output current (leakage) (DQ1-DQ5, SOUT1-SOUT5) | V _O = 0.4 V to 5.5 V, V _{DD} = 5 V | | | ± 10 | | | µA | |
| I _{DD1} | Average operating current during read or write cycle | t _c (rd) = minimum cycle time, TR/OE low after RAS falls,‡ SCLK and SIN low, SOE high, No load on DQ1-DQ5 and SOUT1-SOUT5 | | | 250 | 350 | 250 | 350 | mA |
| I _{DD2} [§] | Standby current | After 1 RAS cycle, RAS and CAS high, SCLK and SIN low, SOE high, No load on DQ1-DQ5 and SOUT1-SOUT5 | | | 80 | 100 | 80 | 100 | mA |
| I _{DD3} | Average refresh current | t _c (rd) = minimum cycle time, CAS high, RAS cycling, SCLK and SIN low, SOE high, TR/OE high, No load on DQ1-DQ5 and SOUT1-SOUT5 | | | 210 | 275 | 185 | 250 | mA |
| I _{DD4} | Average page-mode current | t _c (P) = minimum cycle time, RAS low, CAS cycling, TR/OE low after RAS falls, SCLK and SIN low, SOE high, No load on DQ1-DQ5 and SOUT1-SOUT5 | | | 225 | 275 | 200 | 250 | mA |
| I _{DD5} | Average shift register current (includes I _{DD2}) | RAS and CAS high, t _c (SCLK) = t _c (SCLK) min, No load on DQ1-DQ5 and SOUT1-SOUT5 | | | 150 | 200 | 150 | 200 | mA |
| I _{DD6} | Worst case average DRAM and shift register current | t _c (rd) = minimum cycle time, t _c (SCLK) = minimum cycle time, TR/OE low after RAS falls, No load on DQ1-DQ5 and SOUT1-SOUT5 | | | 425 | 475 | 400 | 450 | mA |

† All typical values are at T_A = 25°C and nominal supply voltages.

‡ See appropriate timing diagram.

§ V_{IL} > -0.6 V

15
Dynamic RAM Modules

capacitance over recommended supply voltage and operating free-air temperature range, $f = 1 \text{ MHz}$

| PARAMETER | | MAX | UNIT |
|-------------|--|-----|------|
| $C_i(A)$ | Input capacitance, address inputs | 35 | pF |
| $C_i(DQ)$ | Input capacitance, data inputs | 25 | |
| $C_i(RC)$ | Input capacitance, strobe inputs | 50 | |
| $C_i(W)$ | Input capacitance, write enable input | 50 | |
| $C_i(CK)$ | Input capacitance, serial clock | 50 | |
| $C_i(SI)$ | Input capacitance, serial in | 25 | |
| $C_i(SOE)$ | Input capacitance, serial output enable | 30 | |
| $C_i(TR)$ | Input capacitance, register transfer input | 35 | |
| $C_o(SOUT)$ | Output capacitance, serial out | 35 | |

† All typical values are at $T_A = 25^\circ\text{C}$ and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

| PARAMETER | TEST CONDITIONS† | ALT. SYMBOL | TM4161EP5-15 | | TM4161EP5-20 | | UNIT |
|-------------------------|---|--|--------------|-----|--------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| $t_a(C)$ | Access time from \overline{CAS} | $C_L = 100 \text{ pF}$ | t_{CAC} | 100 | | 135 | ns |
| $t_a(QE)$ | Access time of Q from $\overline{TR}/\overline{OE}$ low | $C_L = 100 \text{ pF}$ | | 40 | | 50 | |
| $t_a(R)$ | Access time from \overline{RAS} | $t_{RLCL} = \text{MAX},$ $C_L = 100 \text{ pF}$ | t_{RAC} | 150 | | 200 | |
| $t_a(RSO)$ | SOUT access time from \overline{RAS} high | $C_L = 30 \text{ pF}$ | | 65 | | 85 | |
| $t_a(SOE)$ | Access time from \overline{SOE} low to SOUT | $C_L = 30 \text{ pF}$ | | 30 | | 30 | |
| $t_a(SO)$ | Access time from SCLK | $C_L = 30 \text{ pF}$ | | 45 | | 50 | |
| $t_{dis}(CH)^\ddagger$ | Q output disable time from \overline{CAS} high | $C_L = 100 \text{ pF}$ | t_{OFF} | 40 | | 40 | |
| $t_{dis}(QE)^\ddagger$ | Q output disable time from $\overline{TR}/\overline{OE}$ high | $C_L = 100 \text{ pF}$ | | 40 | | 40 | |
| $t_{dis}(SOE)^\ddagger$ | Serial output disable time from \overline{SOE} high | $C_L = 30 \text{ pF}$ | | 30 | | 30 | |

† Figure 1 shows the load circuit.

‡ The maximum values for $t_{dis}(CH)$, $t_{dis}(QE)$, and $t_{dis}(SOE)$ define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL} .

TM4161EP5
65,536 BY 5-BIT MULTIPOINT VIDEO RAM MODULE

timing requirements over recommended supply voltage range and operating free-air temperature range

| | ALT. SYMBOL | TM4161EP5-15 | | TM4161EP5-20 | | UNIT |
|---|-------------|--------------|--------|--------------|--------|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{c(P)}$ Page-mode cycle time | t_{PC} | 160 | | 225 | | ns |
| $t_{c(rd)}$ Read cycle time [†] | t_{RC} | 240 | | 315 | | ns |
| $t_{c(W)}$ Write cycle time | t_{WC} | 240 | | 315 | | ns |
| $t_{c(TW)}$ Transfer write cycle time [‡] | | 240 | | 315 | | ns |
| $t_{c(Trd)}$ Transfer read cycle time | | 240 | | 315 | | ns |
| $t_{c(SCLK)}$ Serial-clock cycle time | t_{SCC} | 45 | 50,000 | 50 | 50,000 | ns |
| $t_{w(CH)}$ Pulse duration, \overline{CAS} high (precharge time) [§] | t_{CP} | 50 | | 80 | | ns |
| $t_{w(CL)}$ Pulse duration, \overline{CAS} low | t_{CAS} | 100 | 10,000 | 135 | 10,000 | ns |
| $t_{w(RH)}$ Pulse duration, \overline{RAS} high (precharge time) | t_{RP} | 80 | | 105 | | ns |
| $t_{w(RL)}$ Pulse duration, \overline{RAS} low | t_{RAS} | 150 | 10,000 | 200 | 10,000 | ns |
| $t_{w(W)}$ Write pulse duration | t_{WP} | 45 | | 45 | | ns |
| $t_{w(CKL)}$ Pulse duration, SCLK low | | 10 | | 10 | | ns |
| $t_{w(CKH)}$ Pulse duration, SCLK high | | 12 | | 12 | | ns |
| $t_{w(QE)}$ $\overline{TR}/\overline{OE}$ pulse duration low time (read cycle) | | 40 | | 40 | | ns |
| t_t Transition times (rise and fall) RAS, CAS, and SCLK | t_T | 3 | 50 | 3 | 50 | ns |
| $t_{su(CA)}$ Column-address setup time | t_{ASC} | 0 | | 0 | | ns |
| $t_{su(RA)}$ Row-address setup time | t_{ASR} | 0 | | 0 | | ns |
| $t_{su(RW)}$ \overline{W} setup time before \overline{RAS} low with $\overline{TR}/\overline{OE}$ low | | 0 | | 0 | | ns |
| $t_{su(D)}$ Data setup time | t_{DS} | 0 | | 0 | | ns |
| $t_{su(rd)}$ Read-command setup time | t_{RCS} | 0 | | 0 | | ns |
| $t_{su(WCL)}$ Early write-command setup time before \overline{CAS} low | t_{WCS} | -5 | | -5 | | ns |
| $t_{su(WCH)}$ Write-command setup time before \overline{CAS} high | t_{CWL} | 40 | | 60 | | ns |
| $t_{su(WRH)}$ Write-command setup time before \overline{RAS} high | t_{RWL} | 40 | | 60 | | ns |
| $t_{su(TR)}$ $\overline{TR}/\overline{OE}$ setup time before \overline{RAS} low | | 0 | | 0 | | ns |
| $t_{su(SI)}$ Serial-data setup time before SCLK high | | 6 | | 6 | | ns |
| $t_h(SI)$ Serial-data-in hold time after SCLK high | | 3 | | 3 | | ns |
| $t_h(CLCA)$ Column-address hold time after \overline{CAS} low | t_{CAH} | 45 | | 55 | | ns |
| $t_h(RA)$ Row-address hold time | t_{RAH} | 20 | | 25 | | ns |
| $t_h(RW)$ \overline{W} hold time after \overline{RAS} low with $\overline{TR}/\overline{OE}$ low | | 20 | | 20 | | ns |
| $t_h(RLCA)$ Column-address hold time after \overline{RAS} low | t_{AR} | 95 | | 120 | | ns |
| $t_h(CLD)$ Data hold time after \overline{CAS} low | t_{DH} | 60 | | 80 | | ns |
| $t_h(RLD)$ Data hold time after \overline{RAS} low | t_{DHR} | 110 | | 145 | | ns |
| $t_h(WLD)$ Data hold time after \overline{W} low | t_{DH} | 45 | | 55 | | ns |
| $t_h(CHrd)$ Read-command hold time after \overline{CAS} high | t_{RCH} | 0 | | 0 | | ns |

(Continued next page.)

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

[†]All cycle times assume $t_t = 5$ ns except $t_{c(SCLK)}$ which assumes $t_t = 3$ ns.

[‡]Multiple transfer write cycles require separation by either a 500-ns \overline{RAS} -precharge interval or any other active \overline{RAS} -cycle.

[§]Page-mode only.

5

Dynamic RAM Modules

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

| | ALT. SYMBOL | TM4161EP5-15 | | TM4161EP5-20 | | UNIT |
|---|-------------|--------------|--------|--------------|--------|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{h(RHrd)}$ Read-command hold time after \overline{RAS} high | t_{RH} | 5 | | 5 | | ns |
| $t_{h(CLW)}$ Write-command hold time after \overline{CAS} low | t_{WCH} | 60 | | 80 | | ns |
| $t_{h(RLW)}$ Write-command hold time after \overline{RAS} low | t_{WCR} | 110 | | 145 | | ns |
| $t_{h(RSO)}$ Serial-data-out hold time after \overline{RAS} low with $\overline{TR}/\overline{OE}$ low | | 30 | | 30 | | ns |
| $t_{h(SO)}$ Serial-data-out hold time after SCLK high | | 8 | | 8 | | ns |
| $t_{h(TR)}$ $\overline{TR}/\overline{OE}$ hold time after \overline{RAS} low (transfer) | | 20 | | 20 | | ns |
| t_{RLCH} Delay time, \overline{RAS} low to \overline{CAS} high | t_{CSH} | 150 | | 200 | | ns |
| t_{CHRL} Delay time, \overline{CAS} high to \overline{RAS} low | t_{CRP} | 0 | | 0 | | ns |
| t_{CLOEH} Delay time, \overline{CAS} low to \overline{OE} high | | 100 | | 135 | | ns |
| t_{CLRHL} Delay time, \overline{CAS} low to \overline{RAS} high | t_{RSH} | 100 | | 135 | | ns |
| t_{CQE} Delay time, \overline{CAS} low to \overline{OE} low (maximum value specified only to guarantee $t_a(QE)$ access time) | | | 60 | | 85 | ns |
| t_{RHSC} Delay time, \overline{RAS} high to SCLK high | | 80 | 50,000 | 80 | 50,000 | ns |
| t_{RLCL} Delay time, \overline{RAS} low to \overline{CAS} low (maximum value specified only to guarantee access time) | t_{RCD} | 25 | 50 | 30 | 65 | ns |
| t_{CKRL} Delay time, SCLK high before \overline{RAS} low with $\overline{TR}/\overline{OE}$ low [†] | | 10 | 50,000 | 10 | 50,000 | ns |
| $t_{rf(MA)}$ Refresh time interval, memory array | t_{REF1} | | 4 | | 4 | ms |
| $t_{rf(SR)}$ Refresh time interval, shift register [#] | t_{REF2} | | 50,000 | | 50,000 | ns |

NOTE 5: Timing measurements are made at the 10% and 90% points of input and clock transitions. In addition, V_{IL} max and V_{IH} min must be met at the 10% and 90% points.

[†]SCLK may be high or low during $t_{w(RL)}$, but there can not be any positive edge transitions on SCLK for a minimum of 10 ns prior to \overline{RAS} going low with $\overline{TR}/\overline{OE}$ low (i.e., before a transfer cycle).

[#]See "refresh" on page 5-9.

5
Dynamic RAM Modules

PARAMETER MEASUREMENT INFORMATION

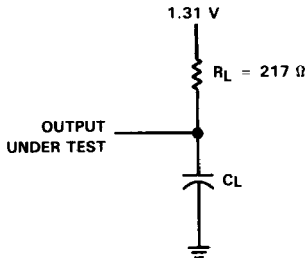
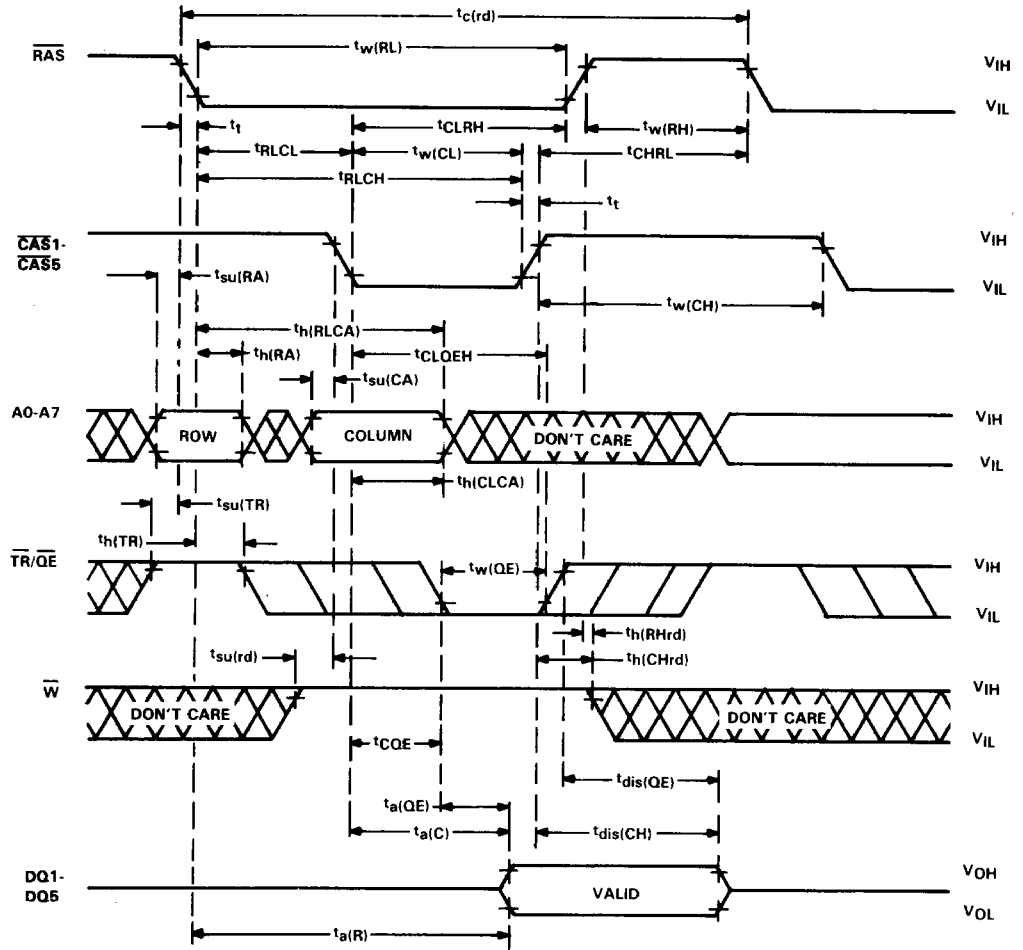


FIGURE 1. LOAD CIRCUIT

TM4161EP5
65,536 BY 5-BIT MULTIPORT VIDEO RAM MODULE

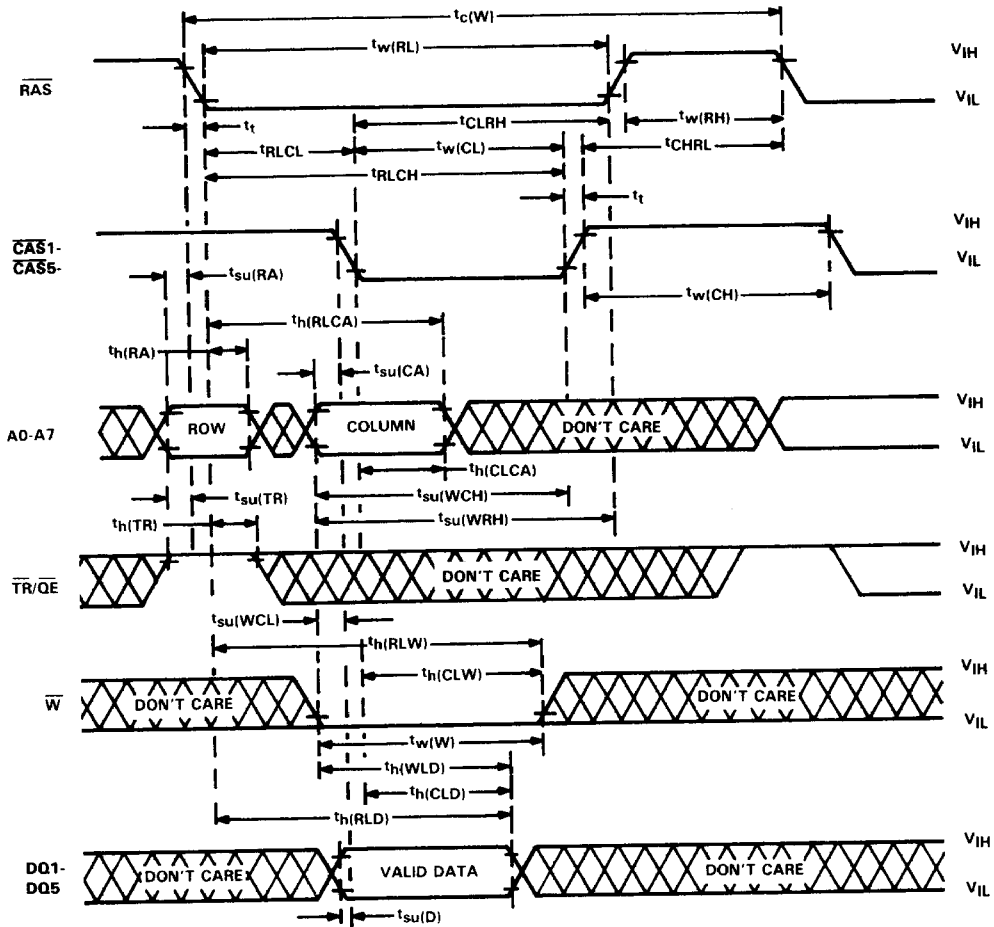
read cycle timing



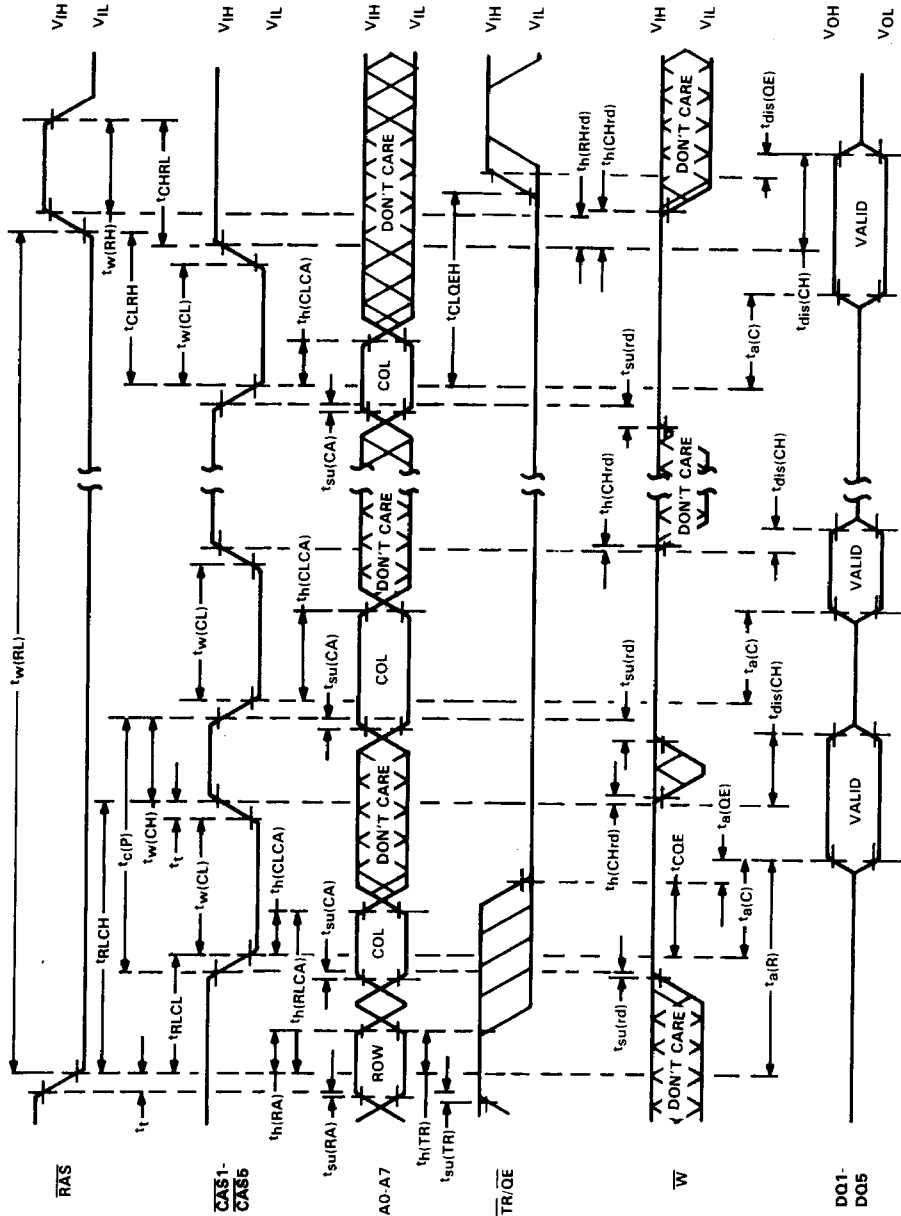
5

Dynamic RAM Modules

early write cycle timing

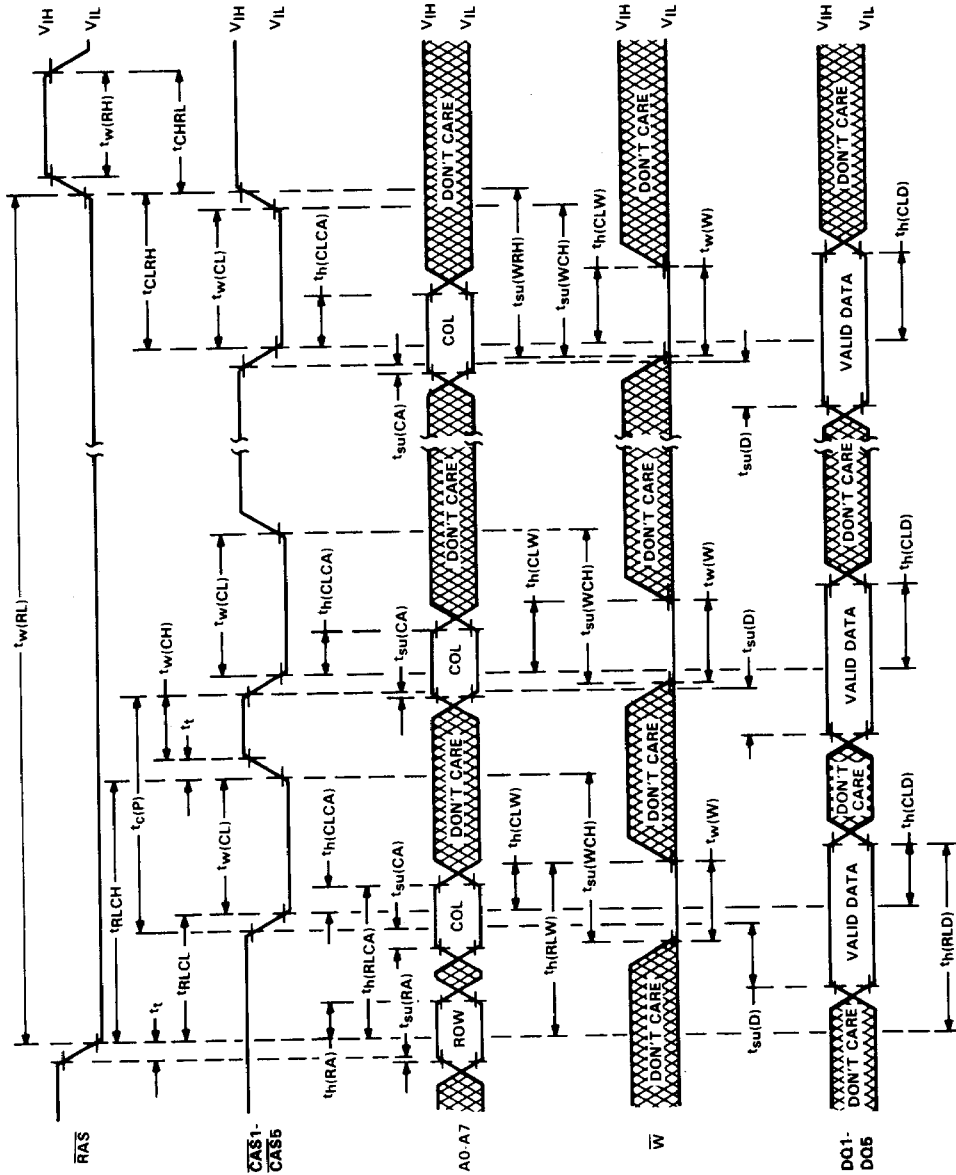


page-mode read cycle timing



NOTES: 6. Timing is for non-multiplexed DQ and address lines.
7. A write cycle or a read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

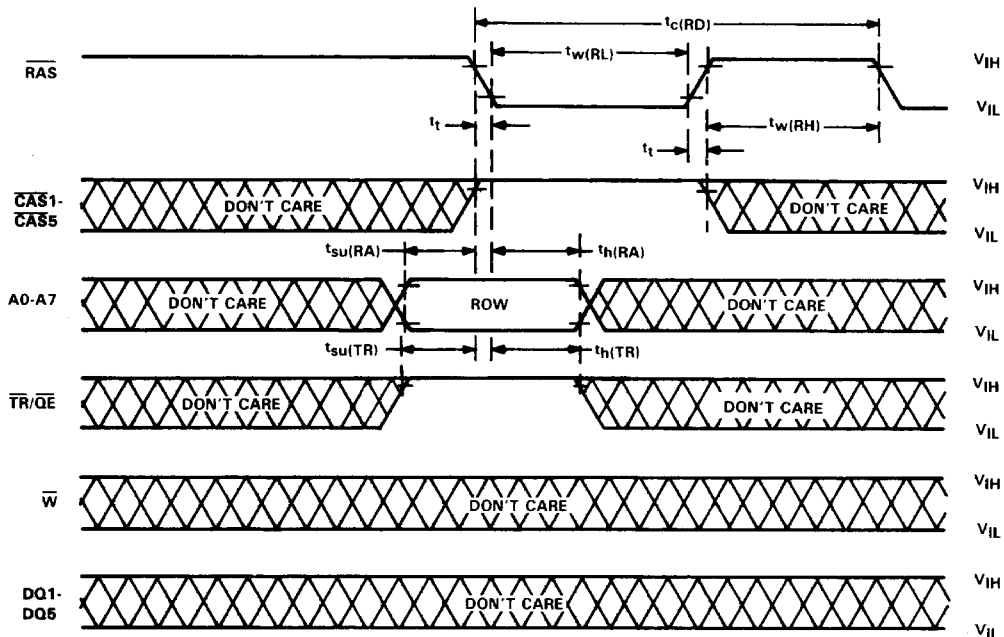
page-mode write cycle timing



NOTES: 6. Timing is for non-multiplexed DQ and address lines.
8. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as the read and read-modify-write timing specifications are not violated.

TM4161EP5
65,536 BY 5-BIT MULTIPORT VIDEO RAM MODULE

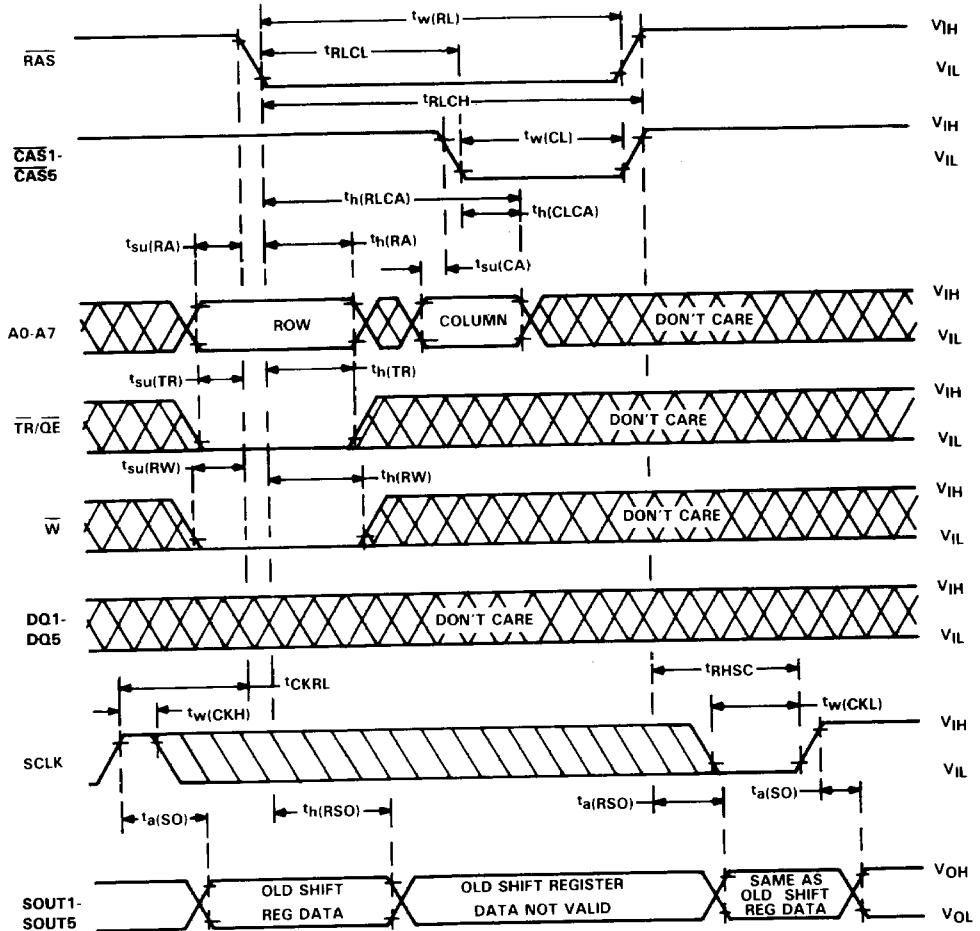
RAS-only refresh timing



5

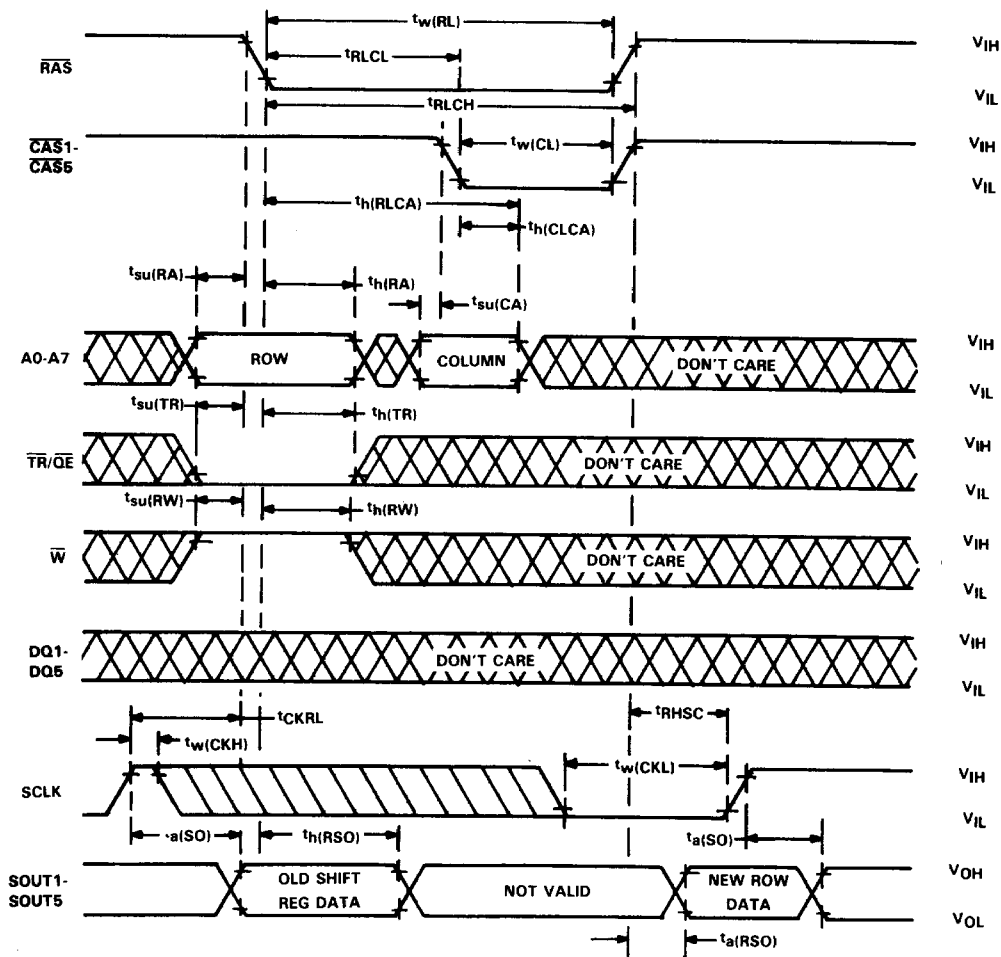
Dynamic RAM Modules

shift register to memory timing



- NOTES:
- The shift register to memory cycle is used to transfer data from the shift registers to the memory array. Every one of the 256 locations in each shift register is written into the 256 columns of the selected row. Note that the data that was in the shift registers may have resulted, either from a serial shift in or from a parallel load of the shift registers from one of the memory array rows.
 - \overline{SOE} assumed low.
 - SCLK may be high or low during $t_w(RL)$.

memory to shift register timing

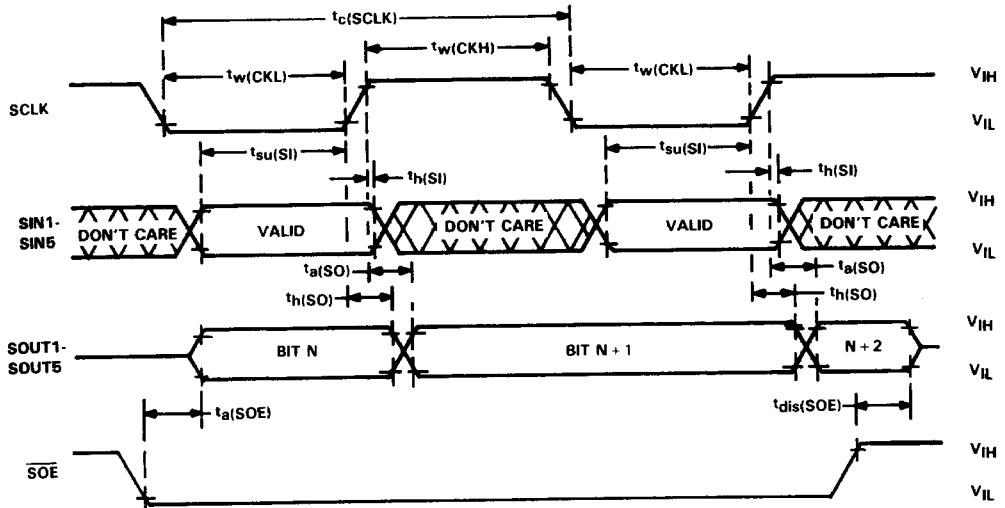


NOTES: 10. \overline{SOE} assumed low.

11. SCLK may be high or low during $t_w(RL)$.

12. The memory to shift register cycle is used to load the shift registers in parallel from the memory array. Every one of the 256 locations in each shift register are written into from the 256 columns of the selected row. Note that the data that is loaded into the shift registers may be either shifted out or written back into another row.

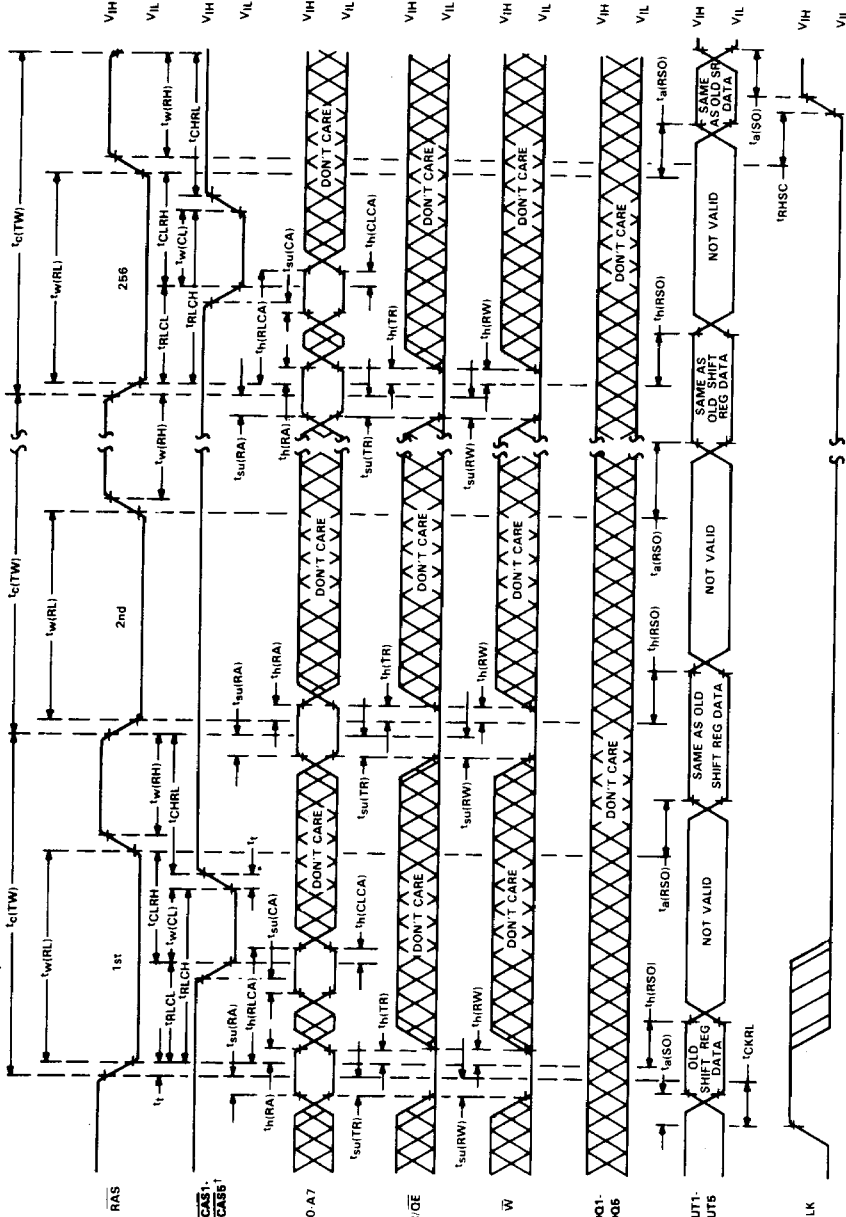
serial data shift timing



- NOTES: 13. When loading data into the shift registers from the serial input in preparation for a shift register to memory transfer operation, the serial clock must be clocked an even number of times.
14. While shifting data through the serial shift registers, the state of $\overline{TR}/\overline{QE}$ is a don't care as long as $\overline{TR}/\overline{QE}$ is held high when \overline{RAS} goes low and $t_{su}(TR)$ and $t_h(TR)$ timings are observed. This requirement avoids the initiation of a register-to-memory or memory-to-register data transfer operation. The serial data transfer cycle is used to shift data in and/or out of the shift registers.

TM4161EP5
65,536 BY 5-BIT MULTIPOINT VIDEO RAM MODULE

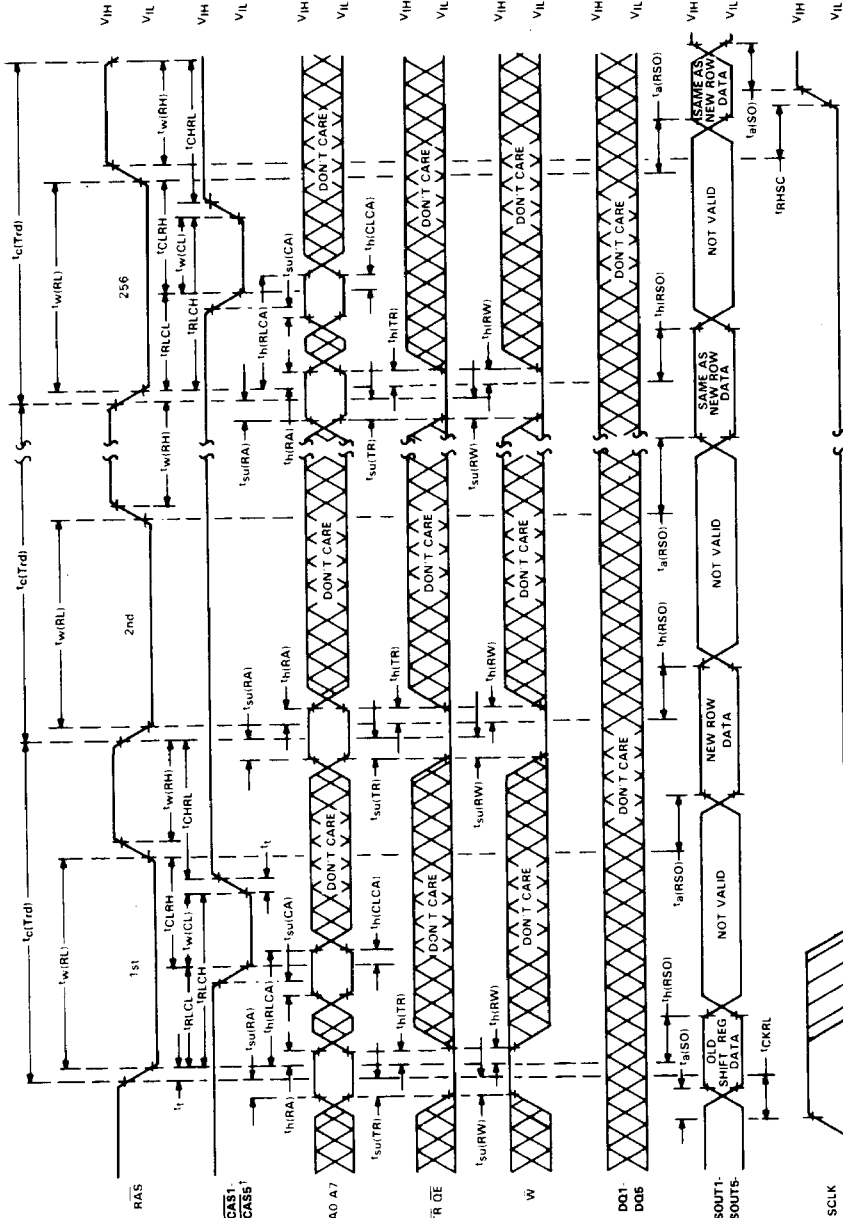
shift register to memory multiple timing



5
Dynamic RAM Modules

- [†]CAS and register address need not be supplied every cycle, only when it is desired to change or select a new register length.
 NOTES: 10. SOE assumed low.
 15. The shift register to memory multiple cycle is used to write the shift register data to more than one row of the memory array. An application of this could be clearing all memory. To do this, the SIN lines would be held at 0 to fill all locations in the shift registers with 0's. The shift registers would then be written into all 256 rows of the memory array in 256 cycles. The random output ports (DQ1-DQ6) will be in a high-impedance state as long as register transfer cycles are selected.
 16. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to t_{CKRL} falling with TR/QE low.

memory to shift register to memory multiple timing



t_{CAS} and register address need not be supplied every cycle, only when it is desired to change from one register address to another.

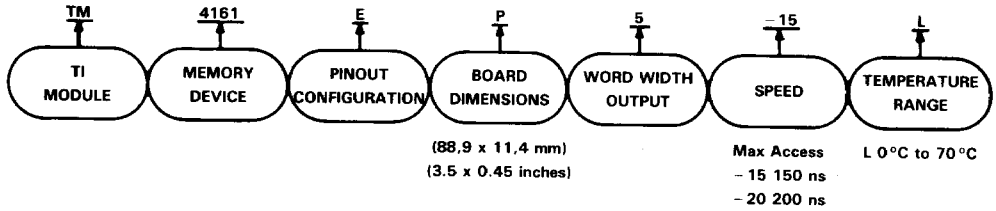
NOTES: 10. S_{OE} assumed low.

16. SCLK is a don't care except that no positive transitions on SCLK can occur for a period equal to t_{CKRL} prior to RAS falling with $\overline{TR}/\overline{DE}$ low.

17. The memory to shift register to memory multiple cycle is used to reorder the rows within the memory array itself. First, the data in a row is stored in the shift register and then it is written into other selected rows. The random output port Q will be in a high-impedance state as long as register transfer cycles are selected.

TM4161EP5
65,536 BY 5-BIT MULTIPOINT VIDEO RAM MODULE

TI single-in-line package nomenclature



5

Dynamic RAM Modules