M TC-20126

ATM Handler

Datasheet

Preliminary Information

Rev. 2 - Sept. 1998

Applications

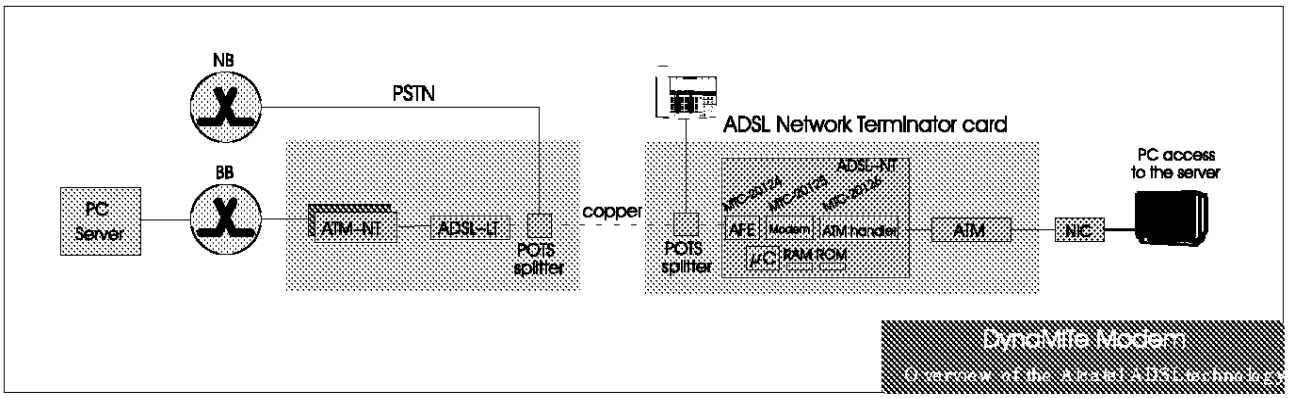
- Network termination unit or line termination unit for ATM based transport system
- Bidirectional ATM interface for xDSL modems.
- 25 Mbps internet access.
- Digital Home Network

Features

- Bidirectional ATM interface to/ from ADSL system (the interface carries ATM cell, but is treated as a byte stream by the rest of the ADSL system.
- Bidirectional ATM interface to/ from external ATM chips (two modes: I* or ATM 25 Mbps).
- Bidirectional V24 interface (two instances).
- Ancillary support functions e.g. general purpose registers linked to pins.

General Description

The MTC-20126 ASIC is designed as an ATM interface to a variety of variable data rata xDSL modems. It is configured by means of a microcontroller interface.
The configuration possibilities are numerous giving a certain flexibility in the use of The MTC-20126C is intended to be used both in a Network Terminating unit (NT) (referred to as the ATU-NT or ATU-R board) and in a Line Terminating unit (LT) (referred to as ATU-LT or ATU-C board), see. ATU-C / ATU-R stand for respectively ADSL Termination Unit on the Central Office side or on the Residential Subscriber side.
In the following text we will use the terms respectively ATU-LT and ATU-NT



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General Functional Description

Functional overview

The ADSL transport system makes use of the DMT-line code (Discrete Multi Tone) and is intended to support bidirectional digital data transmission over a single conventional twisted pair already in use for the analog POTS service.

In essence, the ADSL transport system is transparent to the format of the digital signal. However, an interface between the input/ output of the ADSL transport system and the input/ output digital data is needed to cope with the equipment specifications.

The present document contains the external specifications of the MTC-20126 ASIC, that incorporates this interface assuming ATM cell based transport on the ADSL transmission system. The functions to be performed by the ATM interface are essentially the same for the ATU-C (Central Office) and the ATU-R (Residential subscriber side), except that the transmit/ receive bit rates are different.

The maximum useful downstream and upstream bitrates depend upon the twisted-pair characteristics and to a lesser degree upon the break up into fast and slow data. Upper limits for useful Downstream (i.e. from Central Office towards Residential Subscriber) and Upstream (i.e. from Residential Subscriber towards Central Office) bitrates are respectively 6.784 Mbps and 640 kbps. In principle, all bitrates, that are smaller than the given maximum rate and are a multiple of the basic granularity, can be supported. The basic granularity depends upon the mode: the ADSL system is able to work in a 3 kHz or a 4.3125 kHz mode for the tone spacing.

The basic granularity is defined as 32 kbps for 4.3125 kHz tone spacing and 22.4 kbps for 3 kHz tone spacing. The variable bandwidth of the ADSL transmission path is not a problem for an ATM based interface because of ATM inherent support for arbitrary bitrates.

The MTC-20126 is able to terminate and generate up to two V24 connections. This facility is limited to the low level aspects, the rest of the processing is the microcontroller responsibility.

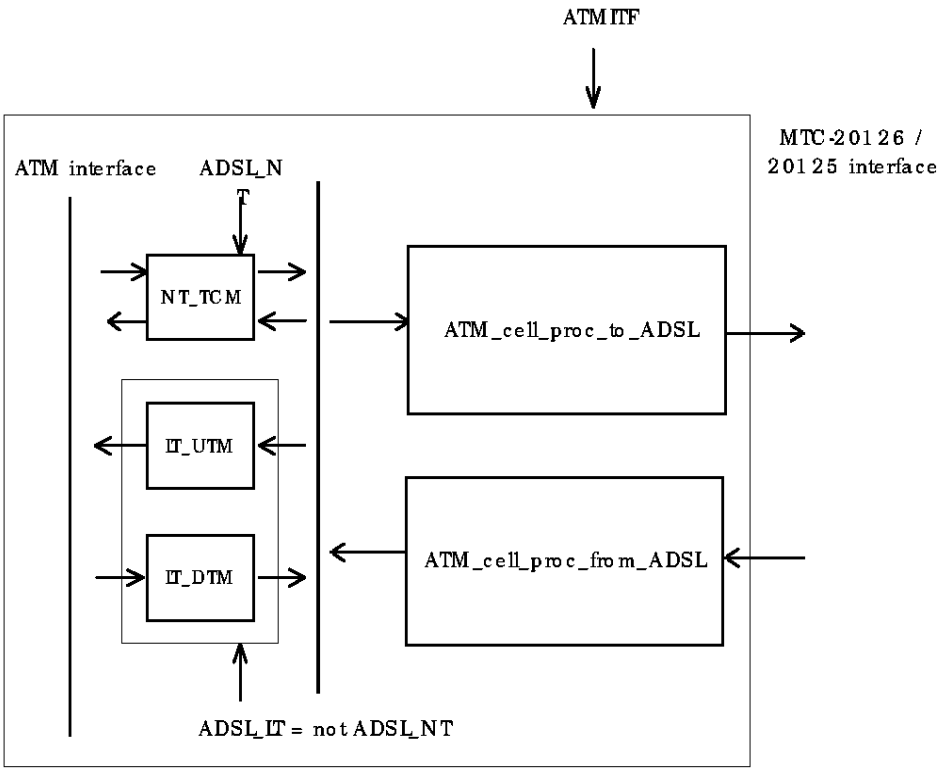
The MTC-20126 performs some low level support functions, essentially to decrease the amount of glue logic needed on the board, including:

- Watchdog timer;
- Address decoding;
- Wait state and recovery state;
- Interrupt grooming;
- Part of the reset logic;
- General purpose registers e.g. for LED driving, temperature sensing and general housekeeping.

Application

The MTC-20126 ASIC is intended to be used in both a Network Termination (NT) unit and in a Line Termination (LT) unit for ATM based transport systems on an ADSL transmission. The MTC-20126 may also be used for DHN* applications. A schematic view of the different modes of operation for the main data path (ADSL to/ from ATM) are shown later for applications using the I* mode / Utopia mode interface.

* Digital Home Network



High Level Model

The following figure presents a high level view of the MTC-20126, including the most important datapaths. This high level view is only used as a reference to support a structured presentation of the MTC-20126 functionality, the structure used by the implementation may differ.

The model is split in 2 different parts:

a) The upper part of the figure is related to ATM processing and is called the ADSL-ATM interface. It bidirectionally transports cells between two ATM interfaces. The first ATM interface is based on a parallel byte interface with an apparent ATM structure (explicit signals for cell delineation and idle), the other one goes to an ADSL or DHN transport system and is called the modem interface in this document.

b) The rest constitutes glue logic and support functions not directly part of any user datapath. The MTC-20126 is configured via the microcontroller interface, and the different control and maintenance datapaths use the extract and insert possibilities. The serial line controller and the glue logic increase the component integration allowing a reduction of the number of components on the board.

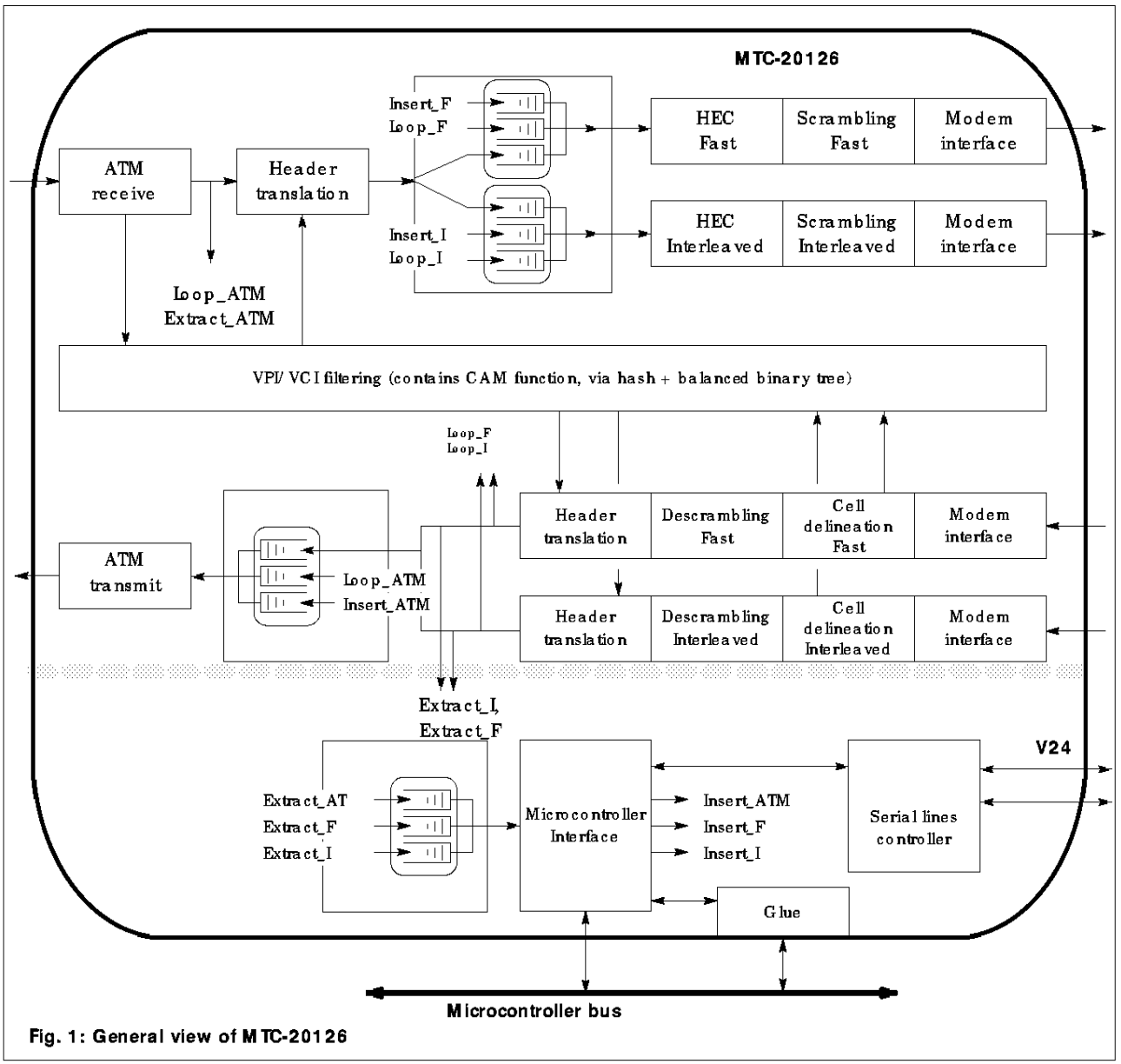


Fig. 1: General view of MTC-20126

Functional Description of the ADSL-ATM Interface

This part implements all functions related to ATM processing, up to the ATM layer itself. The following functional blocks are defined for the ATM-ADSL interface:

- ATM interface (I* or ATM 25 Mbps mode);
- ATM_cell_proc_to_ADSL;
- ATM_cell_proc_from_ADSL;
- VPI/VCI check;
- Ext_proc;
- Ins_proc;
- Modem interface (ADSL).

Each functional block is described in detail in the following sections.

The ADSL-ATM interface can be disabled (by clearing the ATMITF bit in the Component Configuration Register), in that case all the logic blocks described in this section become inactive. This also results in breaking most of the control and maintenance paths.

ATM cell procedure from ADSL Function

This function block accepts two data streams, one per modem interface. One data stream contains the Interleaved (data) traffic. The other data stream contains the Fast (data) traffic. Fast and Interleaved refer to two slightly different ways of transporting data on the ADSL link. Both traffic streams may operate at different frequencies, but the total traffic (Fast and Interleaved) will not exceed 8.2 Mbit/s for the ADSL application.

The Fast and Interleaved traffic are first treated separately, though the function blocks are similar. As described in the following paragraphs and depicted in Fig. 2, the functions are specified as working in series. In a first part the following functions are defined for both the Fast and Interleaved traffic:

- ATM cell delineation;
- ADSL link performance monitoring;
- HEC check;
- ATM payload descrambler;
- Idle cell filter;
- PLOAM extraction;
- Header translation.

Note that the interfaces of the Fast and Interleaved traffic are working independently, they have the same peak bandwidth, but the payload bitrates are independent.

Then, the cell traffic is multiplexed ('ATM cell mux' function) to a single ATM cell stream. Hereby, the information to which traffic a cell belongs (i.e. Fast or Interleaved) is kept with the cell.

According to the outcome of the context (Loopback, Inactive, Fast, Interleaved, Extract, Extract_PT and Pass_through) the following functions can be triggered:

- Forward cell to output buffer, normal operation;
- Drop Loopback;
- Drop Inactive;
- Extract ATM cell.

Forwarded cell (towards the output buffer) receive a new header also retrieved from the context table.

In the output buffer towards the ATM interface, cells can be inserted either from the INS_ISTAR_FIFO or from the Loopback buffer in addition to the normal datapath from the ADSL interface.

The ATM_cell_proc_from_ADSL function block provides only non-idle cells to the ATM interface (I* bus). In case the MTC-20126 is in Network termination mode, the ATM interface will provide an idle cell indication on the I* bus if necessary. In case the MTC-20126 is in Line termination mode, the ATM interface will not ask for access on the I* bus if no cell is available.

Notes:

- Additional indications (i.e. cell direction and Fast/Interleaved) are needed for an extracted PLOAM cell, as otherwise no distinction can be made to which traffic the PLOAM cell belonged. The header for PLOAM cells is the same for Fast and Interleaved traffic.
- As the cell streams from Fast and Interleaved traffic are merged, there cannot be made a distinction between cell header values from the Fast and Interleaved traffic.
- No payload scrambling is performed for ATM cells passed to the ATM interface (I* interface).

The context of the cell is retrieved by invoking the Virtual Path Identifier / Virtual Channel Identifier 'VPI/VCI check' function.

ATM cell procedure to ADSL Function

This function block accepts an ATM stream at its ATM interface (I* interface) and splits the ATM traffic in a so-called Fast and Interleaved parts, which are transmitted on a cell base to the ADSL interface.
The interface to the ADSL is byte based and the ATM cells are byte aligned. Both traffic streams can operate at different rates, but the total traffic (Fast and Interleaved) is limited. The Fast and Interleaved path of the ADSL interface are independent and bursty, the bursts may happen at any time. They don't have to follow cell boundaries.

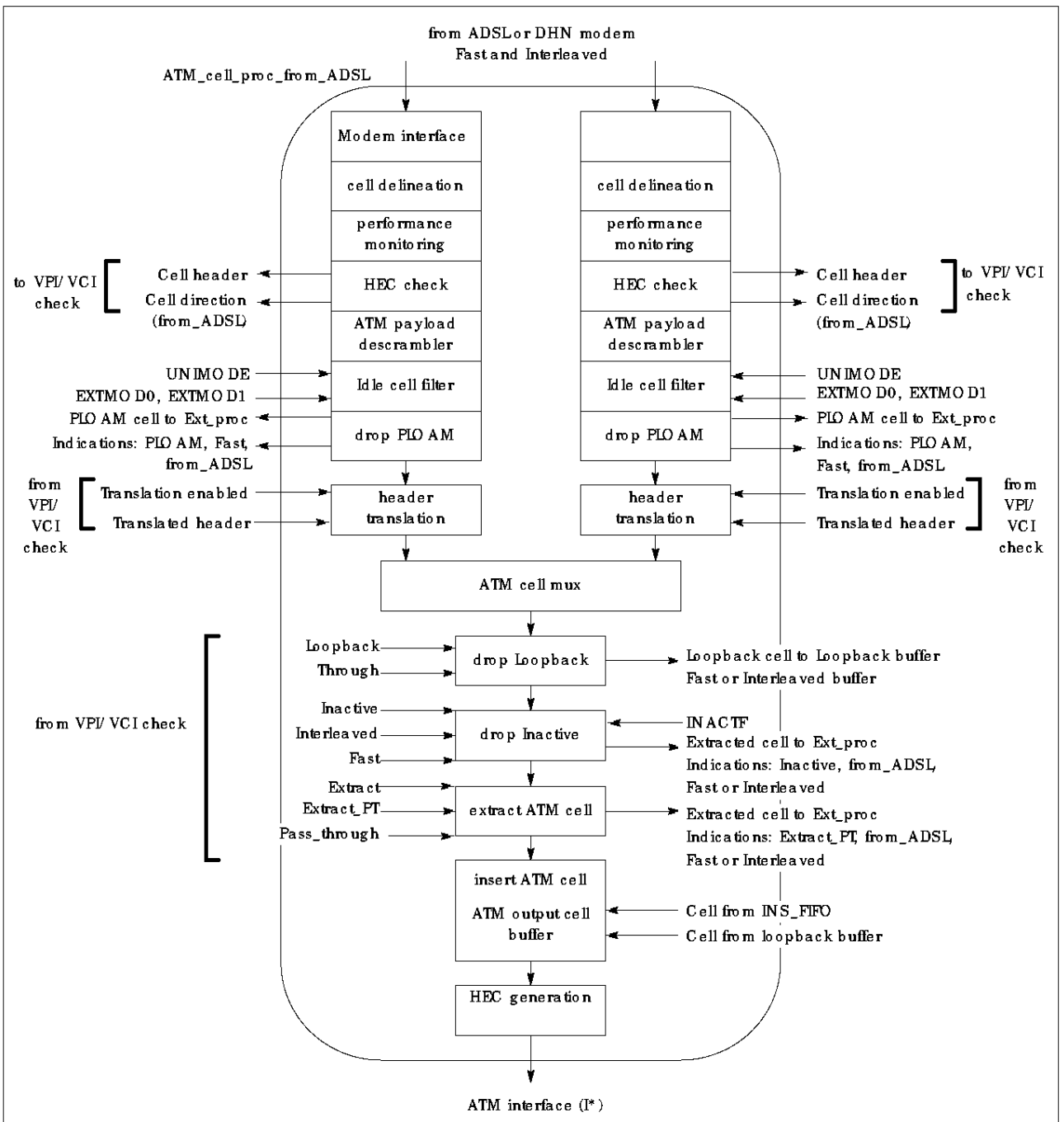


Fig. 2: Description of 'ATM_cell_proc_from_ADSL'

A cell clock is provided from the ATM interface, so that no cell delineation is necessary. The HEC will be checked for errors and the payload of the ATM cells received at the ATM interface is not scrambled.
Additionally, the ATM interface (I* bus) provides an indication for the idle cells. So, only non-idle cells are provided to the ATM_cell_proc_to_ADSL function. Therefore, the function block will not provide an idle cell filter.

Afterwards, the ATM cell header together with the cell direction 'to_ADSL' invokes the function 'VPI/ VCI check'. Consecutively, the functions drop Inactive, loopback and extract ATM cell are addressed. As described in the following paragraphs and shown in Fig. 3, the functions are specified as working in series, at least logically.
The implementation may differ in order as long as the final result is equivalent.

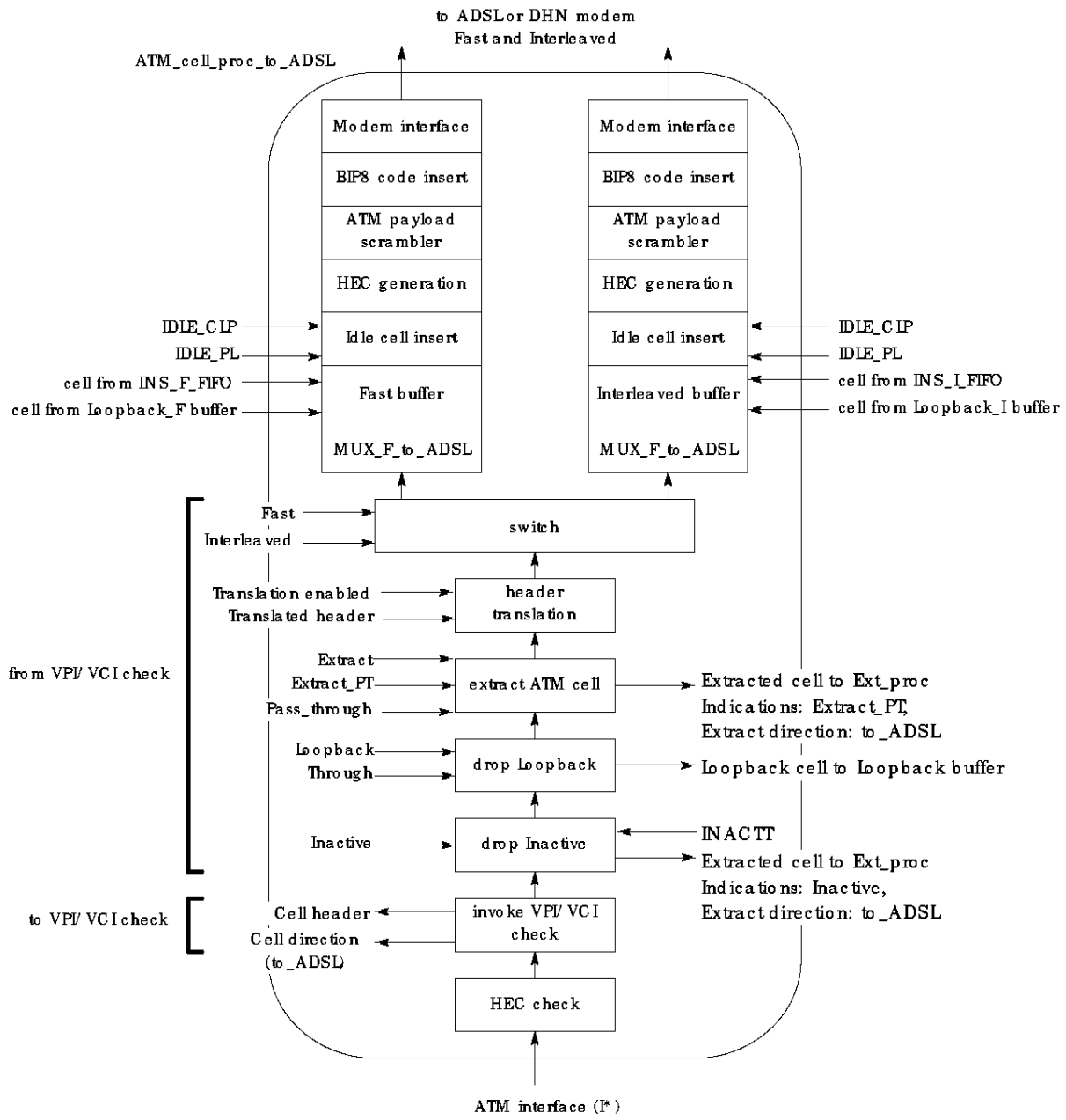


Fig. 3: Description of 'ATM cell procedure to ADSL'

Afterwards, the ATM cell is routed to the correct outgoing traffic (Fast or Interleaved) by taking the indications of the context into account. From that point on, the Fast and Interleaved traffic are considered independently. Cells are written in a Fast or Interleaved buffer, with the possibility to insert cells (from Ins_proc or Loopback_F/ Loopback_I buffer). To accommodate the outgoing cell rate, idle cells are inserted. A correct HEC is inserted and the ATM payload is scrambled. The final step is the optional addition of a BIP8 code.

Note: The interface of the Fast and Interleaved traffic is working independently and at a different rate.

Pin function and description

tbsbi	BS cell for bidirectional pin
tbscap	BS cell for fast input pin
tbsen	BS cell for pad enable signal (all I/O, OD, OS, OZ pins need to be controlled by an EN signal)

1. Pin Assignment of the MTC-20126

Table 1: Pin assignment of the MTC-20126

Pin		BS cell	Name	Function
no	Type	BS type		
1			NC	
2			NC	
3			NC	
4			VSS	Power 0 V
5			NC	
6	I	tbsin	ILIMAD[4]	I* LIM/ATMF AD4
7	I	tbsin	ILIMAD[3]	I* LIM/ATMF AD3
8	I	tbsin	ILIMAD[2]	I* LIM/ATMF AD2
9			VDD	Power 3.3 V
10	IOZ	tbsbi	ILIMAD[1]	I* LIM/ATMF AD1
11	IOZ	tbsbi	ILIMAD[0]	I* LIM/ATMF AD0
12	I	tbsin	notIUAAI	I* Upstream Access Arbitration
13	OD	tbsout	notIUOE	I* Upstream Output Enable
14			VSS	Power 0 V
15	OS	tbsout	IUAAO	I* Upstream Access Arbitration
16	I	tbsin	IBDCI	Board Daisy chain I/P
17	O	tbsout	IBDCO	Board Daisy chain O/P
18	I	tbsin	IUAF	I* Upstream Acces Flag
19			VDD	Power 3.3 V
20			NC	
21	IOZ	tbsbi	IDCUAS	I* Downstream Cell Sync
22	I	tbsin	IUCS	I* Upstream Cell Sync
23	O	tbsout	ICLKOUT	I* Buffered ICLKIN
24			VSS	Power 0 V
25	OZ	tbsout	ITXDATA[7]	I* TX Data bit 7
26	OZ	tbsout	ITXDATA[6]	I* TX Data bit 6
27	OZ	tbsout	ITXDATA[5]	I* TX Data bit 5
28	OZ	tbsout	ITXDATA[4]	I* TX Data bit 4
29			VDD	Power 3.3 V
30	OZ	tbsout	ITXDATA[3]	I* TX Data bit 3
31	OZ	tbsout	ITXDATA[2]	I* TX Data bit 2
32	OZ	tbsout	ITXDATA[1]	I* TX Data bit 1
33	OZ	tbsout	ITXDATA[0]	I* TX Data bit 0
34			VSS	Power 0 V
35	I	tbsin_s	IRXDATA[7]	I* RX Data bit 7
36	I	tbsin_s	IRXDATA[6]	I* RX Data bit 6
37	I	tbsin_s	IRXDATA[5]	I* RX Data bit 5
38	I	tbsin_s	IRXDATA[4]	I* RX Data bit 4
39			VDD	Power 3.3 V

Pin		BS cell	Name	Function
no	Type	BS type		
40	I	tbsin_s	IRXDATA[3]	I* RX Data bit 3
41	I	tbsin_s	IRXDATA[2]	I* RX Data bit 2
42	I	tbsin_s	IRXDATA[1]	I* RX Data bit 1
43	I	tbsin_s	IRXDATA[0]	I* RX Data bit 0
44			VSS	Power 0 V
45	I	tbscap	ICLKIN	I* Clock input
46	I	tbsin	ITFMODE	I* interface mode enable
47	I	tbsin	NTNOTLT	NT or LT mode select
48			NC	
49			VDD	Power 3.3 V
50			NC	
51			NC	
52			NC	
53			NC	
54			NC	
55			NC	
56			VSS	Power 0 V
57	IU		TMS	JTAG IEEE 1149.1
58	OZ		TDO	JTAG IEEE 1149.1
59	IU		TDI	JTAG IEEE 1149.1
60	IU		TCK	JTAG IEEE 1149.1
61			VDD	Power 3.3 V
62	ID		TRST	JTAG Reset
63	ISC	tbsin	notHARD_RESET	Reset pin
64	I	tbsin	SLR_DATA_F[1]	Modem I/F Rx F data 1
65	I	tbsin	SLR_DATA_F[0]	Modem I/F Rx F data 0
66			VSS	Power 0 V
67	I	tbsin	SLR_VAL_F	Modem I/F F valid indication
68	I	tbsin	SLR_DATA_I[1]	Modem I/F Rx I data 1
69	I	tbsin	SLR_DATA_I[0]	Modem I/F Rx I data 0
70	I	tbsin	SLR_VAL_I	Modem I/F I valid indication
71			VDD	Power 3.3 V
72	O		SLT_DATA_F[1]	Modem I/F Tx F data 1
73	O		SLT_DATA_F[0]	Modem I/F Tx F data 0
74	I	tbsin	SLT_REQ_F	Modem I/F F Byte request
75	O		SLT_DATA_I[1]	Modem I/F Tx I data 1
76			VSS	Power 0 V
77	O		SLT_DATA_I[0]	Modem I/F Tx I data 0
78	I	tbsin	SLT_REQ_I	Modem I/F I Byte request
79	I	tbsin	SIN[0]	UART input stream 0

Pin		BS cell	Name	Function
no	Type	BS type		
80	I	tbsin	STB_OK[0]	UART signal quality 0
81			VDD	Power 3.3 V
82	I	tbsin	ACT_MONN[0]	General input 0
83	O	tbsout	SOUT[0]	UART output stream 0
84	I	tbsin	SIN[1]	UART input stream 1
85	I	tbsin	STB_OK[1]	UART signal quality 1
86			VSS	Power 0 V
87	I	tbsin	ACT_MONN[1]	General input 1
88	O	tbsout	SOUT[1]	UART output stream 1
89	I	tbsin	INV_IN[1]	Inventory input 1
90	I	tbsin	INV_IN[0]	Inventory input 0
91			VDD	Power 3.3 V
92	OD	tbsout	INV_OUT[3]	Inventory output 3
93	OD	tbsout	INV_OUT[2]	Inventory output 2
94	OD	tbsout	INV_OUT[1]	Inventory output 1
95	OD	tbsout	INV_OUT[0]	Inventory output 0
96			VSS	Power 0 V
97	O	tbsout	notBOARD_RESET[3]	Reset signal output 3
98	O	tbsout	notBOARD_RESET[2]	Reset signal output 2
99	O	tbsout	notBOARD_RESET[1]	Reset signal output 1
100	O	tbsout	notBOARD_RESET[0]	Reset signal output 0
101			VDD	Power 3.3 V
102			NC	
103			NC	
104			NC	
105			NC	
106			NC	
107			NC	
108			VSS	Power 0 V
109	O	tbsout_s	LED[7]	Led driver output 7
110	O	tbsout_s	LED[6]	Led driver output 6
111	O	tbsout_s	LED[5]	Led driver output 5
112	O	tbsout_s	LED[4]	Led driver output 4
113			VDD	Power 3.3 V
114	O	tbsout_s	LED[3]	Led driver output 3
115	O	tbsout_s	LED[2]	Led driver output 2
116	O	tbsout_s	LED[1]	Led driver output 1
117	O	tbsout_s	LED[0]	Led driver output 0
118			VSS	Power 0 V
119	O	tbsout	notEPROM_WE[3]	Eprom write enable 3

Pin		BS cell	Name	Function
no	Type	BS type		
120	O	tbsout	notEPROM_WE[2]	Eprom write enable 2
121	O	tbsout	notEPROM_WE[1]	Eprom write enable 1
122	O	tbsout	notEPROM_WE[0]	Eprom write enable 0
123			VDD	Power 3.3 V
124	O	tbsout	notCS[7]	Chip select 7
125	O	tbsout	notCS[6]	Chip select 6
126	O	tbsout	notCS[5]	Chip select 5
127	O	tbsout	notCS[4]	Chip select 4
128			VSS	Power 0 V
129	O	tbsout	notCS[3]	Chip select 3
130	O	tbsout	notCS[2]	Chip select 2
131	O	tbsout	notMEM_OE	Memory output enable
132	O	tbsout	MUXCTL	DRAM mux control
133			VDD	Power 3.3 V
134	O	tbsout	notCAS[3]	Column Address Strobe 3
135	O	tbsout	notCAS[2]	Column Address Strobe 2
136	O	tbsout	notCAS[1]	Column Address Strobe 1
137	O	tbsout	notCAS[0]	Column Address Strobe 0
138			VSS	Power 0 V
139	O	tbsout	notRAS[1]	Row Address Strobe 1
140	O	tbsout	notRAS[0]	Row Address Strobe 0
141	O	tbsout	notDRAM_WE	DRAM Write Enable
142	I	tbsin	notBLAST	Burst Last
143			VDD	Power 3.3 V
144	I	tbsin	notADS	Address Data Strobe
145	I	tbsin	W / notR	Write / Read
146	IOD	tbsbi	notRDYRCV	Ready / Recover
147			NC	
148			VSS	Power 0 V
149	O	tbsout	notWDTO	Watchdog timer output
150	ISC	tbsin	TEMP	Temperature Signal
151			NC	
152	I	tbsin	notBE[3]	Byte Enable 3
153			VDD	Power 3.3 V
154			NC	
155			NC	
156			NC	
157			NC	
158			NC	
159			NC	

Pin		BS cell	Name	Function
no	Type	BS type		
160			VSS	Power 0 V
161	I	tbsin	notBE[2]	Byte Enable 2
162	I	tbsin	notBE[1]	Byte Enable 1
163	I	tbsin	notBE[0]	Byte Enable 0
164	I	tbsin	AD[18]	Address / Data bit18
165			VDD	Power3.3 V
166	I	tbsin	AD[19]	Address / Data bit19
167	I	tbsin	AD[20]	Address / Data bit20
168	I	tbsin	AD[21]	Address / Data bit21
169	I	tbsin	AD[22]	Address / Data bit22
170			VSS	Power 0 V
171	I	tbsin	AD[29]	Address / Data bit29
172	I	tbsin	AD[30]	Address / Data bit30
173	I	tbsin	AD[31]	Address / Data bit31
174	I	tbscap	PCLK	Master Processor clock
175			VDD	Power3.3 V
176	IO	tbsbi	AD[0]	Address / Data bit0
177	IO	tbsbi	AD[1]	Address / Data bit1
178	IO	tbsbi	AD[2]	Address / Data bit2
179	IO	tbsbi	AD[3]	Address / Data bit3
180			VSS	Power 0 V
181	I	tbscap	MASTER_CLK	System Master clock
182			VDD	Power3.3 V
183	ID	tbsin	SLF_TST_RAM	Ram self test
184	ID	tbsin	SCAN_EN	Enable scan test
185			VDD	Power3.3 V
186	IO	tbsbi	AD[4]	Address / Data bit4
187	IO	tbsbi	AD[5]	Address / Data bit5
188	IO	tbsbi	AD[6]	Address / Data bit6
189	IO	tbsbi	AD[7]	Address / Data bit7
190			VSS	Power 0 V
191	I	tbsin	AD[8]	Address / Data bit8
192	I	tbsin	AD[9]	Address / Data bit9
193	I	tbsin	AD[10]	Address / Data bit10
194	I	tbsin	AD[11]	Address / Data bit11
195			VDD	Power3.3 V
196	I	tbsin	notWR	Write enable
197	I	tbsin	notRD	Read enable
198	I	tbsin	ALE	Address Latch Enable
199	OD	tbsout	notInterrupt	Interrupt request O/P

Pin		BS cell	Name	Function
no	Type	BS type		
200			VSS	Power 0 V
201	OZ	tbsout	RDY	Ready
202	I	tbsin	EXT_INT	External int request I/P
203	I	tbsin	CID[1]	Chip id 1
204	I	tbsin	CID[0]	Chip id 0
205			VDD	Power 3.3 V
206	I	tbsin	notCS	Chip Select
207			NC	
208			NC	

MTC-20126 Device Layout

Fig. 4 shows the pin assignment of the MTC-20126.

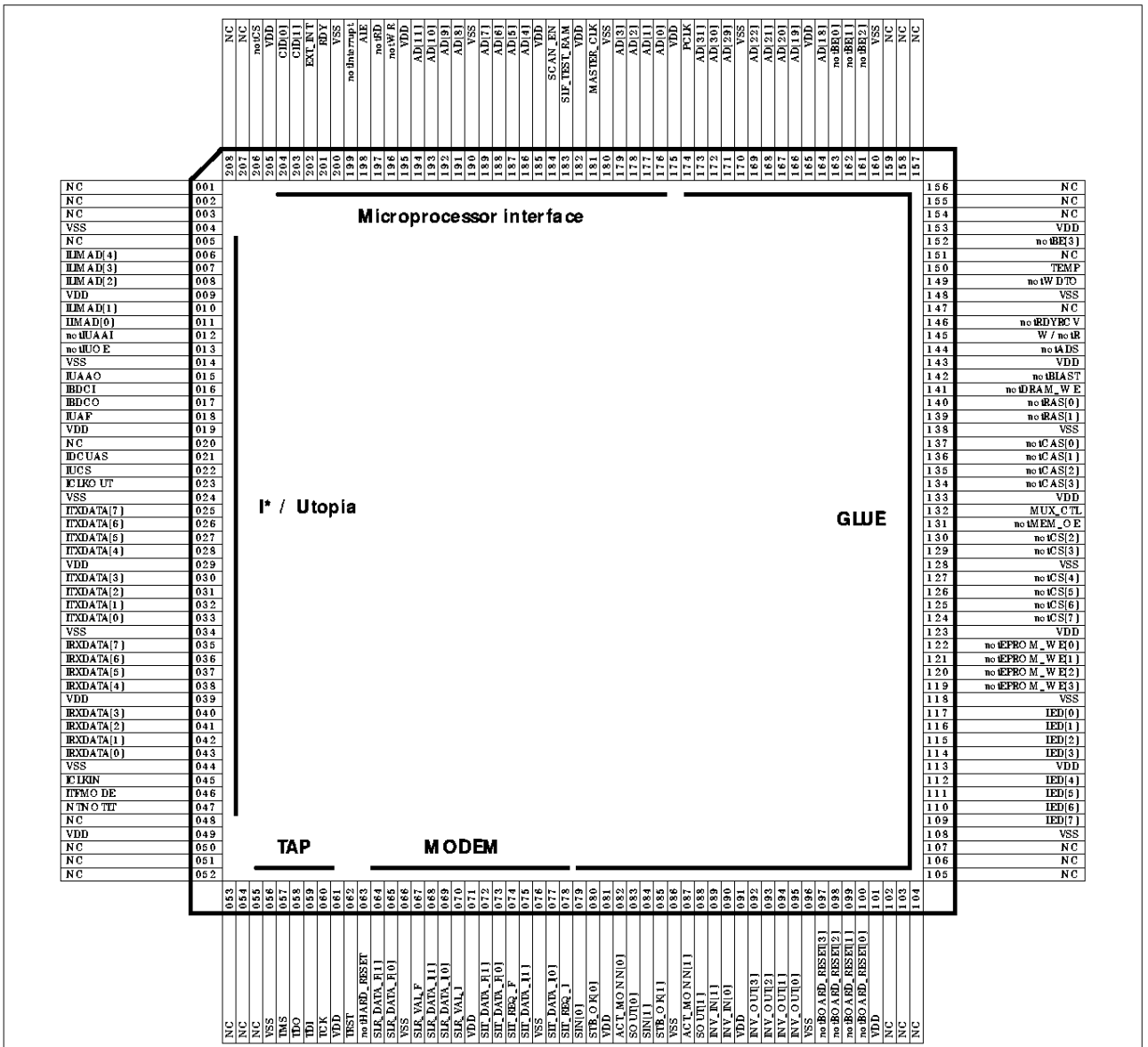


Fig. 4: MTC-20126 pin layout

Electrical, Physical and Environmental Characteristics

Maximum Ratings

Absolute maximum ratings are those parameter limits above which permanent damage to the integrated circuit may occur. It is not allowed to apply more than one of these conditions simultaneously.

Table 2: Maximum Ratings

Absolute maximum ratings						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{DD} to V_{SS}	Supply voltage	All voltages are referenced to V_{SS}	-0.4		5	V
V_{IN}	Input voltage		-0.5		V_{DD} +0.5	V
V_{OUT}	Output voltage		-0.5		V_{DD} +0.5	V
I	DC current drain per I/O pin				50	mA
I	DC current drain V_{DD} / V_{SS} pin				75	mA
T_{stg}	Storage temperature		-65		150	°C
T_L	Soldering lead temperature	10 seconds soldering			300	°C

Transient Energy Capabilities

ESD

The MTC-20126 is compliant with the ALCATEL standard 1AB 00000 0043 QTZZA, with a limit voltage of 1500 V, and with ALCATEL standard 1AB 00000 0044 QTZZA, with a limit voltage of 250 V.

1.1. Latch-up

The MTC-20126 is compliant with the ALCATEL standard 1AB 00000 0046 QTZZA, with a limit current of 100 mA.

Recommended Operating Conditions

Table 3: Operating Conditions

Recommended Operating Conditions						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{DD} to V_{SS}	Supply voltage		3.15	3.3	3.45	V
V_{IN}, V_{OUT}	Input voltage, Output voltage		V_{SS}		V_{DD}	V
T_J	Junction temperature		-25	85 †	110	°C
T_A	Ambient temperature		-25		85	°C
P_D	Power dissipation	See below			1	W

CMOS Input/Output Generic Characteristics

All outputs on the MTC-20126 are CMOS-compatible.

All inputs on the MTC-20126 are CMOS-compatible, except where otherwise stated.

The values presented in the following table apply for all CMOS inputs and/or outputs unless specified otherwise.

Table 4: CMOS IO buffer generic characteristics

DC Electrical Characteristics V_{SS} = 3.3 V ± 5% All voltages are referenced to V_{SS}, unless otherwise specified, positive current is towards the device						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	High level input voltage		0.7 * V_{DD}			V
V_{IL}	Low level input voltage				0.3 * V_{DD}	V
V_{OH}	High level output voltage	I_{OUT} = -4 mA	V_{DD}- 0.5			V
V_{OL}	Low level output voltage	I_{OUT} = 4 mA			0.5	V
I_{IN}	Input leakage current	V_{IN} = V_{SS}, V_{DD}	-10		10	µA
I_{OZ}	Tristate leakage current	V_{IN} = V_{SS}, V_{DD}	-10		10	µA
C_{IN}	Input capacitance	@ f = 1 MHz			5	pF
I_{OLD}	Dynamic output current	V_{OLD} = 2.3 V	-80			mA
I_{OHD}		V_{OHD} = 1 V	80			mA
C_{OUT}	Output capacitance (also bidirectional and tristate drivers)	@ f = 1 MHz			7	pF

Mechanical Data

The device is housed in a 208 pins Quad-Flat Package compliant with the Alcatel specifications PB026a 3/96 Package Handbook. Looking at the package with cavity facing up and the marked corner in the upper left corner, pin 1 is located on the top of the left side; pin numbers increase counter-clock wise.

2. Quality Insurance and Reliability

Inspection Requirements

Integrated circuits supplied to ALCATEL shall be subjected to and shall pass the Qualification Approval, Quality Conformance and Inspection Test Requirements detailed in the ALCATEL standards:

- 1 AB 00000 0014 QSZZA IC, qualification and quality conformance test specification;
- 1 AB 00000 0022 ASZZA General Requirements for the supply and inspection of component;
- 1 AB 00000 0085 ASZZA Technology Reliability Requirements;

if not specified in more detail in other agreed documents.

Device Life Requirements

The life requirements for this component is 25 years under benign conditions (75% RH average, 90% RH for max. 30 days per year, ambient temperature T=40 °C average, T=70 °C maximum, 60% confidence level).

The failure rate shall be:

a) up to 3000 h operation $\leq$0.2%;

b) from 3000 h to 25 years operation $\leq 200\ 10^{-9}$ failures/comph.

3. Physical Interfaces

Legend used throughout this chapter:

I	=	normal Input
IU	=	Input with pull-up resistance
ID	=	Input with pull-down resistance
O	=	normal output (only tri-state for test purposes)
OZ	=	tristatable output
O-OD	=	Open Drain Output
O-OS	=	Open Source Output
IO	=	input / output
IO-PU	=	input / Tri-state Push-pull output with pull-up resistance
IO-OD	=	Input / Open Drain Output
ISC	=	Schmitt Trigger Input (for reset)
BS cell	=	Boundary-Scan cell I = Input cell O = Output cell B = Bidirectional cell C = Capture cell

All outputs use CMOS levels.

All inputs use CMOS levels, except where otherwise stated.

Note: All ports that do not transport useful data will be put at a constant level (either 'high' or 'low').

I*-bus Interface

Pins & Functional Description

All I* inputs use TTL levels.

Table 5: General I* interface signals

Name	Type	Function
ICLKIN	I	Clock for I* bus operation
ICLKOUT	O	Buffered version of ICLKIN
IUMAD[4:2]	I	IUM ADdress, the pins have another meaning when the ATM 25 Mbps mode is used. IUMAD[1:0] output buffers are disabled when in I* mode.
IUMAD[1:0]	IOZ	
ITFMODE	I	Interface mode (high level = I* interface enabled)
NTnotLT	I	Enables/disables Network Termination mode

Table 6: Receive and transmit pins

Name	Type	Function
IRXDATA[7:0]	I	Receive Data Bus
ITXDATA[7:0]	OZ	Transmit Data Bus

Table 7: Access pins

Name	Type	Function
IUCS	I	Upstream Cell Synchronization
IDC/UAS	IOZ	Downstream Cell Synchronization and idle cell indication/ Upstream Access Start
IUAF	I	Upstream Access Flag Input, also used for ULAA signal
notIUAAI	I	Upstream Access Arbitration, input
IUAAO	OS	Upstream Access Arbitration, output
notIUOE	OD	Upstream Output Enable (active low)
IBDCI	I	Board Daisy Chain, input
IBDCO	O	Board Daisy Chain, output

Depending on the mode of operation on the I² bus (either LT or NT mode), the pinning on the I² interface have different signal definition.

The correspondence with the I² specification definition of the paragraph 'The ATM interface (I² interface)' is provided in the following table:

Table 8: Signal definition for the NT or LT mode of the MTC-20126

MTC-20126 in LT mode	Type	MTC-20126 in NT mode	Type	MTC-20126 pinning	Type
Receive					
IDDATA[7:0]	I	IUDATA[7:0]	I	IRXDATA[7:0]	I
Transmit					
IUDATA[7:0]	O	IDDATA[7:0]	O	ITXDATA[7:0]	O
Access					
IUCS	I	IUCS	I	IUCS	I
IDC/UAS	I	IDC/UAS	O	IDC/UAS	IO
IULAA	I	IUAF	I	IUAF	I
notIUAAI	I	--		notIUAAI	I
IUAAO	OS	--		IUAAO	OS
notIUOE	OD	--		notIUOE	OD
General					
ILIMAD[4:0]	I	--		ILIMAD[4:0]	I

Modem Interface

There are two modem interfaces, one for the Fast, the other for the Interleaved streams.

Pins & Functional Description

Table 9: Stream to modem

Name	Type	Function
SIT_DATA_I,F[1:0]	O	Modem data out, I & F
SIT_REQ_I,F	I	Modem out Byte Request, I & F

Table 10: Stream from modem

Name	Type	Function
SIR_DATA_I,F[1:0]	I	Modem data in, I & F
SIR_VAL_I,F	I	Modem data in valid indication, I & F

Dynamic Characteristics

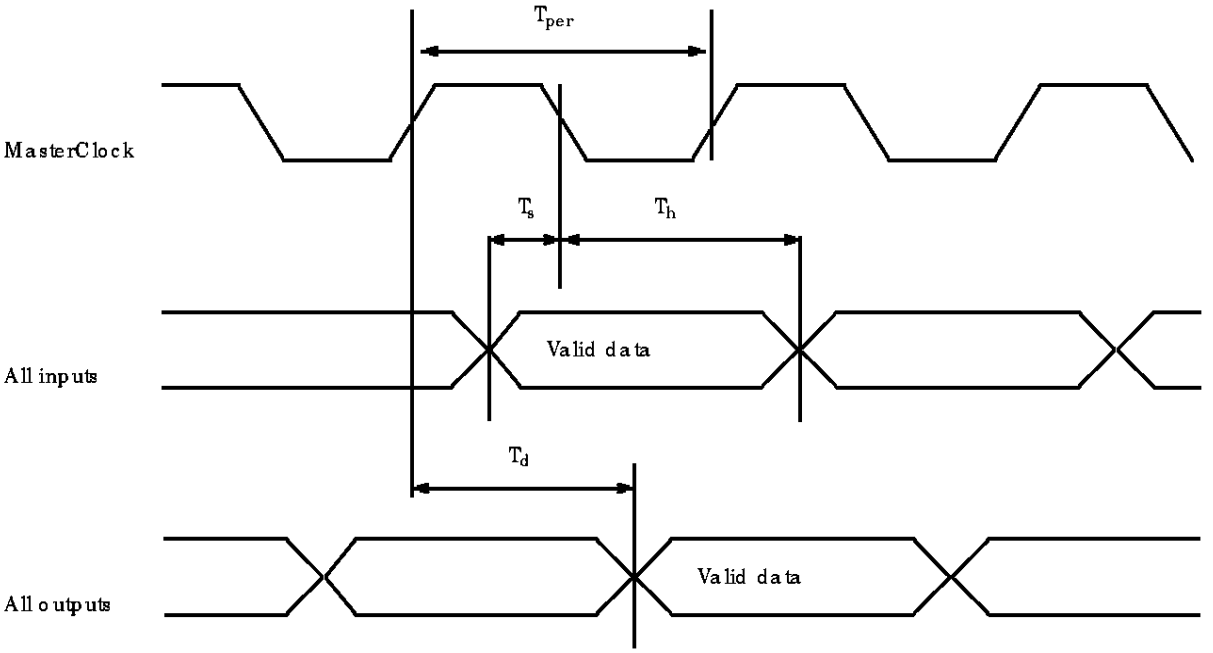


Fig. 5: Modem Interface: timing relation

Modem interface, AC Electrical Characteristics						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
T_{per}	Clock Period		28	40.69		ns
T_s	Setup		3			ns
T_h	Hold		14			ns
T_d	Data delay	20 pF load	3		17	ns

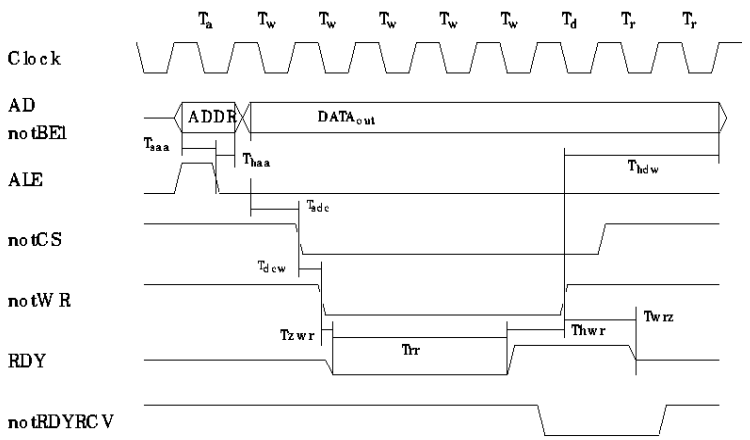
Microprocessor Interface

Pins & Functional Description

Note: See also the microprocessor support part of the glue logic, especially notBE1 carries bit [0] of internal address. Also internal address bits [8:1] are carried on AD[9:2], note the one bit shift due to the Intel i960™ memory model

Name	Type	Function
AD[11:8]	I	Address (MTC-20126 returns 8 bits data)
AD[7:0]	IO	Multiplexed Address/ Data
ALE	I	Address Latch Enable
RDY	OZ	Ready signal
notInterrupt	OD	Interrupt (Active low by default)
notCS	I	Chip Select (Active low)
notWR	I	Write access (Active low)
notRD	I	Read access (Active low)

Dynamic Characteristics



Write cycle

Fig. 6: Write access (microprocessor writes data into MTC-20126)

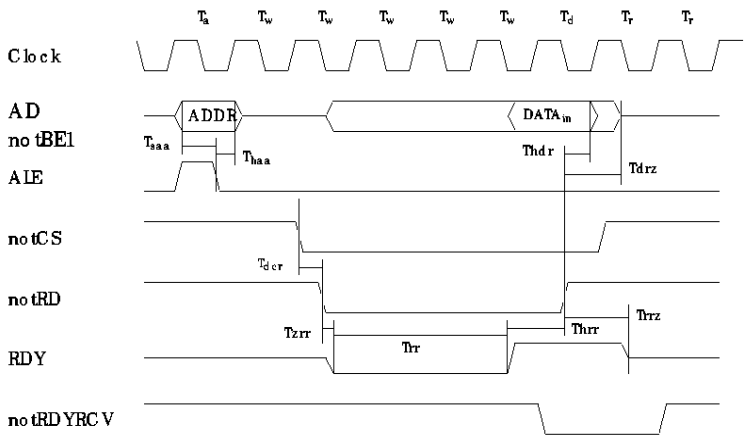


Fig. 7: Read access (microprocessor reads data from MTC-20126)

Microprocessor interface, AC Electrical Characteristics Time referenced at pins, internal timing slightly different due to combinational logic						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
T_{per}	Clock Period		28	40.69		ns
T_{saa}	Setup address (AD[11:2] and notBE1) to AIE down		11			ns
T_{haa}	Hold address (AD[11:2] and notBE1) after AIE down		11			ns
T_{dcw}	Delay notCS down to notWR down		0			ns
T_{sdc}	Setup data to (notCS| notWR) down		0			ns
T_{zwr}	RDY low and driven after (notCS| notWR) down				15	ns
T_{wrz}	RDY high z after (notCS| notWR) up				15	ns
T_{rr}	Low pulse of RDY (master clock at nominal frequency)				800	ns
T_{hdw}	Hold data after (notCS| notWR) up		0			ns
T_{hwr}	Hold (notCS| notWR) after RDY up		0			ns
T_{dcr}	Delay notCS down to notRD down		0			ns
T_{drz}	Data high z after (notCS| notRD) up		3		15	ns
T_{hdr}	Hold data after (notCS| notRD) up		3			ns
T_{zrr}	RDY low and driven after (notCS| notRD) down				15	ns
T_{hrr}	Hold (notCS| notRD) after RDY up		0			ns
T_{rrz}	RDY high z after (notCS| notRD) up				15	ns

Glue Logic

Pins & Functional Description

Table 11: Watchdog timer

Name	Type	Function
notWDTO	O	Watchdog timeout

Table 12: General purpose registers

Name	Type	Function
LED[7:0]	O	LED control pins
STB_OK[1:0]	I	UART signal quality
ACT_MONN[1:0]	I	Generic input
CID[1:0]	I	Chip identity

Table 13: Board reset logic

Name	Type	Function
notBOARD_RESET[3:0]	O	Reset signals for external devices

Table 14: Temperature sensing

Name	Type	Function
TEMP	ISC	Temperature signal

Table 15: Remote inventory

Name	Type	Function
Inventory Inputs[1:0]	I	Data Inputs
Inventory Outputs[3:0]	OD	Clock, Control and Data Outputs

Table 16: Interrupt concentration

Name	Type	Function
EXT_INT	I	External Interrupt Input

Table 17: Micropocessor support

Name	Type	Function
PCLK	I	Microprocessor master clock
AD[31:29],AD[22:18]	I	Address (MTC-20126 returns 8 bits data)
notRDYRCV	IO-OD	Ready/ Recover signal (Active low)
notADS	I	Address Data Strobe
W/notR	I	Write/ notRead, access direction
notBE[3:0]	I	Byte Enable
notBLAST	I	Burst Last
notCS[7:2]	O	Select signals (Active low), to other chips
notMEM_OE	O	Memory Output Enable
notEPROM_WE[3:0]	O	EPROM Write Enable
MUXCTL	O	Mux Control, Row or Column address
notRAS[1:0]	O	Row Address Strobe
notDRAM_WE	O	DRAM Write Enable
notCAS[3:0]	O	Column Address Strobe

† there are no notCS[1:0], they are replaced by the notRAS[1:0]

Most timings are synchronous with the PCLK rising edge, except MUXCTL. Priority inputs are defined by setup and hold and outputs by minimum and maximum delay against the clock edge.

Modem interface, AC Electrical Characteristics						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
T_s	Setup		5			ns
T_h	Hold		3			ns
T_{d1}	Delay, light load	20 pF	3		17	ns
T_{d2}	Delay, high load	100 pF	5		25	ns
T_{d3}	Delay, light load, notEPROM_WEx (special case)	20 pF	3		25	ns

UART Interfaces

Pins & Functional Description

Name	Type	Function
SIN[1:0]	I	Serial line input
SOUT[1:0]	O	Serial line output

System Clock

The MTC-20126 receives its Master Clock from the MTC-20125 Modem, this clock is the reference clock for the modem interface and is dependent on the channel spacing for ADSL applications. For DHN applications, the Master Clock comes from an undefined source (probably a master oscillator on the board).

Pins & Functional Description

Name	Type	Function
MasterCLK	I	System clock

Dynamic Characteristics

Symbol	Parameter	Minimum	Nominal	Maximum	Unit
T_{per}	Clock Period	14.153	20.345		nsec
t_r, t_f	Rise, fall time (10% - 90%)			2.5	nsec

Configuration Interface

Pins & Functional Description

Name	Type	Function
notHARD-RESET	ISC	RESET pin
SLF_TST_RAM	ID	self test of internal RAM blocks

Remark: The V_{IH} (Minimum high level input voltage) for the Reset pin is 2.4 Volt (instead of $0.7 * V_{DD}$).

Test Access Port

Pins & Functional Description

Name	Type	Function
TCK	IU	Test Clock
TDI	IU	Test Data In
TDO	OZ	Test Data Out
TMS	IU	Test Mode
TRST	ID	Test Reset (active low)
SCAN_EN	ID	Test Scan Enable

Dynamic Characteristics

The signals entering the device will be sampled at the rising edge of TCK, whilst the outgoing signals will change at the falling edge.

Maximum Boundary Scan operating frequency is 10 MHz.

Symbol	Parameter	Minimum	Nominal	Maximum	Unit
tr, tf	Rise, Fall Time (10% - 90%)			2.5	nsec

All parameters are specified for a 15 pF load capacitance.

MTC-20126

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